Modular Computers ®

CP603

6U CompactPCI System Controller for Embedded Applications

Manual ID 22085, Rev. Index 0100
Jun 00

The product described in this manual is in compliance with all applied CE standards.

This page was intentionally left blank.

Table of Contents

Preface

Chapter 1

Introduction

Chapter 2

Functional Description and Configuration

Chapter 3

Chapter 4

Appendix A

CP-RIO6-02 Module

Appendix B

CP-RIO6-10 Module

Appendix C

Transition Module VGA1

Figures

Figure Number and Title

Tables

Table Number and Title

Revision History

Revision History			
Manual/Product Title:	**CP603**		
Manual ID Number:	**22085**		
Rev. Index	**Brief Description of Changes**	**Board Index**	**Date of Issue**
0100	Initial Issue	00	June 00

Trademarks

Explanation of Symbols

CE Conformity

This symbol indicates that the product described in this manual is in compliance with all applied CE standards. Please see also the section “Applied Standards” in this manual.

Caution!

This symbol and title warn you of hazards due to electrical shocks (> 60 V) when touching products or parts of them. Failure to observe the necessary precautions as described and/or prescribed by the law may result in damage to your product and/or endanger your life/health.

Please see also the section “High Voltage Safety Instructions”.

ESD-Sensitive Device!

This symbol and title highlight the fact that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Please read also the section “Special Handling and Unpacking Instructions” on the following pageof this manual.

Attention!

This symbol and title emphasize aspects which, if not understood and taken into consideration by the reader, may result in hazards to health and/or material damage.

Note:

This symbol and title relate to information the user should read through carefully for his or her own advantage.

PEP Advantage

This symbol and title accompany information highlighting positive aspects of a *PEP* product and/or procedure.

Troubleshooting

This symbol and title accompany information about troubleshooting and problem solving.

For your safety

Your new *PEP* product has been developed and carefully tested in order to provide all the features necessary to ensure full compliance with all electrical safety requirements. It has also been designed for a long fault-free life. However, the life expectancy of your product will be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interests of your own safety and of the correct operation of your new *PEP* product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions

Warning!

All operations on this device must be carried out by sufficiently skilled personnel.

Caution!

The power supply must always be disconnected before installation, repair and maintenance operations are carried out on this product. Failure to comply with this basic precaution will subject the operator to serious electrical shock hazards. Always unplug the power cable before such operations.
Before installing your new *PEP* product into a system always ensure that your mains power is switched off. This applies also to the installation of piggybacks.

Special Handling and Unpacking Instructions

ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Care must therefore be exercised at all times during handling and inspection of the board, in order to ensure product integrity.

- Do not handle this product while it is outside its protective enclosure while it is not used for operational purposes, unless it is otherwise protected.
- Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where safe work stations are not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.
- It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or tracks on the board.

General Instructions on Usage

- In order to maintain *PEP's* product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by *PEP Modular Computers* and described in this manual or received from *PEP* Technical Support as a special handling instruction, will void your warranty.
- This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.
- In performing all necessary installation and application operations, please, follow only the instructions supplied by the present manual.
- Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board please re-pack it as nearly as possible in the manner in which it was delivered.
- Special care is necessary when handling or unpacking the product. Please consult the special handling and unpacking instructions on the previous page of this manual.

Two Year Warranty

PEP Modular Computers grants the original purchaser of a *PEP* product a ***TWO YEAR LIMITED HARDWARE WARRANTY*** as described in the following. However, no other warranties that may be granted or implied by anyone on behalf of *PEP* are valid unless the customer has the express written consent of *PEP Modular Computers*.

PEP Modular Computers warrants their own products, excluding software, to be free from manufacturing and material defects for a period of 24 consecutive months from the date of purchase. This warranty is not transferable nor extendible to cover any other users or long-term storage of the product. It does not cover products which have been modified, altered or repaired by any other party than *PEP Modular Computers* or their authorized agents. Furthermore, any product which has been, or is suspected of being damaged as a result of negligence, improper use, incorrect handling, servicing or maintenance, or which has been damaged as a result of excessive current/voltage or temperature, or which has had its serial number(s), any other markings or parts thereof altered, defaced or removed will also be excluded from this warranty.

If the customer's eligibility for warranty has not been voided he should, in the event of any claim, return the product at the earliest possible convenience to the original place of purchase, together with a copy of the original document of purchase, a full description of the application in which the product has been used and a description of the defect. Please pack the product in such a way as to ensure safe transportation (see our safety instructions).

PEP provides for repair or replacement of any part, assembly or sub-assembly at the company's own discretion, or to refund the original cost of purchase, if appropriate. In the event of repair, refunding or replacement of any part, the ownership of the removed or replaced parts reverts to *PEP Modular Computers*, and the remaining portion of the original guarantee, or any new guarantee to cover the repaired or replaced items, will be transferred to cover the new or repaired items. Any extensions to the original guarantee are considered gestures of goodwill, and will be defined in the "Repair Report" issued by *PEP* with the repaired or replaced item.

PEP Modular Computers will not accept liability for any further claims resulting directly or indirectly from any warranty claim, other than the above specified repair, replacement or refund. In particular, all claims for damage to any system or process in which the product was employed, or any loss incurred as a result of the product not functioning at any given time, are excluded. The extent of *PEP Modular Computers* liability to the customer shall not exceed the original purchase price of the item for which the claim exists.

PEP Modular Computers issues no warranty or representation, either explicit or implicit, with respect to its products' reliability, fitness, quality, marketability or ability to fulfil any particular application or purpose. As a result, the products are sold "as is," and the responsibility to ensure their suitability for any given task remains that of the purchaser. In no event will *PEP* be liable for direct, indirect or consequential damages resulting from the use of our hardware or software products, or documentation, even if *PEP* were advised of the possibility of such claims prior to the purchase of the product or during any period since the date of its purchase.

Please remember that no *PEP Modular Computers* employee, dealer or agent is authorized to make any modification or addition to the above specified terms, either verbally or in any other form, written or electronically transmitted, without the company's prior consent.

Chapter 1

Introduction

This page was intentionally left blank.

1. Introduction

1.1 Introduction to CompactPCI

The *PEP Modular Computers* CompactPCI product described in this chapter operates with the PCI bus architecture to support additional I/O and memory-mapped devices as required by various industrial applications. For detailed information concerning the CompactPCI standard, please consult the complete Peripheral Component Interconnect (PCI) and CompactPCI Specifications. For further information regarding these standards and their use, visit the homepage of the *PCI Industrial Computer Manufacturers Group (PICMG)*.

Many system-relevant CompactPCI features that are specific to *PEP Modular Computers* CompactPCI systems may be found described in the *PEP* CompactPCI System Manual. Due to its size, this manual cannot be downloaded via the internet. Please refer to the section “Related Publications” at the end of this chapter for the relevant ordering information.

The CompactPCI System Manual includes the following information:

- Common information that is applicable to all system components, such as safety information, warranty conditions, standard connector pinouts etc.
- All necessary information to combine *PEP Modular Computers* racks, boards, backplanes, power supply units and peripheral devices in a customized CompactPCI system, as well as configuration examples.
- Data on rack dimensions and configurations as well as information on mechanical and electrical rack characteristics.
- Information on the distinctive features of *PEP Modular Computers* CompactPCI boards, such as functionality, hotswap capability. In addition, an overview is given for all existing *PEP Modular Computers* CompactPCI boards with links to the relating datasheets.
- Generic information on the *PEP Modular Computers* CompactPCI backplanes, such as the slot assignment, PCB form factor, distinctive features, clocks, power supply connectors and signalling environment, as well as an overview of the *PEP Modular Computers* CompactPCI standard backplane family.
- Generic information on the *PEP Modular Computers* CompactPCI power supply units, such as the input/output characteristics, redundant operation and distinctive features, as well as an overview of the *PEP Modular Computers* CompactPCI standard power supply unit family.

1.2 *PEP* Double-height CPU Boards

The *PEP* range of double height 6U CompactPCI CPU boards is based on Socket-7 and Pentium III processors and has been designed to operate in a common software environment.

Socket 7 Family

The CP610 is a system controller which controls three PCI buses comprising one local and two external CompactPCI buses (on P1/P2 and P4/P5). The onboard PCI bus supports a Fast Ethernet port and one PMC slot. The VGA interface is integrated within the Chipset. To achieve high CPU and memory performance the board includes 512kB L2 Cache. DRAM is 32 MB or 64 MB soldered which together with the SODIMM provide up to 320 MB main memory. All standard PC interfaces are implemented and assigned to the front panel and to the rear connector P3.

The CP600 is a system controller which is identical to the CP610 in every respect except that it does not have the second CompactPCI interface at P4/P5 while P3 is optional.

The CP611 is a non-system controller which is identical to the CP600 apart from having a different PCI/PCI (non-transparent) bridge at P1/P2. This makes possible the addition of further CP611's together with a system controller CPU on one CompactPCI bus, i.e. multiprocessing.

The CP612 is a special controller; on the CompactPCI interface on P1/P2 there is a non transparent bridge implemented, as with the CP611. On the second CompactPCI interface at P4/P5 the CP612 controls an additional independent CompactPCI bus as a system controller.

Celeron and Pentium III Family

The CP603 is a high performance CompactPCI system controller board designed to utilize the Intel Celeron™ and Pentium III microprocessors and future processors. This board is based on the Intel 440BX AGPsets and can support CPU speeds of 300 MHz through 850 MHz and host bus speeds of 66 MHz to 100 MHz.

This integrated system board controls three PCI buses comprising one local and two external CompactPCI buses on P1/P2 and one with a special PCI extender at P1/P2. The onboard bridge controls seven CompactPCI slots to the left side of the backplaneand the PCI extender controls an addtional seven CompactPCI slots to the right side of the backplane.

The onboard PCI bus supports two Fast Ethernet ports, one UltraWide SCSI interface and one PMC slot. System features include memory options between 64 MB and 768 MB via DIMM SDRAM modules with and without ECC support, high-performance AGP VGA video support, two IDE ports, two COM ports, a parallel port, two USB interfaces and an optional onboard flash disk. All standard PC interfaces are implemented and assigned to the front panel and to the rear connectors P3, P4 and P5.

Features of the *PEP* Range of Double-height CPU boards

Table 1-1: Comparison between CP600, CP610, CP611, CP612 and CP602/3

Feature	CP600	CP610	CP611	CP612	CP602/3
System Controller CPU 32-bit	P1/P2	P1/P2	--	P4/P5	P1/P2
Max CompactPCI peripheral slots	7 (6U)	14 (3U)	--	7 (3U)	7 and with PCI extender 14 (6U)
Rear I/O	Optional on P3	Yes on P3	Optional on P3	Optional on P3	Yes on P3, P4 , P5
Non-transparent PCI/PCI bridge	No	No	Yes	Yes	No

1.3 CP603 Product Overview

The CP603 is a quality, high performance system motherboard designed around Intel Pentium III Coppermine microprocessors. The board utilizes the Intel BX AGPset and supports CPU speeds of 300 MHz through 850 MHz. The CP603, with its built-in AGP Port, provides high performance capabilities that are ideal for a wide range of industrial applications.

The CP603 is available with either one or two CompactPCI interfaces (depending on version). The version with the 2nd CompactPCI bus is able to address a maximum of 14 slots but at the expense of the PMC slot.

Finding an optimum equilibrium between performance and power dissipation, the CP603 is a reliable Celeron™ and Pentium III controlled board supporting a clock speed of 850 MHz and higher when available.

Designed for stability and packaged in a rugged format, the board fits into all applications situated in industrial environments. The low power consumption of the board is further assured through the use of low power technology.

The board is compatible with the operating system Microsoft Windows NT®. However, the performance of CompactPCI can be tailored to suit real-time applications and operating systems like VxWorks or QNX which are instrumental to the success of CompactPCI in these market sectors.

In industrial applications the mechanical configuration frequently necessitates easy access to the main module interfaces. For this reason all critical user I/O's (keyboard, USB, VGA, Ethernet and COM1) are routed to the front-panel. The remaining two IDE hard-disk interfaces, one SCSI interface and one floppy-disk interface are provided as onboard pin-row connectors. The CP603 supports either front panel I/O or rear panel interfacing in conjunction with the the rear I/O transition module CP-RIO6-02 for the routing of all onboard interfaces

1.4 CP603 Board Introduction

The CP603 is a CompactPCI Pentium II Celeron™ and Pentium lll family based single-board computer specifically designed for use in highly integrated platforms with solid mechanical interfacing for a wide range of industrial environment applications.

Some of the CP603's outstanding features are:

- compliance with CompactPCI Interface 2.1
- optional one/two independent CompactPCI interfaces
- suitable for all Intel Celeron™ and Pentium III processors in the 370-pin PPGA and FCPGA package
- up to 768 MB SDRAM main memory
- 256 kB FLASH for BIOS
- onboard high performance AGP VGA controller
- Flash Disk
- two IDE interfaces
- two Fast Ethernet devices: 10BaseT & 100BaseTX
- one UltraWide SCSI interface
- integrated Hardware monitor
- "hot-swap" compliant

The CP603 includes the following commonly used peripheral devices:

- floppy disk interface
- keyboard/USB controller
- two serial ports(ESD protected and EMI compliant)
- counter/timers
- watchdog timer
- real-time clock
- parallel port
- rear I/O at P3, P4, P5
- PMC Interface and break-out on front panel

1.5 Optional Modules for Expanded Capability

The CP603 has been designed to support the attachment of optional Transition modules (such as the CP602 VGA1, CP610 HDD and CP602 BR1 module.

Transition CP602 VGA1-Module

The Transition VGA-Module includes additional standard PC interfaces, a high-performance AGP VGA video interface, one configurable COM2 port and one ECP/EPP compatible Parallel Port. Front panel LED's and interfaces characterize the CP603 board as a whole and are, therefore, described in this chapter. The jumper settings and pinout of the transmission module are described under separate headings in the "Transition Module" chapter.

Hard-Disk/Flash Disk Module

A double-width version of the CP603 containing an adapter module which allows connection of a 2.5" hard-disk is available and can be mounted as an alternative or in addition to the transition module. The hard-disk itself has to be mounted directly on the adapter module.

As an option, instead of the hard-disk, a 2.5" flash disk can be mounted on the module.

Bridge Module

A Bridge module may be added on the optional connector CON17 to support seven extra CompactPCI slots to the right side, making up to 14 Compact PCI slots available.

Rear I/O Modules

There are two optional Rear I/O modules available for use with the CP603. The CP603 CPU board equipped with the P3, P4 and P5 Rear I/O connectors may be upgraded by means of the Rear I/O module CP-RIO6-02, while the version of the baseboard including only the P3 connector is capable of utilizing the CP-RIO6-10 Rear I/O module. These modules are designed to be inserted at the back of the system and are plugged into the backplane CompactPCI connectors which are in line with the CPU board.

When the CP-RIO6-02 Rear I/O module is used, the signals from all the main board/ front panel connectors are routed to the module interfaces. Thus the use of Rear I/O modules makes it much easier to remove the CPU in the rack as there is practically no cabling on the CPU board.

1.6 Power Consumption

The CP603 board is based on the Intel Celeron and Pentium III processor in the PPGA and FCPGA 370-pin package.

The goal of this description is to provide a method to calculate the power consumption for the CP603 base board and for additional configurations. The processor dissipates the majority of the thermal power.

The power consumption table lists the voltage and current specifications for the CP603 board and the CP603 accessories. The values are measured with a 8 slot passive CompactPCI backplane and two power supplies, one for the CPU and the other one for the harddisk. During the measurement the power consumption of the backplane can be ignored. The operating systems was DOS 6.22 without power management and Windows NT 4.0 with power management. The measured values varied, because the power depended on the processor activity.

1.6.1 Power Consumption Tables for CP603 Baseboard

Values Measured at DOS Prompt and without keyboard

Table 1-2: Power Consumption: CP603 Baseboard with Celeron Processor (DOS)

Power (Voltage)	Celeron 300 MHz 128/256 MB Memory	Celeron 366 MHz 128/256 MB Memory	Celeron 433 MHz 128/256 MB Memory	Celeron 566 MHz 128/256 MB Memory	Celeron 733 MHz 128/256 MB Memory
5V	12.75 W	14.05 W	15.55 W	13.10 W	Tbd
3.3V	6.43 W	6.56 W	6.63 W	6.74 W	Tbd
Total	19.18 W	20.61 W	22.18 W	18. 84W	Tbd

Table 1-3: Power Consumption: CP603 Baseboard with Pentium lll Processor (DOS)

Power (Voltage)	Pentium III 600 MHz 128/256 MB Memory	Pentium III 700 MHz 128/256 MB Memory	Pentium III 850 MHz 128/256 MB Memory
5V	15.05 W	15.7 W	17.3 W
3.3V	8.11 W	8.18 W	8.23 W
Total	23.16W	23.88 W	25.53 W

Values Measured with Windows NT 4.0 Running (no application started) and without Keyboard

Table 1-4: Power Consumption: CP603 Baseboard with Celeron Processor (NT)

Power (Voltage)	Celeron 300 MHz 128/256 MB Memory	Celeron 366 MHz 128/256 MB Memory	Celeron 433 MHz 128/256 MB Memory	Celeron 566 MHz 128/256 MB Memory	Celeron 733 MHz 128/256 MB Memory
5V	4.4 W	4.5 W	4.7 W	3.90 W	Tbd
3.3V	5.74 W	5.77 W	5.77 W	5.80 W	Tbd
Total	10.14 W	10.27 W	10.47 W	9.70 W	Tbd

Table 1-5: Power Consumption: CP603 Baseboard with Pentium III Processor (NT)

Power (Voltage)	Pentium III 600 MHz 128/256 MB Memory	Pentium III 700 MHz 128/256 MB Memory	Pentium III 850 MHz 128/256 MB Memory
5V	4.3 W	4.45 W	5.2 W
3.3V	6.93 W	6.90 W	7.0 W
Total	11.23 W	11.35 W	12.2 W

1.6.2 Power Consumption Table for CP603 Accessories

Table 1-6: Power Consumption Table: CP603 Accessories

Module	Power 5 V	Power 3.3 V
Keyboard	100 mW	--
128 MB DIMM module (18 chips)	--	800 mW
256 MB DIMM module (18 chips)	--	800 mW
DiskOnChip 16 MB	100 mW	--
DiskOnChip 144 MB	100 mW	--
CP602 PCI extender with second CPCI interface	--	300 mW

1.7 Temperature Range

The CP603 enables the extended temperature range from -25°C up to + 75°C. All onboard components are specially selected for the higher temperature range. For the higher temperatures the new FCPGA processors are suitable. These processors are produced with the new 0.18-micron process which have lower power consumption and support higher case temperatures.

1.7.1 Temperature Range and Air Flow Tables

These values are measured with typical applications under DOS and Windows NT 4.0. In worst case situations, the value varies and the temperature range must be reduced. For all situations the max. case temperature of the Pentium III processor must be below the max. temperature value. This temperature value can be measured with the onboard remote temperature sensor. To guarantee the max. temperature, the BIOS supports a temperature control feature. The temperature range for the active heatsink is (for all processors) 0°C - 60°C.

Table 1-7: Temperature Range and Air Flow - Celeron Processor

Heatsink Version	Range	300 MHz	366 MHz	433 MHz	566 MHz	733 MHz
8HP Passive	0°C – 50°C	0 m/s	0.5 m/s	0.5 m/s	0 m/s	Tbd
	0°C – 60°C	0.5 m/s	1 m/s	1 m/s	0.5 m/s	Tbd
	-25°C – 75°C	1 m/s	--	--	1 m/s	Tbd
Max. Temp.	--	85°C case	85°C case	85°C case	90°C die	Tbd
Tjunction offset	--	--	--	--	2.6°C	Tbd

Table 1-8: Temperature Range and Air Flow - Pentium III Processor

Heat Sink Version	Range	600 MHz	700 MHz	850 MHz
8HP Passive	0°C – 50°C	0.5 m/s	0.5 m/s	1.0 m/s
	0°C – 60°C	1.0 m/s	1.0 m/s	2.0 m/s
	-25°C – 75°C	2.0 m/s	2.0 m/s	--
Max. Temp.	--	82°C die	80°C die	80°C die
Tjunction offset	--	3.6°C	4.1°C	4.9°C

Please see explanatory notes for these tables on the next page

Temperature Range and Air Flow Tables explanatory notes:

- 0 m/s air flow means: standard convection cooling, and the board is in a upright position.
- 1.0 m/s air flow was measured with the PEP ASM 7 rack on the CPU heatsink (6U CompactPCI rack and 1U cooling fan).
- The Tjunction offset is the worst-case difference between the thermal reading from the on-die thermal diode and the hottest location on the processors die.
- The CP603 is a very compact, highly integrated CPU board which uses high performance components. This results in the generation of considerable amount of heat. In order to preclude damage to the board and increase performance reliability, it is recommended to use an additional airflow to increase the live time.

1.8 Software Support

Real-time operating systems such as QNX, VxWorks, and others are supported. The standard PC features supported by the BIOS also allow for PC operating systems such as Linux, MS-DOS, Windows 9X, Windows 2000, Windows NT 4.0 (Embedded).

1.9 CP603 Main Specifications

Table 1-9: CP603 Main Specifications

CP603	Specifications
CPU	Intel Celeron processor with 128 kB L2 on-die cache in 370-pin PPGA package at 300 MHz*, 366 MHz*, 433 MHz * up to 533 MHz Intel Celeron processor with 128 kB L2 on-die cache in 370-pin FCPGA package at 566 MHz*, 733 MHz* Intel Pentium III processor with 256 kB L2 on-die cache in 370-pin FCPGA package at 600 MHz*, 700 MHz* up to 850 MHz * These processor speeds are available from Intel Applied Computer Group. For longer life requirements, use only these kind of processors.
Memory	66/100 MHz system memory bus 256 kB L2 on-die full speed processor cache 64 MB up to 768 MB SDRAM with ECC via three DIMM sockets 512 kB Flash (or optional SRAM with 256 kB or 512 kB) Optional DiskOnChip™ module up to 96 MB 256 Byte EEPROM for storing CMOS data when operating without battery and 2 x 256 EEPROM for user purposes
Super I/O	The FDC37C672 from SMSC is an ISA Plug and Play-compatible I/O device that provides the following functions: - Two 16C550 compatible UARTs with 16 bytes FIFO - PS/2 Keyboard and mouse interface - Floppy disk controller up to 2.88 MB - Parallel port ECP/EPP compatible
Chipset	Intel 82440BX PCI/AGP controller - GTL Processer interface - Integrated DRAM controller - AGP and PCI interface Intel 82371EB PCI/ISA IDE Xcelerator (PIIX4E) - Multifunction PCI to ISA bridge - Enhanced DMA controller - Interrupt controller based on two 82C59's - Timer based on 82C84 - Real-Time clock - Power management logic - Supports two USB interfaces - Supports two IDE interfaces
AGP/VGA interface	Controller: C&T 69030 Video memory: 4 MB Resolution: up to 1600x1200x16 @ 60 Hz

Table continued on following page

Table 1-9: CP603 Main Specifications

CP603	Specifications
Fast Ethernet Interface	Controller: Intel 82559 Fast Ethernet Controller Data Rate: 10 & 100 Mbps Ethernet: Full 802.2 & 802.3 IEEE compliance supporting 10Base-T and 100Base-TX Cabling: Category 5 two-pair cabling
UltraWideSCSI interface	Controller: Symbios SYM53C895 Connector: 68-pin high density SCSI connector
CompactPCI Bus Interface	Compatible with CompactPCI Specification V 2.0, Rev. 3.0 64-bit/33 MHz master interface 3.3V/5.0V compatible
Rear I/O Interface	For optimized cabling purposes rear I/O is possible via the P3, P4, P5 connectors in conjunction with the rear I/O transition module CP-RIO6-02.
Hotswap-Compatible	The CP603 supports the addition or removal of other boards with power on. Individual clocks for each slot and Enum signal handling are in compliance with the PCIMG 2.1 Hotswap Specification.
PMC Interface	Compliant with single CMC specification IEEEP1386 32-bit master interface 3.3V and 5.0V compatible
General	Dimensions: 233.35 mm x 160 mm Operating temp.: 0 °C to +60 °C –25 °C to +75 °C (optional) Storage temp.: –55 °C to +85 °C Operating humidity: 0% to 95% non-condensing Weight: CP603 8HP without heatsink: 690 grams
Front Panel Interfaces	PS-2 style connector for Keyboard/Mouse via Y-cable (6-pin mini-DIN) COM1 9-pin D-Sub (RS232) COM2 9-pin D-Sub (RS232, RS422, RS485) USB two 4-pin connectors Parallel port 25-pin D-Sub Ethernet two RJ-45 connectors VGA 15-pin D-Sub SVGA connector PMC opening for PMC front panel LED's: ACT, LNK, SPEED Ethernet status per channel SCSI SCSI activity TMP thermal control WDG Watchdog timer status Reset button, guarded
Onboard interfaces	Two IDE interfaces supporting Ultra/DMA each for 2 hard disks or CD-ROM on 40-pin 2.54mm connectors One floppy disk interface (up to 2.88 MB) 68-pin high density SCSI connector for UltraWide SCSI

Table continued on following page

Table 1-9: CP603 Main Specifications

CP603	Specifications
Thermal Management / System Monitoring	Watchdog: software configurable watchdog generates IRQ, SMI or hardware reset Hardware monitor: LM81 monitoring temperature, fan speed and all onboard voltages Temperature monitor: MAX 1617 monitoring the CPU on-die and board temperature
Common Features	DC power monitors (3.3V and 5V) Battery socket and 3.0V lithium battery for RTC: VARTA Type CR2025 PANASONIC BR2020
Software Support	Award BIOS with Preboot Agent contained within 256 kB of Flash memory. The BIOS parameters are saved in the EEPROM. The CP603 is able to operate without disks, keyboard and video operating systems: Linux, QNX, VxWorks, Windows NT etc. MS-DOS, Windows 95, 98, Windows 2000

1.10 Applied Standards

1.10.1 CE Compliance

The *PEP Modular Computers'* CompactPCI systems comply with the requirements of the following CE-relevant standards:

- Emission EN50081-1
- Immission EN50082-2
- Electrical Safety EN60950

1.10.2 Mechanical Compliance

- Mechanical Dimensions IEEE 1101.10

1.10.3 Environmental Tests

- Vibration IEC68-2-6
  Random Vibration, Broadband IEC68-2-64 (3U boards)
- Permanent Shock IEC68-2-29
- Single Shock IEC68-2-27

1.11 Related Publications

1.11.1 CompactPCI Systems/Boards

- CompactPCI Specification, V. 2.0, Rev. 3.0

Chapter 2

Functional Description and Configuration

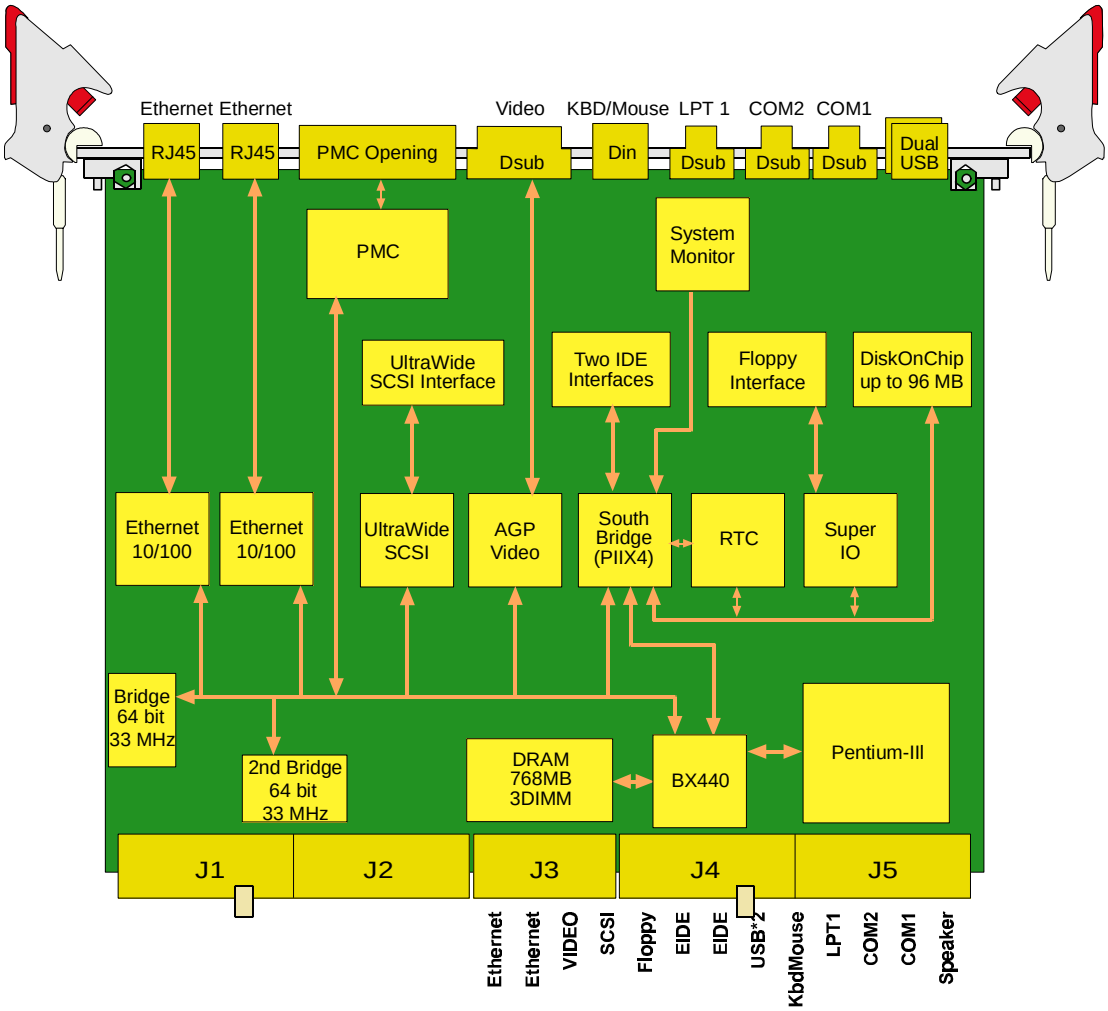
Functional Description and Configuration

Functional Description and Configuration

2. Functional Description and Configuration

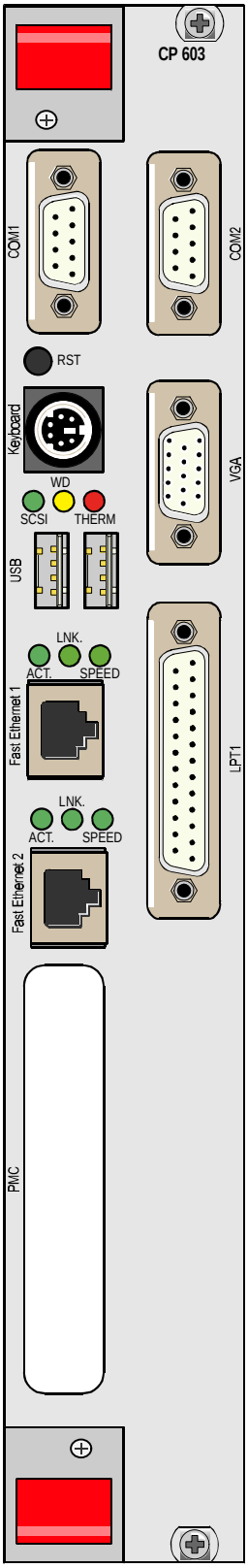
2.1 Functional Block Diagram

Figure 2-1: CP603 Functional Block Diagram



2.2 Front Panel

Figure 2-2: CP603 Front Panel



The front panel includes three LED's placed under the keyboard/mouse interface connector ("Board LED's") and three LED's placed over the two Ethernet connectors ("Ethernet LED's"). The functions of the LEDs are as follows:

Board LED's:

- "SCSI" (green) = if ON, The SCSI interface is active
- "WD" (yellow) = Watchdog timer status; if ON, the watchdog is active.
- "THERM" (red) = Temperature alarm; if ON, an overtemperature has occurred. To rectify, reduce the CPU clock speed.

Ethernet LED's (green):

- Left = Active; if ON, the Ethernet link is active.
- Middle = Link; if ON, transmission is in progress via the Ethernet link.
- Right = Speed; if ON transmission speed is 100 MBit/s.

2.3 Board Layouts

Figure 2-3: CP603 Board Layout (Front Side)

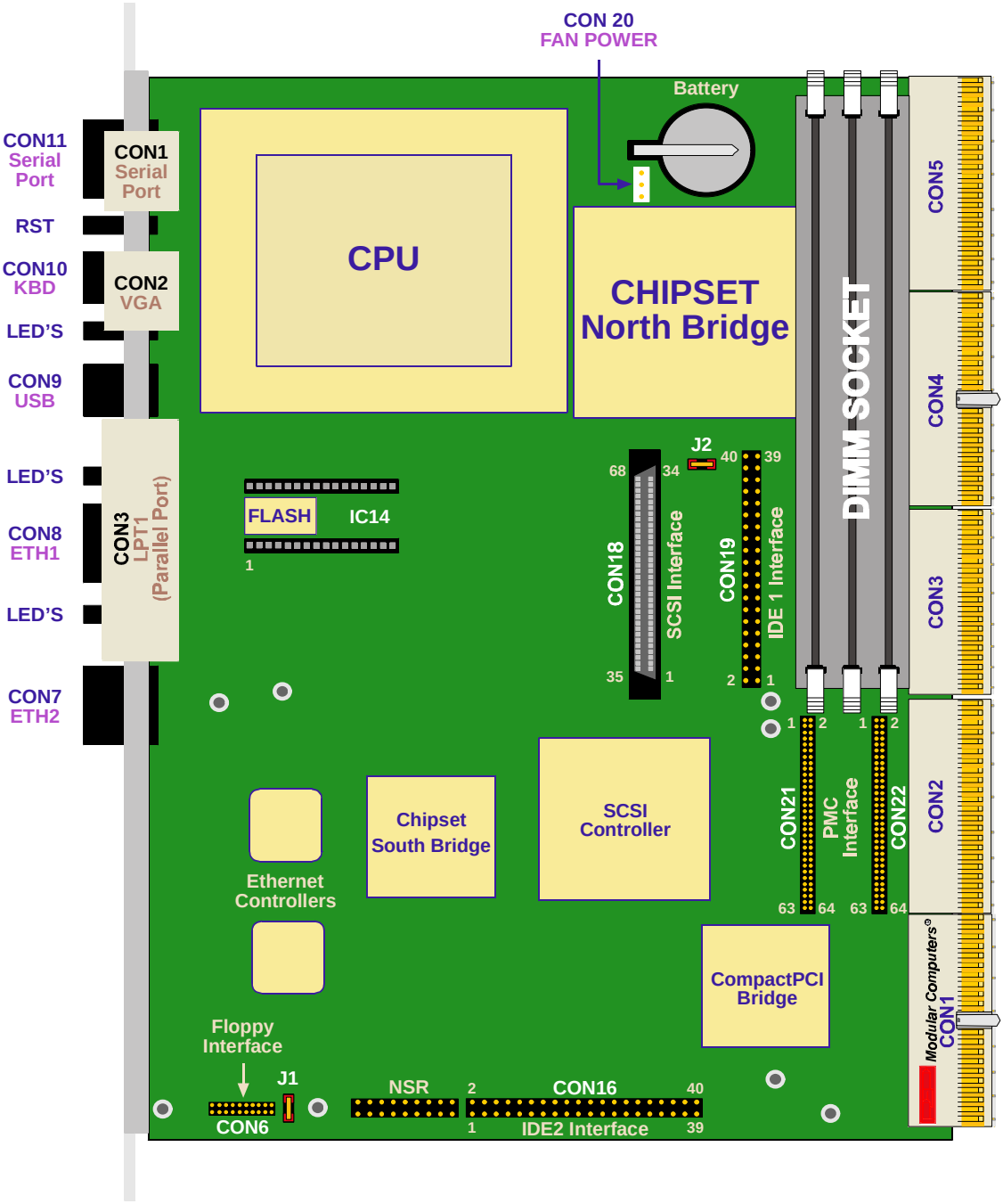
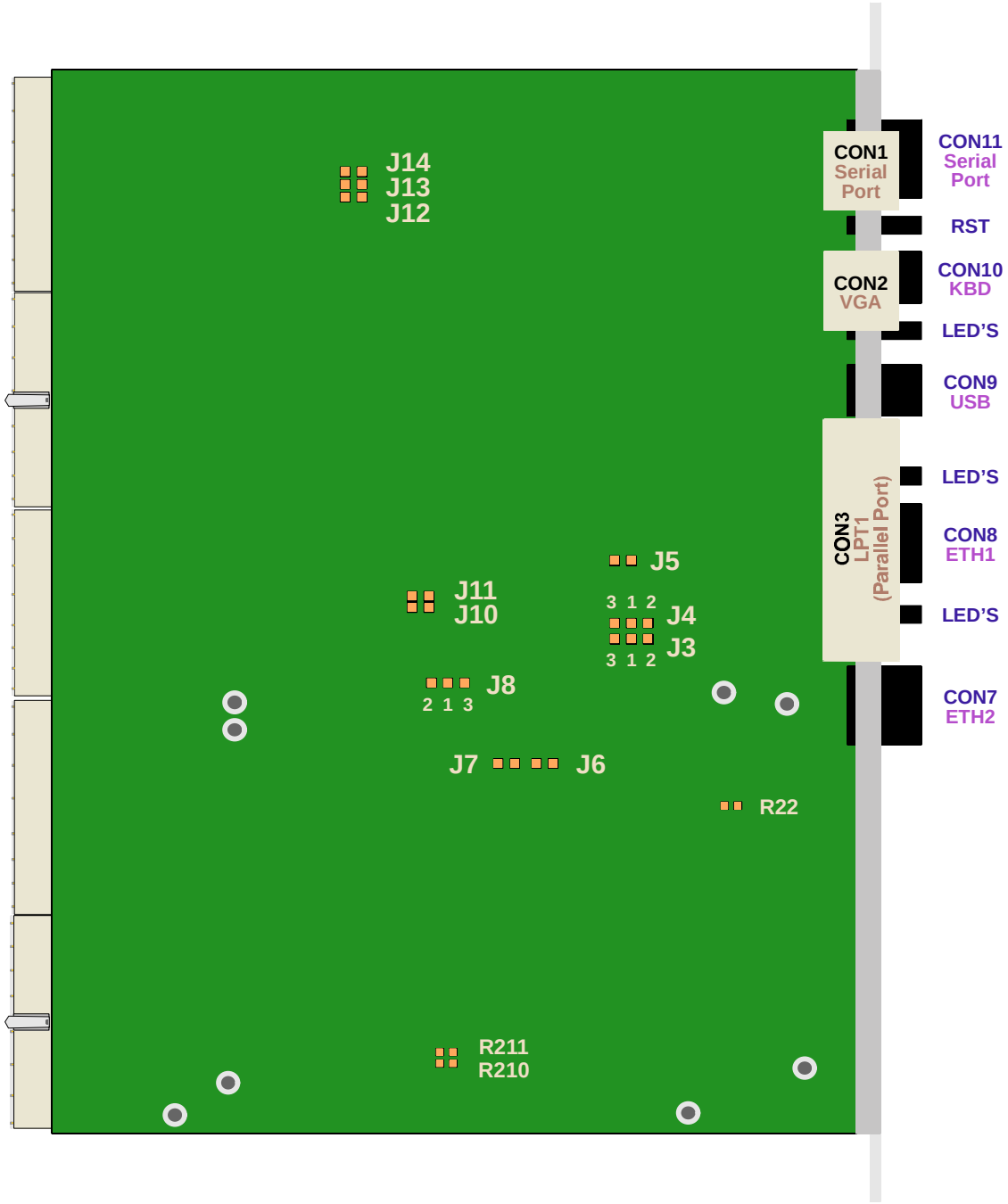


Figure 2-4: CP603 Board Layout (Reverse Side)



2.4 Main Features

The following sections describe the main features of the principal functional blocks of the CP603 and include, where relevant, jumper settings and pinouts.

2.4.1 CPU

The CP603 supports all Intel Celeron and Pentium lll processors in the 370-pin PPGA and FCPGA packages up to 850 MHz with 256 kB L2 on-die cache. The processor speed is automatically selected. The onboard voltage regulator is automatically programmed by the processor's VID pins to provide the required voltage. All supported onboard memory can be cached.

2.4.2 Memory

The CP603 has three locations for installing memory modules in DIMM sockets. The board supports a maximum of 768 MB. All installed memory will be automatically detected, so there is no need to set any jumpers. Either 72-bit (ECC) or 64-bit (non-ECC) 100 MHz, 3.3 V, PC/100 compliant SDRAM on 168 pin gold DIMM's are supported by the CP603 board. DIMM modules may be installed in any socket and in any order.

Table 2-1: Memory Options Utilizing DIMM Sockets

DIMM 0	DIMM 1	DIMM 2	Total
64 MB	--	--	64 MB
64 MB	64 MB	--	128 MB
64 MB	64 MB	64 MB	192 MB
128 MB	--	--	128 MB
128 MB	128 MB	--	256 MB
128 MB	128 MB	128 MB	384 MB
256 MB	--	--	256 MB
256 MB	256 MB	--	512 MB
256 MB	256 MB	256 MB	768 MB

Important:

All memory components and DIMM's used with this board must comply with the following PC SDRAM specifications:

- PC SDRAM Specification
- PC Serial Presence Detect Specification

Do not mix registered and unbuffered memory. Mixing non-ECC memory and ECC memory causes all ECC features to be disabled.

2.4.3 Interrupts

Two enhanced 8259-style interrupt controllers provide a total of fifteen interrupt inputs with features which include level and edge-triggered inputs, fixed and rotating priorities and individual input masking. Interrupt sources include: Counter/timers, serial I/O, RTC, keyboard/mouse, printer, floppy disk, IDE interfaces and four interrupt sources on the CompactPCI backplane.

2.5 Peripherals

The following standard peripherals are available on the CP603 board:

2.5.1 Real-Time Clock

The real-time clock performs time keeping functions and includes 256 bytes of general purpose battery backed CMOS RAM. Features include an alarm function, programmable periodic interrupt and a 100-year calendar. All battery-backed CMOS RAM data remains stored in an additional EEPROM. This makes data loss impossible.

2.5.2 Counter/Timer

Three 8254-style counter/timers are included on the CP603 as defined for the PC/AT.

2.5.3 Watchdog Timer

A watchdog timer is provided, which forces an SMI, IRQ or Reset condition (configurable in the watchdog register). The watchdog time can be programmed in 12 steps ranging from 125 msec up to 256 seconds. If the watchdog timer is enabled, it cannot be stopped or reprogrammed.

2.5.4 Battery

The CP302 is provided with a 3.0V “coin cell” lithium battery for the RTC.

To replace the battery please proceed as follows:

- Turn off power
- Remove the battery
- Place the new battery in the socket.
- Make sure that you insert the battery the right way round. The plus pole must be on the top!

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer. Suitable batteries include the VARTA CR2025 and PANASONIC BR2020

Important additional information about the battery follows on the next page.

Important

- Care must be taken to ensure that the battery is correctly replaced.
- The battery should be replaced only with an identical or equivalent type recommended by the manufacturer.
- Dispose of used batteries according to the manufacturer's instructions.
- The typical life expectancy of a 170 mAh battery (VARTA CR2025) is 4 - 5 years with an average on-time of 8 hours per working day at an operating temperature of 30°C. However, this typical value varies considerably because the life expectancy is dependent on the operating temperature and the standby time (shutdown time) of the system in which it operates.
  To ensure that the lifetime of the battery has not been exceeded it is recommended to exchange the battery after 3 - 4 years.

2.5.5 Reset

The CP603 is automatically reset by a precision voltage monitoring circuit that detects a drop in voltage below the acceptable operating limit of 4.725 V for the 5V line and below 3.0V for the 3.3V line, or in the event of a power failure of the DC/DC converter. Other reset sources include the watchdog timer and local push-button switch. The CP603 responds to any of these sources by initializing local peripherals and issuing the PCIRST# signal on the CompactPCI bus.

The CP603 supports several reset options:

- Front panel push button
- Watchdog
- Backplane reset (PRST input)
- Power control (5V, 3.3V and CPU core voltage)

2.5.6 SMBus Devices

The CP603 provides a System Management Bus (SMBus) for access to several system monitoring and configuration functions. The SMBus consists of a two-wire I2C bus interface. The following table describes the function and address of every onboard SMBus device.

Table 2-2: SMBus Devices Addresses

Device	SMB Address
PIIX4 slave port	0001000Xb
Temperature sensor MAX1617	0011000Xb
Hardware Monitor LM81	0101100Xb
EEPROM	1010XXXXb

2.5.7 Thermal Management / System Monitoring

The LM81 can be used to monitor several critical hardware parameters of the system, including power supply voltages, fan speeds and temperatures; all of which are very important for the proper operation and stability of a high-end computer system. The LM81 provides an I2C™ serial bus interface.

The voltages of the onboard power supply (+12 V, -12V, +5V, +3.3V, +1.5V, Vcore) are supervised. The onboard hardware monitor is able to detect the CPU fan speed and an external fan speed in revolutions per minute (RPM). The presence of the fans is automatically detected.

The integrated MAX1617 temperature sensors monitor the CPU temperature to make sure that the system is operating at a safe temperature level. If the temperature is too high, the sensors automatically reduces the CPU clock frequency, depending on the mode chosen in the BIOS set.

2.5.8 Serial EEPROM

A serial EEPROM is provided, organised into 4 blocks with 256 bytes per block (24LC08). This EEPROM is connected to the I2C™ bus provided by the PIIX4E.

Table 2-3: EEPROM Address Map

Address	Function
1010000xb	DIMM 0 SPD
1010001xb	DIMM 1 SPD
1010010xb	DIMM 2 SPD
1010011xb	Not available
1010100xb	VxWorks parameter (24LC08)
1010101xb	Free for user purposes (24LC08)
1010110xb	Free for user purposes (24LC08)
1010111xb	CMOS backup (24LC08)

Important:

It is strongly recommended that users access only the two free EEPROM banks

2.5.9 Flash Disk

There are two Flash devices available as described below, one for the BIOS and one 32-pin socket for a flexible Flash configuration.

1. BIOS Flash

The CP603 uses a 256 kB flash memory to store BIOS firmware. It can be updated as new versions of the BIOS become available. You may easily upgrade your BIOS using the AWARD *awdflash* utility .

2. Socket memory

Different flash module versions are available. In order to achieve flexibility with low cost the flash disk is not soldered, but connected via a special module from M-Systems (DiskOnChip™ 2000).

- Standard flash memory of up to 512 KB in a 32-pin DIL package
  - AMD29F010
  - AMD29F040
- Standard EEPROM memory in a 32-pin DIL package
  - AMD27C010
  - AMD27C020
- DiskOnChip™ flash memory:
  - 8 - 96 MB

For higher flash disk capacity it is recommended to use an ATA flash disk.

2.5.10 PCI- to-PCI Bridge

The Intel 21154 bridge is a 64-bit 33 MHz PCI-to-PCI bridge device. It supports up to seven CompactPCI loads through a passive backplane.

The 21154 is a second generation PCI-to-PCI bridge and is fully compliant with the PCI Local Bus Specification Rev. 2.1. The 64-bit interface interoperates transparently with either 64-bit or 32-bit devices.

The PC-to-PCI bridge allows the primary and secondary PCI bus to operate concurrently. A master and target on the same PCI bus can communicate while the other PCI bus is busy.

2.6 Board Interfaces

2.6.1 Keyboard/Mouse Interface

The onboard keyboard controller is 8042 software compatible.

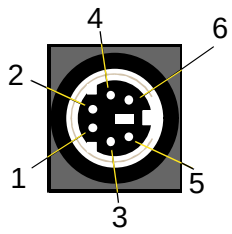


Figure 2-5: Keyboard/Mouse Connector

The PC/AT standard keyboard/mouse connector is a PS/2-type 6-pin shielded mini-DIN connector.

A special adapter to connect a mouse device and/or a keyboard to the PS/2 connector is available from *PEP.*

2.6.1.1 Keyboard/Mouse Connector CON10 Pinout

Table 2-4: Keyboard Connector CON10 Pinout

Pin	Name	Function	In/Out
1	KDATA	Keyboard data	In/Out
2	MDATA	Mouse data	In/Out
3	GND	Ground signal	--
4	VCC	VCC signal	--
5	KCLK	Keyboard clock	Out
6	MCLK	Mouse clock	Out

Note:

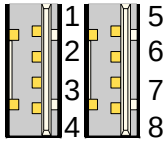
The keyboard power supply unit is protected by a 500 mA fuse. All signal lines are EMI-filtered.

2.6.2 USB Interfaces

The Universal Serial Bus (USB), is a most versatile port. This one port type can function as a serial, parallel, mouse, keyboard, or joystick port and is capable of supporting up to 127 daisy-chained peripheral devices.

Figure 2-6: USB Connector CON9

There are two identical USB interfaces on the CP603 baseboard each with a maximum transfer rate of 12 Mbit provided for connecting USB devices. One USB peripheral may be connected to each port. To connect more than two USB devices an external hub is required.



2.6.2.1 USB Connector CON9 Pinout

Table 2-5: USB Connector CON9 Pinout

Pin	Name	Function
1	VCC	VCC signal
2	UV0-	Differential USB-
3	UV0+	Differential USB+
4	GND	GND signal
5	VCC	VCC signal
6	UV0-	Differential USB-
7	UV0+	Differential USB+
8	GND	GND signal

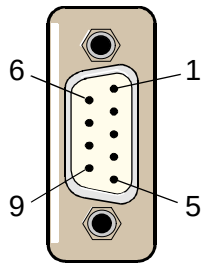
Note:

The USB power supply feeding the two connectors is protected by a 1.5 A fuse. All signal lines are EMI-filtered.

2.6.3 Serial Interface

On the baseboard a single PC-compatible 9-pin male D-sub serial port is available which features 5V charge-pump technology so eliminating the need for a +12V and -12V supply. This port allows the connection of RS232 devices to the CP603 board. This interface includes the complete signal set for handshaking, modem control and data transfer up to 460.8 kB/s. Serial Port COM1 can be enabled/disabled under SW control. Selection can be made inside the BIOS or via the Rear I/O configuration register. The standard software configuration is Front I/O.

Figure 2-7: PC-compatible D-Sub Serial Connector CON11



2.6.3.1 Serial Port Connector CON11 Pinout

Table 2-6: Serial Port Connector CON11 Pinout

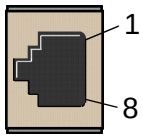
D-sub 9	Signal	Function	In/Out
1	DCD	Data carrier detect	In
2	RXD	Receive data	In
3	TXD	Transmit data	Out
4	DTR	Data terminal ready	Out
5	GND	Signal ground	--
6	DSR	Data send request	In
7	RTS	Request to send	Out
8	CTS	Clear to send	In
9	RI	Ring indicator	In

2.6.4 Fast Ethernet Interface

The CP603 board includes a 10BASE-T/100BASE-TX network solution based on the Intel 82559 Fast Ethernet PCI Bus Controller. The controller contains two receive and transmit FIFO buffers that prevent data overruns or underruns while waiting for access to the PCI bus. Three LED's monitor the network conditions. The Boot from LAN feature is supported, for details please refer to section 4.5, BIOS Features Setup, in chapter 4.

Figure 2-8: Ethernet/Fast Ethernet Connector

The Ethernet connector is realized as an RJ45 twisted-pair connector. The Interface provides automatic detection and switching between 10Base-T and 100Base-TX data transmission.



2.6.4.1 Ethernet Connectors CON7 and CON8 Pinout

The CON7 and CON8 connectors provide the 10Base-TX/100Base-TX interface to the Ethernet controller. These connectors are enabled/disabled via the BIOS setting or the Rear I/O Configuration Register. The standard software is Front I/O.

Table 2-7: Ethernet Connectors CON7 and CON8 Pinout

RJ45	Signal	Function
1	TX+	Transmit +
2	TX-	Transmit -
3	RX+	Receive +
4	NC	--
5	NC	--
6	RX-	Receive -
7	NC	--
8	NC	--

2.6.5 Ethernet LED Status

Green: Link: This LED monitors 10Base-T and 100Base-TX connections. The LED lights up to indicate a successful network connection. If this indicator is off, the cable connection may be faulty.

Green: Activity: This LED monitors network activity. The LED lights up when network packets are sent or received through the RJ45 port. When off, the computer is not sending or receiving network data.

Green: Speed: The LED lights up to indicate a successful 100Base-TX connection. While off the connection is operating at 10Base-T

2.6.6 Fan Power Supply

A fan for CPU cooling can be connected via the power connector CON20.

2.6.6.1 Fan Power Supply Connector CON20 Pinout

Table 2-8: Fan Power Supply Connector CON20 Pinout

CON20	Function
1	GND
2	+5V or +12V
3	Sense input

2.6.7 IDE Interfaces

The IDE interfaces supports PIO mode 4 with transfers of up to 14 MB per second and Bus Master Ultra-DMA 33 transfer up to 33 MB per second. The EIDE controller can sustain a maximum transfer rate of 33 MB per second between the EIDE drive buffer and PCI.

The CP603 features two independent Enhanced IDE ports onboard, a primary one (IDE1) and a secondary one (IDE2). The primary CON19 and the secondary CON16 are 40-pin, 2.54 mm male connector AT standard interfaces for IDE hard-disks.

Each IDE interface provides support for up to two hard-disks and/or CD-ROM drives (two master-slave couples). All hard-disks can be used in cylinder head sector (CHS) mode with the BIOS also supporting the logical block addressing (LBA) mode.

Important

Each of the two interfaces, IDE1 and IDE2, support a maximum of two hard-disks connected in the master-slave mode. To configure the first as a master disk and the second as a slave disk, please refer to the hard-disk manufacturer's documentation.

IDE connector pinouts follow on next page.

2.6.7.1 IDE Connectors CON16 and CON19 Pinouts

The following table sets out the pin numbers of connectors CON16 and CON19 and details their corresponding signal names and functions. The colored stripe on a ribbon cable (pin 1) from the IDE1 port should face towards the PMC module and from the IDE2 port it should face towards the front panel.

Table 2-9: Pinout of AT Standard Connectors IDE1 and IDE2

Pin	Signal	Function	In/Out
1	IDERESET	Reset HD	Out
2	GND	Ground signal	--
3	HD7	HD data 7	In/Out
4	HD8	HD data 8	In/Out
5	HD6	HD data 6	In/Out
6	HD9	HD data 9	In/Out
7	HD5	HD data 5	In/Out
8	HD10	HD data 10	In/Out
9	HD4	HD data 4	In/Out
10	HD11	HD data 11	In/Out
11	HD3	HD data 3	In/Out
12	HD12	HD data 12	In/Out
13	HD2	HD data 2	In/Out
14	HD13	HD data 13	In/Out
15	HD1	HD data 1	In/Out
16	HD14	HD data 14	In/Out
17	HD0	HD data 0	In/Out
18	HD15	HD data 15	In/Out
19	GND	Ground signal	--
20	N/C	--	--
21	IDEDRQ	DMA request	In
22	GND	Ground signal	--
23	IOW	I/O write	Out
24	GND	Ground signal	--
25	IOR	I/O read	Out

Table continued on following page

Table 2-9: Pinout of AT Standard Connectors IDE1 and IDE2

Pin	Signal	Function	In/Out
26	GND	Ground signal	--
27	IOCHRDY	I/O channel ready	In
28	GND	Ground signal	--
29	IDEDACKA	DMA Ack	Out
30	GND	Ground signal	--
31	IDEIRQ	Interrupt request	In
32	N/C		--
33	A1	Address 1	Out
34	N/C	--	--
35	A0	Address 0	Out
36	A2	Address 2	Out
37	HCS0	HD select 0	Out
38	HCS1	HD select 1	Out
39	LED	LED driving	In
40	GND	Ground signal	--

2.6.8 Floppy Drive Interface

The onboard floppy disk controller supports either 5.25 inch or 3.5 inch (1.44 MB or 2.88 MB) Floppy Disks. A 20-pin male connector provides the signals for an optional floppy-drive that can be installed by means of a special adapter.

2.6.8.1 Floppy Drive Connector CON6 Pinout

On the CP603 a 20-pin male connector CON6 provides the signals for the floppy disk. To connect the floppy disk, a 20-to-34 pin adapter is necessary. In the following the pinout of the 20-pin connector is described. The remaining 14 pins of the adapter correspond to those of a standard floppy interface.

Table 2-10: Floppy Drive Connector CON6 Pinout

Pin	Signal	Function	In/Out
20	DRVDEN0	Drive and media select	Out
19	DRVDEN1	Drive and media select	Out
18	MTR0	Motor 0 enable	Out
17	INDEX	Index pulse	In
16	DS0	Driver select 0	Out
15	DS1	Driver select 1	Out
14	DIR	Step direction	Out
13	MTR1	Motor 1 enable	Out
12	WDAT	Write data	Out
11	STEP	Step pulse	Out
10	TRK0	Track 0 signal	In
9	WGAT	Write enable	Out
8	RDATA	Read data	In
7	WP	Write protect	In
6	DSKCH	Disk change	In
4	HDSEL	Head select	Out
1-4	GND	Ground signal	--

Note:

The adapter must be mounted directly onto the Floppy Drive. No intermediate cable between the floppy drive and the adapter is necessary.

2.6.9 SCSI Interface

The CP603 is equipped with an ultra-wide SCSI controller with a 68-pin female high-density SCSI D-sub connector CON18. The CPU board includes a Symbios Logic SYM53C895 embedded single channel PCI SCSI host adapter. The onboard ultra-wide SCSI controller is a PCI chip which uses Bus Master technology. This allows the SCSI controller to independently manage data transfer between the SCSI peripherals and the computer system memory.

Logic, termination, or resistor loads are not required to connect devices to the SCSI controller, other than termination in the device at the end of the cable. The SCSI bus is terminated on the server board with active terminators that cannot be disabled. The onboard device must always be at one end of the bus.

The SCSI LED indicates drive activity in the SCSI controller.

Note:

It is advisable to use only good quality SCSI lines, otherwise transmission problems may occur.

The connectors of 16-bit SCSI devices have 68 pins. The connectors of 8-bit SCSI devices have 50 pins; therefore if it is required to connect 8-bit SCSI devices to the ultra-wide SCSI controller an adapter will be necessary (from 68-pin to 50-pin).

SCSI connector pinout follows on next page.

2.6.9.1 SCSI Connector CON18 Pinout

Table 2-11: SCSI Connector CON18 Pinout

Pin	Signal	Pin	Signal
1	GND	35	-DB(12)
2	GND	36	-DB(13)
3	GND	37	-DB(14)
4	GND	38	-DB(15)
5	GND	39	-DB(P1)
6	GND	40	-DB(0)
7	GND	41	-DB(1)
8	GND	42	-DB(2)
9	GND	43	-DB(3)
10	GND	44	-DB(4)
11	GND	45	-DB(5)
12	GND	46	-DB(6)
13	GND	47	-DB(7)
14	GND	48	-DB(P)
15	GROUND GND	49	GROUND
16	DIFFSENS GND	50	CONNECTOR-Detect
17	TERMPWR#	51	TERMPWR
18	TERMPWR#	52	TERMPWR
19	RESERVED#	53	RESERVED
20	GND	54	GROUND
21	GND	55	-ATN
22	GND	56	GROUND
23	GND	57	-BSY
24	GND	58	-ACK
25	GND	59	-RST
26	GND	60	-MSG
27	GND	61	-SEL
28	GND	62	-C/D
29	GND	63	-REQ
30	GND	64	-I/O
31	GND	65	-DB(8)
32	GND	66	-DB(9)
33	GND	67	-DB(10)
34	GND	68	-DB(11)

= no ground

2.6.10 CompactPCI Bus Interface

The complete CompactPCI connector configuration is composed of five connectors referred to as P1, P2, P3, P4, and P5.

Their function is as follows:

- P1/P2: 64-bit CompactPCI interface with PCI bus signals, arbitration, clock and power
- P3, P4 and P5: Rear I/O interface

The board is capable of driving up to seven CompactPCI slots, with individual arbitration and clock signals. In addition to standard CompactPCI system functionality, the CP603 also supports Hotswap capability which means that hotswappable boards can be removed from or installed in the system whilst it is running.

The CP603 is designed for the CompactPCI bus architecture. The CompactPCI standard is electrically identical to the PCI local bus. However, these systems are enhanced to operate in rugged industrial environments and to support multiple slots.

CompactPCI connector pinouts begin on next page.

2.6.10.1 Compact PCI Connectors CON1 (P1) and CON2 (P2)

The CP603 is provided with two 2 mm x 2 mm female CompactPCI bus connectors, P1 and P2.

Table 2-12: CompactPCI Bus Connector CON1 (P1) Pinout

Pin	Row A	Row B	Row C	Row D	Row E	Row F
25	5V	REQ64#	ENUM#	3.3V	5V	GND
24	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND
23	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
22	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
21	3.3V	AD[9]	AD[8]	M66EN#	C/BE[0]#	GND
20	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	3.3V	SDONE	SBO#	GND	PERR#	GND
16	DEVSEL	GND	V(I/O)	STOP#	LOCK#	GND
15	3.3V	FRAME#	IRDY#	GND	TRDY#	GND
12-14	Key Area					
11	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND
8	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	REQ#	GND	3.3V	CLK	AD[31]	GND
5	BRSVP1A5	BRSVP1B5	RST#	GND	GNT#	GND
4	BRSVP1A4	GND	V(I/O)	INTP	INTS	GND
3	INTA#	INTB#	INTC#	5V	INTD#	GND
2	TCK	5V	TMS	TDO	TDI	GND
1	5V	-12V	TRST#	+12V	5V	GND

Table 2-13: CompactPCI Bus Connector CON2 (P2) Pinout

Pin	Row Z	Row A	Row B	Row C	Row D	Row E	Row F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	CLK6	GND	RSV	RSV	RSV	GND
20	GND	CLK5	GND	RSV	GND	RSV	GND
19	GND	GND	GND	RSV	RSV	RSV	GND
18	GND	RSV	RSV	RSV	GND	RSV	GND
17	GND	RSV	GND	PRST#	REQ6#	GNT6#	GND
16	GND	RSV	RSV	DEG#	GND	RSV	GND
15	GND	RSV	GND	FAL#	REQ5#	GNT5#	GND
14	GND	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND
13	GND	AD[38]	GND	V(I/O)	AD[37]	AD[36]	GND
12	GND	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND
11	GND	AD[45]	GND	V(I/O)	AD[44]	AD[43]	GND
10	GND	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND
9	GND	AD[52]	GND	V(I/O)	AD[51]	AD[50]	GND
8	GND	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND
7	GND	AD[59]	GND	V(I/O)	AD[58]	AD[57]	GND
6	GND	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND
5	GND	C/BE[5]#]	GND	V(I/O)	C/BE[4]#]	PAR64	GND
4	GND	V(I/O)	RSV	C/BE[7]#]	GND	C/BE[6]#]	GND
3	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	GND	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND

2.6.10.2 Compact PCI Rear I/O Connectors CON3-CON5 (P3-P5)

The CP603 conducts all I/O signals through the rear I/O connectors P3, P4 and P5. The CP603 board provides optional rear I/O connectivity for peripherals for special compact systems. All standard PC interfaces are implemented and assigned to the front panel and to the Rear I/O connectors CON3, CON4 and CON5 (P3, P4 and P5).

When the Rear I/O module is used, the signals of some of the main board/front panel connectors are routed to the module interface. Thus the Rear I/O module makes it much easier to remove the CPU in the rack as there is practically no cabling on the CPU board.

For the system Rear I/O feature a special backplane is necessary. The CP603 with Rear I/O is compatible with all standard 6U CompactPCI passive backplanes with Rear I/O support on the system slot

CompactPCI Rear I/O connector pinouts begin on next page.

Table 2-14: Backplane CON3 (P3) Pin Definitions

Pin	Z	A	B	C	D	E	F
19	GND	IDE.PWRGD	IDE.IOCS16#	IDE.IOCHRDY	IDES.IRQ	IDEP.IRQ	GND
18	GND	IDES.CS3#	IDES.CS1#	IDEP.CS3#	IDEP.CS1#	IDES.DAK#	GND
17	GND	IDEP.D15	IDEP.D14	IDEP.D13	IDEP.D12	IDES.DRQ	GND
16	GND	IDEP.D11	IDEP.D10	IDEP.D9	IDEP.D8	IDEP.DAK#	GND
15	GND	IDEP.A0	IDEP.A1	VCC	IDEP.A2	IDEP.DRQ	GND
14	GND	IDEP.D7	IDEP.D6	IDEP.D5	IDEP.D4	IDEP.IOW#	GND
13	GND	IDEP.D3	IDEP.D2	IDEP.D1	IDEP.D0	IDEP.~IOR	GND
12	GND	FD.DS0#	FD.MSEN0	FD.MTR0#	FD.INDEX#	FD.WDATA#	GND
11	GND	FD.DS1#	FD.DSKCHG#	FD.MTR1#	FD.DENSEL	FD.RDATA#	GND
10	GND	FD.WP#	FD.HDSEL#	FD.DIR#	FD.TRK0#	FD.STEP#	GND
9	GND	FD.WGATE#	IDES.D15	IDES.D14	IDES.D13	USB0+	GND
8	GND	IDES.D12	IDES.D11	VCC	IDES.D10	USB0-	GND
7	GND	IDES.D9	IDES.D8	IDES.D7	IDES.D6	IDES.IOW#	GND
6	GND	IDES.D5	IDES.D4	IDES.D3	IDES.D2	IDES.IOR#	GND
5	GND	ABORT#	MSDAT	SPKR	KBDAT	RSV	GND
4	GND	PRST#	MSCLK	VCC	KBCLK	S2RXD	GND
3	GND	S2CTS	S2RTS	S2DSR	S2DCD	S2TXD	GND
2	GND	IDES.D1	IDES.D0	S2RIN	S2DTR	--	GND
1	GND	IDES.A0	IDES.A1	IDES.A2	RSV	--	GND

Legend:

IDE Primary and shared Primary/Secondary signals
IDE Secondary signals
Floppy signals
COM2, and USB signals
Mouse, keyboard, reset, speaker, and reserved signals

The greyed table cells indicate the power grouping

Table 2-15: Backplane CON4 (P4) Pin Definitions

Pin	Z	A	B	C	D	E	F
25	GND	VCC	S1DTR	USB1+	+3.3V	VCC	GND
24	GND	S1CTS	PD0	Init	GND	Link LED 2	GND
23	GND	+3.3V	S1RXD	USB1-	VCC	GND	GND
22	GND	S1RTS	PD1	Active LED 2	GND	Transmit – 2	GND
21	GND	+3.3V	S1TXD	AutoFD	GND	GND	GND
20	GND	S1DSR	PD2	SelectIN	GND	Transmit + 2	GND
19	GND	+3.3V	PD3	Strobe	GND	GND	GND
18	GND	S1RIN	PD4	Speed LED 2	GND	Receive – 2	GND
17	GND	+3.3V	PD5	BUSY	GND	GND	GND
16	GND	S1DCD	PD6	VIO	GND	Receive + 2	GND
15	GND	+3.3V	PD7	ACK	GND	GND	GND
12-14	GND	Key	Area	--	--	--	GND
11	GND	DCLKVGA	OCO	PE	GND	GND	GND
10	GND	DATAVGA	WDLED	Active LED 1	GND	Transmit - 1	GND
9	GND	HSYVGA	TEMPLED	Select	GND	GND	GND
8	GND	VSYVGA	SCSILED	VIO	GND	Transmit + 1	GND
7	GND	GND	PIIX4 GPO30	Error	GND	GND	GND
6	GND	BVGA	PIIX4 GPO29	Speed LED 1	GND	Receive - 1	GND
5	GND	GND	PIIX4 GPO28	PIIX4 GPI16	GND	GND	GND
4	GND	GVGA	GND	VIO	GND	Receive + 1	GND
3	GND	GND	PIIX4 GPO27	PIIX4 GPI15	VCC	GND	GND
2	GND	RVGA	VCC	PIIX4 GPI14	GND	Link LED 1	GND
1	GND	VCC	-12V	PIIX4 GPI13	+12V	VCC	GND

Legend:

Ethernet1 and Ethernet2 signals
Parallel Port signals
GPIO
COM1 and USB signals
LED signals
VGA and reserved signals

The greyed table cells indicate the power grouping

Table 2-16: Backplane CON5 (P5) Pin Definitions

Pin	Z	A	B	C	D	E	F
22	GND	NC	NC	NC	NC	NC	GND
21	GND	NC	NC	NC	NC	NC	GND
20	GND	NC	NC	NC	NC	NC	GND
19	GND	NC	NC	NC	NC	NC	GND
18	GND	NC	NC	NC	NC	NC	GND
17	GND	NC	NC	NC	NC	NC	GND
16	GND	NC	NC	NC	NC	NC	GND
15	GND	NC	NC	NC	NC	NC	GND
14	GND	NC	NC	NC	NC	NC	GND
13	GND	NC	NC	NC	NC	NC	GND
12	GND	NC	NC	NC	NC	NC	GND
11	GND	RS232 Cont.	GND	VIO	Fan Sense	Free	GND
10	GND	Free	-DB11	-DB10	GND	-DB9	GND
9	GND	-DB8	GND	VIO	-I/O	-REQ	GND
8	GND	-C/D	-SEL	-MSG	GND	-RST	GND
7	GND	-ACK	GND	VIO	-BSY	-ATN	GND
6	GND	TERMPWR	TERMPWR	TERMPWR	GND	TERMPWR	GND
5	GND	TERMPWR	GND	VIO	TERMPWR	TERMPWR	GND
4	GND	VIO	DET_CON1	DET_CON2	GND	-DB_P	GND
3	GND	-DB7	GND	-DB6	-DB5	-DB4	GND
2	GND	-DB3	-DB2	-DB1	-DB0	-DB_P1	GND
1	GND	-DB15	RIOPRESENT	-DB14	-DB13	-DB12	GND

Legend:

SCSI signals

Control signals

The greyed table cells indicate the power grouping

2.6.11 PMC Interface

For flexible and easy configuration one onboard PMC socket is available. The PN1 and PN2 connectors provide the signals for the 32-bit PCI Bus. The 64-bit interface for the PMC interface is not implemented. User defined I/O signals are not supported.

This interface has been designed to comply with the IEEEP1386.1 specification which defines a PCI electrical interface for the CMC (Common Mezzanine Card) form factor. The CP603 provides for either a 5V or 3.3V PMC PCI signaling environment.
PMC connector pinouts follow on next page.

2.6.11.1 PMC Connectors CON21 and CON22 Pinouts

Table 2-17: PMC Connectors CON21 and CON22 Pinouts

PN1/JN1				PN2/JN2			
Pin #	**Signal Name**	**Signal Name**	**Pin #**	**Pin #**	**Signal Name**	**Signal Name**	**Pin #**
1	Signal	-12V	2	1	+12V	Signal	2
3	Ground	Signal	4	3	Signal	Signal	4
5	Signal	Signal	6	5	Signal	Ground	6
7	BUSMODE1#	+5V	8	7	Ground	Signal	8
9	Signal	Signal	10	9	Signal	Signal	10
11	Ground	Signal	12	11	BUSMODE2#	+3.3V	12
13	Signal	Ground	14	13	Signal	BUSMODE3#	14
15	Ground	Signal	16	15	+3.3V	BUSMODE4#	16
17	Signal	+5V	18	17	Signal	Ground	18
19	V (I/O)	Signal	20	19	Signal	Signal	20
21	Signal	Signal	22	21	Ground	Signal	22
23	Signal	Ground	24	23	Signal	+3.3V	24
25	Ground	Signal	26	25	Signal	Signal	26
27	Signal	Signal	28	27	+3.3V	Signal	28
29	Signal	+5V	30	29	Signal	Ground	30
31	V (I/O)	Signal	32	31	Signal	Signal	32
33	Signal	Ground	34	33	Ground	Signal	34
35	Ground	Signal	36	35	Signal	+3.3V	36
37	Signal	+5V	38	37	Ground	Signal	38
39	Ground	Signal	40	39	Signal	Ground	40
41	Signal	Signal	42	41	+3.3V	Signal	42
43	Signal	Ground	44	43	Signal	Ground	44
45	V (I/O)	Signal	46	45	Signal	Signal	46
47	Signal	Signal	48	47	Ground	Signal	48
49	Signal	+5V	50	49	Signal	+3.3V	50
51	Ground	Signal	52	51	Signal	Signal	52
53	Signal	Signal	54	53	+3.3V	Signal	54
55	Signal	Ground	56	55	Signal	Ground	56
57	V (I/O)	Signal	58	57	Signal	Signal	58
59	Signal	Signal	60	59	Ground	Signal	60
61	Signal	+5V	62	61	Signal	+3.3V	62
63	Ground	Signal	64	63	Ground	Signal	64

2.7 Onboard Configuration Description

2.7.1 External BIOS Selection

It is possible to redirect the first CPU fetch from the onboard flash to the Flash socket using Jumper J2. If the jumper J2 is open, the board boots from the BIOS in the onboard flash memory. When J2 is closed, the board boots from the socket flash.

Table 2-18: BIOS Selection Jumper Setting

J2	Function	Comment
Closed	External Bios	Use this setting only if the onboard flash does not work.
Open	*Internal Bios*	*Normal boot from the onboard BIOS*

The default setting is indicated by italics

2.7.2 Memory Type Selection

These solder jumpers select the memory type to be installed on the Flash socket IC14.

Table 2-19: Memory Type Selection Jumper Setting

J3	J4	Memory type
1-2	1-2	SRAM with 256 kB or 512 kB
1-3	*1-3*	*All DiskOnChip, FLASH and EEPROM types up to 4 Mbit*

The default setting is indicated by italics

2.7.3 Flash Type Selection

This solder jumper selects the Flash type to be installed on the Flash socket IC14.

Table 2-20: Flash Type Selection Jumper Setting

J11	Function
Closed	4 Mbit Flash type
Open	*2 Mbit Flash type*

The default setting is indicated by italics

2.7.4 External Reset J1 Jumper Setting

An external reset button can be plugged to this connector. The system will do a cold start after the Reset button is pushed.

Table 2-21: External Reset J1 Jumper Setting

J1	Function
Open	No reset
Closed	Reset system

2.7.5 Fan Power Supply Voltage Selection

The voltage for the CPU cooling fan can be configured using jumpers J13 and J14

Table 2-22: Fan Power Supply Voltage Selection Jumper Setting

J14	J13	Function
Closed	Open	+5V
Open	*Closed*	*+12V*

The default setting is indicated by italics

2.7.6 PCI VI/O setting

The CP603 provides for either a 5V or 3.3V PCI signaling environment.

The BVI/O power jumpers on the board are used to power the buffers on the peripheral boards and the PMC interface. The BVI/O does not provide power to the CompactPCI interface. The CompactPCI VI/O must be configured via the backplane.

Table 2-23: PCI VI/O setting

Board VI/O setting	R210	R211
5V	*Open*	*Closed*
3.3V	Closed	Open

The default setting is indicated by italics

2.7.7 Shorting Chassis GND (Shield) to Logic GND

The front panel including the front panel connectors are isolated to the logic ground. This zero Ohm resistor enables connection between the chassis GND and logic GND.

Table 2-24: Shorting Chassis GND (Shield) to Logic GND

R22	Function
Open	*Connectors are isolated to logic GND*
Short	Connectors are connected to logic GND and chassis GND

The default setting is indicated by italics.

2.8 Software Configuration

2.8.1 System Memory Map

The CP603 board uses the standard AT ISA system memory map.

The following table sets out the memory map for the first megabyte:

Table 2-25: System Memory Map

Memory Hex.	Size	Function
0xE0000-0xFFFFF	**128k**	BIOS implemented in Flash EPROM Reset vector 0xFFFF0
0xD0000-0xDFFFF	**64k**	Flash Disk
0xC8000-0xCFFFF	**32k**	Free
0xC0000-0xC7FFF	**32k**	BIOS of the VGA card.
0xA0000-0xBFFFF	**128k**	Normally used as video RAM as follows: CGA video : 0x0B8000 0x0BFFFF Monochrome video : 0x0B0000 0x0B7FFF EGA/VGA video : 0x0A0000 0x0AFFFF
0x000000-0x9FFFF	**640k**	DOS reserved memory space
0x00000-0x00501	**1.25k**	BIOS data area and interrupt space

2.8.2 I/O Memory Map

The following table sets out the memory map for the I/O memory:

Table 2-26: Memory Map for I/O Memory

Address Range (Hex.)	Device
000,00F	MA controller #1
020,021	Interrupt controller #1
022,02F	Reserved
040,043	Timer 1
048,04B	Timer 2
060,063	Keyboard interface
070,071	RTC port
080,08F	DMA page register
0A0,0A1	Interrupt controller #2
0C0,0DF	DMA controller #2
0E0,0EF	Reserved
0F0,0FF	Math coprocessor
170,17F	Secondary IDE channel
1F0,1FF	Primary IDE channel
278,27F	Parallel port LPT2
280#	Watchdog trigger
281#	Onboard reset
282#	Watchdog time
283#	Rear I/O control
284#	Interrupt routing
286#	I/O status
288#	Board version
289#	Hardware index
28A#	Jumper status
28B#	Logic index
28C#	PCI Interrupt routing
28E#	Memory management
28F	Flash Socket Page

Table continued on following page

Table 2-26: Memory Map for I/O Memory

2E8,2EF	Serial port COM4
2F8,2FF	Serial port COM2
378,37F	Parallel printer port LPT1
3BC,3BF	Parallel printer port LPT3
3E8,3EF	Serial port COM3
3F0,3F7	Floppy Disk + Super-I/O #1 Com.
3F8,3FF	Serial port COM1
LPTn + 400	ECP port, LPTn base address +400h

= CP603 specific registers

2.8.3 Special Registers Description

The following registers are special registers specific to the CP603 enabling it to watch the onboard hardware special features and the CompactPCI control signals. Normally, only the system BIOS uses these registers but they are described here for application use as required. Take care when modifying the contents of these registers as the system BIOS may be relying on the state of the bits under their control.

2.8.3.1 Watchdog

The CP603 has one watchdog timer. This timer is provided with a programmable timeout ranging from 125 msec to 256 seconds. Failure to strobe the watchdog timer within a set time period results in a system reset, SMI or an interrupt. This can be configured via the register 0x284.

To enable the watchdog bit ”4” of the register 0x282 must be set. If the watchdog is enabled via bit ”4” this bit can not then be cleared.

With a write access to the register 0x280 the watchdog is retriggered. Once the watchdog is enabled, it must be continuously strobed within the terminal count period to avoid resetting the system hardware.

Watchdog Trigger

A write access triggers the watchdog.

The I/O location for the watchdog trigger is 0x280.

Watchdog Time

The I/O location for the watchdog configuration is 0x282.

Watchdog Configuration

Table 2-27: Watchdog Configuration

Bits	Type	Default	Function
7-5	--	0	Reserved
4	RW	0	1 = enable watchdog (write) 0 = disable watchdog (read only)
3-0	RW	0	The nominal timeout period is 20% longer than the minimum. 0 = 125msec 1 = 250msec 2 = 500msec 3 = 1sec 4 = 2sec 5 = 4sec 6 = 8sec 7 = 16sec 8 = 32sec 9 = 64sec 10 = 128sec 11 = 256sec 12-15 reserved

2.8.3.2 Reset Control Register

This register controls the reset signal for the two Ethernet controllers, the SCSI controller and the AGP interface.

The default configuration is high.

The I/O location for the reset control register is 0x281.

Table 2-28: Reset Control Register

Bits	Type	Default	Function
7-2	--	0	Reserved
1	RW	1	Reset the SCSI chip and the AGP interface 1 = set reset signal high 0 = set reset signal low
0	RW	1	Reset the Ethernet chips 1 = set reset signal high 0 = set reset signal low

2.8.3.3 Rear I/O Configuration Register

This register is used by the CPU to control the signal path (front I/O or rear I/O) of the two Ethernet interfaces and the COM1 (CON11 connector)) port. The default configuration is the front I/O interface.

The I/O location for the rear I/O register is 0x283.

Table 2-29: Rear I/O Configuration Register

Bits	Type	Default	Function
7-3	--	0	Reserved
2	RW	0	COM1 (CON11 connector) interface 1 = rear I/O interface 0 = front I/O interface
1	RW	0	Ethernet 2 interface 1 = rear I/O interface 0 = front I/O interface
0	RW	0	Ethernet 1 interface 1 = rear I/O interface 0 = front I/O interface

2.8.3.4 Interrupt Configuration Register

The interrupt configuration register holds a series of bits defining the interrupt routing for the watchdog, the power control derate signal and the CompactPCI enumeration signal. If the watchdog timer fails, it can generate three independent hardware events: reset, SMI and IRQ5 interrupt.

The enumeration signal is generated by a hotswap compatible board after insertion and prior to removal. The system uses this interrupt signal to force software to configure the new board. The derate signal indicates that the power supply is beginning to derate its power output.

The I/O location for the interrupt configuration is 0x284.

Table 2-30: Onboard Interrupt Configuration

Bits	Type	Default	Function
7-5	--	0	Reserved
4	RW	0	CPCI enum signal IRQ5 routing 1 = enable IRQ5 0 = disable IRQ5
3	RW	0	CPCI derate signal IRQ5 routing 1 = enable IRQ5 0 = disable IRQ5
2	RW	0	Watchdog hardware reset 1 = enable reset 0 = disable reset
1	RW	0	Watchdog IRQ5 routing 1 = enable IRQ5 0 = disable IRQ5
0	RW	0	Watchdog SMI routing 1 = enable SMI 0 = disable SMI

2.8.3.5 I/O Status

This register describes the local and CompactPCI control signals. The watchdog status bit indicates the status of the watchdog timer. If the timer is not retriggered within the previously set time period, the bit is set to ”0” and the watchdog LED lights up. The fail signal is an output of the power supply indicating a power supply failure. For a description of the derate and enumeration signals please see the interrupt routing register.

The I/O location for the I/O status is 0x286

Table 2-31: I/O Status

Bits	Type	Default	Function
7	R	--	Watchdog status 0 = watchdog interrupt
6	R	--	Reserved
5	R	--	Reserved
4	R	--	Reserved
3	R	--	System slot identification 0 = System slot
2	R	--	System enumeration hot swap 0 = new board
1	R	--	Supply fail signal of CPCI
0	R	--	Derating signal of CPCI

2.8.3.6 Board ID

The I/O location for the Board ID is 0x288

This register describes the hardware and the board index.

Table 2-32: Board ID

Bits	Type	Default	Function
7-0	R	1	Board version 0 = reserved 0x20 = CP602 0x21 = CP603

2.8.3.7 Hardware Index

The hardware index will signal to the software when differences in the hardware require different handling by the software. It starts with the value 0 and will be incremented with each change in hardware as development continues.

The I/O location for the Hardware Index is 0x289

Table 2-33: Hardware Index

Bits	Type	Default	Function
7-0	R	--	Revision ID 0 = Index 0000

The revision ID is incremented for each hardware or logic revision.

2.8.3.8 Jumper Status

This register can be used to read the onboard jumper configuration. The I/O location for the Jumper Status is 0x28A

Table 2-34: Jumper Status

Bits	Type	Default	Function
7	R	1	Boot jumper 1 = onboard Flash 0 = socket Flash
6-3	R	--	Reserved
2	R	--	Rear I/O module status 1 = no rear I/O module plugged 0 = rear I/O module plugged
1	R	--	Reserved
0	R	--	Reserved

2.8.3.9 Logic Version

The logic version register may be used to identify the logic status of the board by software. It starts with the value 0 and will be incremented with each logic update.

The I/O location for the Logic Version is 0x28B

Table 2-35: Logic Version

Bits	Type	Default	Function
7-0	R	--	Logic version 0 = Index 0000

The logic version is incremented for each logic update.

2.8.3.10 PCI Interrupt Routing

This register is used by the CPU to control the PCI interrupt routing. Every interrupt line of the backplane can be enabled or disabled. The interrupt mask register bits enable the appropriate bits when low and disable them when high. The default configuration is ”all interrupts enabled”.

The I/O location for the PCI interrupt routing is 0x28C.

Table 2-36: PCI interrupt Routing

Bits	Type	Default	Function
7-4	R	--	Reserved
3	RW	0	P1/2 INTD
2	RW	0	P1/2 INTC
1	RW	0	P1/2 INTB
0	RW	0	P1/2 INTA

2.8.4 Memory Management of Flash Socket

Flash devices which may be mounted in socket IC14 are accessed in paged mode, up to 512 kB are addressable in total. The page size depends on the setting of the Flash Socket Page Register; the Flash access is 8 pages with 64 kB, 16 pages with 32 kB or 64 pages with 8 kB.

The Memory Management Register should be used to select the individual pages. The I/O location is 0x28E.

Table 2-37: Memory Management

Bits	Type	Default	Function 8 kB	Function 32 kB	Function 64 kB
7-6	R	--	Reserved	--	--
5	RW	0	Address A18	--	--
4	RW	0	Address A17	--	--
3	RW	0	Address A16	Address A18	--
2	RW	0	Address A15	Address A17	Address A18
1	RW	0	Address A14	Address A16	Address A17
0	RW	0	Address A13	Address A15	Address A16

2.8.5 Flash Socket Page

The Flash Socket Page register is used to select the page size to be addressed. The size can be programmed from 8 kB to 64 kB. The default value is 8 kB which results in the following address window: 0xDE000 - 0xDFFFF.

The I/O location of the flash window setup is 0x28F.

Table 2-38: Flash Socket Page

Bits	Type	Default	Addressable Range in
7-0	RW	0	2 = 64kB 0xD0000 - 0xDFFFF 1 = 32kB 0xD8000 - 0xDFFFF 0 = 8kB 0xDE000 - 0xDFFFF

Note:

The default value for DiskOnChip™ is 8 kB.

This page was intentionally left blank.

Chapter 3

Installation

This page was intentionally left blank.

3. Installation

3.1 Board Installation

Caution!

If your board type is not specifically qualified as hotswap capable, please switch off the CompactPCI system before installing the board in a free CompactPCI slot. Failure to do so could endanger your life/health and may damage your board or system.

Note:

Certain CompactPCI boards require bus master and/or rear I/O capability. If you are in doubt whether such features are required for the board you intend to install, please check your specific board and/or system documentation to make sure your system is provided with an appropriate free slot to insert the board.

ESD Equipment!

Your CompactPCI board contains electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:

- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector-pins or traces.
- If working at an anti-static workbench with professional discharging equipment, please do not omit to use it.

Chapters 2 and chapter 4 of this manual describe the hardware and software setup of the CP603 controller board, its CPU and the following related devices:

- serial ports COM1 and COM2
- floppy disk interface
- one IDE Hard Disk interface
- keyboard/mouse interface on the front panel
- VGA
- USB
- Fast Ethernet
- SCSI interface

PEP Advantage

One or more of the above mentioned mass storage and I/O devices may be connected to your CP603 controller board. However, none of these devices have to be installed for the CP603 to function, as it is designed to be bootstrapped solely from the FLASH device.

3.1.1 Placement of the CP603

The *PEP* CompactPCI system configuration is characterized by the fact that its system slot (slot “1”) is on the right end of the backplane, thus allowing for physical CPU growth (heat-sink, cooling fan etc.) associated with higher-performance processors.

Important!

After having inserted your controller board, please make sure it has been fitted into the system slot.

3.1.2 IDE Interfaces

The CP603 baseboard is provided with two IDE interfaces, IDE1 and IDE2.

The interface allows installation of up to four hard disks (two master-slave pairs). If installed, the hard disks are automatically recognized by the BIOS at system “power on”.

Important!

The IDE1 and IDE2 interfaces support a maximum of four hard disks (two master-slave pairs) connected in the master-slave mode. For details about how to configure the hard disks as either masters or slaves please refer to the hard disk manufacturer’s documentation.

Hard-Disk Installation

To install a hard disk, it is necessary to perform the following operations in the given order:

1. Install the hardware;
2. Initialize the software necessary to run the chosen operating system.

Attention!

The incorrect connection of power or data cables can damage your hard disk unit and/or CP603 board.

3.1.3 Keyboard/Mouse Connector

The CP603 uses a PC/AT standard keyboard/mouse connection realized as a 6-pin shielded mini-DIN connector. To connect both a mouse and keyboard to your mini-DIN connector, a suitable keyboard/mouse Y-adapter may be used

Attention

When plugging in your keyboard and mouse, or when plugging anything into a Serial or Com port, make sure that the power is off. Connecting these devices while the power is on, which is known as “hot plugging”, may damage your system.

3.2 Rear I/O Installation

Note:

- To ensure proper functioning of the Rear I/O serial interfaces, the driver for the COM1 port must be disabled per software and the driver for the COM2 port must be disabled per solder jumper on the Transition VGA-module
- To ensure functioning of the Rear I/O VGA interface, the solder jumpers on the Transition VGA-module CP602-VGA1 must be configured for the Rear I/O.

3.3 Software Installation

The installation of all onboard peripheral drivers is described in detail in the relevant Driver Kit files.

This page was intentionally left blank.

Chapter 4

CMOS Setup

This page was intentionally left blank.

4. CMOS Setup

This chapter describes the Award BIOS Setup program, EliteBIOS, version 4.51PG. The Setup program lets you modify basic system configuration settings.

4.1 Proprietary Notice

Unless otherwise noted, chapter 4 of this manual, which concerns the EliteBIOS setup program, as well as the information herein disclosed are proprietary to AWARD Software International, Inc. Any person or entity to whom this document is furnished or who otherwise has possession thereof, by acceptance agrees that it will not be copied or reproduced in whole or in part, nor used in any manner except to meet the purposes for which it was delivered.

The information presented in this chapter is subject to change without notice, and should not be considered as a commitment by Award. Although Award will make every effort to inform users of substantive errors, Award disclaims all liability for any loss or damage resulting from the use of this document or any hardware or software described herein, including without limitation contingent, special, or incidental liability.

4.2 Introduction to Setup

This manual describes the Award BIOS Setup program. The Setup program lets you modify basic system configuration settings. The settings are then stored in a dedicated battery-backed memory, called CMOS RAM, that retains the information when the power is turned off.

A special feature of *PEP's* CompactPCI boards is that all Setup information is additionally saved in a non-volatile serial EEPROM. This feature provides the user with enhanced data security in comparison with a standard PC board, because setup data will not be lost should the battery fail.

The Award BIOS in your computer is a customized version of an industry-standard BIOS for IBM PC AT–compatible personal computers. It supports the Intel®x86 and compatible processors. The BIOS provides critical low-level support for the system central processing, memory, and I/O subsystems.

The Award BIOS has been customized by adding important, but nonstandard, features such as virus and password protection, power management, and detailed fine-tuning of the chipset controlling the system.

The rest of this manual is intended to guide you through the process of configuring your system using Setup.

Starting Setup

The Award BIOS is immediately activated when you first turn on the computer. The BIOS reads system configuration information in CMOS RAM and begins the process of checking out the system and configuring it through the Power-on Self Test (POST).

When these preliminaries are finished, the BIOS seeks an operating system on one of the data storage devices (hard drive, floppy drive, etc.). The BIOS launches the operating system and hands control of system operations to it.

During POST, you can start the Setup program in one of two ways:

- By pressing <Del> immediately after switching the system on, or
- By pressing the <Del> key or by simultaneously pressing <CTRL>, <ALT>, and <ESC> keys when the following message appears briefly at the bottom of the screen during POST:

Press DEL to enter SETUP

If the message disappears before you respond and you still wish to enter Setup, restart the system to try again by turning it OFF then ON or pressing the RESET button on the system case. You may also restart by simultaneously pressing <CTRL>, <ALT>, and <Delete> keys. If you do not press the keys at the correct time and the system does not boot, an error message appears and you are again asked to

Press F1 to continue, DEL to enter SETUP

Setup Keys

The following table describes how to navigate in Setup using the keyboard.

Table 4-1: Keyboard Commands

Up Arrow	Move to previous item
Down Arrow	Move to next item
Left Arrow	Move to the item to the left
Right Arrow	Move to the item to the right
Esc Key	Main Menu: Quit without saving changes into CMOS RAM. Status Page Setup Menu and Option Page Setup Menu: Exit current page and return to Main Menu
PgUp Key	Increase the numeric value or make changes
PgDn Key	Decrease the numeric value or make changes
+ Key	Increase the numeric value or make changes
- Key	Decrease the numeric value or make changes
F1 Key	General help, only for Status Page Setup Menu and Option Page Setup Menu
F2 Key **Shift-F2**	Change color from total of 16 colors. F2 to select color forward, Shift-F2 to select color backward
F3 Key	Calendar, only for Status Page Setup Menu
F4 Key	Reserved
F5 Key	Restore the previous CMOS value from CMOS, only for Option Page Setup Menu
F6 Key	Load the default CMOS RAM value from BIOS default table, only for Option Page Setup Menu
F7 Key	Load the default
F8 Key	Reserved
F9 Key	Reserved
F10 Key	Save all the CMOS changes, only for Main Menu

Getting Help

Press F1 and a small help window pops up that describes the appropriate keys to use and the possible selections for the highlighted item. To exit the Help Window press <Esc> or the F1 key again.

In Case of Problems

If, after making and saving system changes with Setup, you discover that your computer is no longer able to boot, the Award BIOS supports an override to the CMOS settings that resets your system to its default configuration.

You can invoke this override by immediately pressing <Insert> when you restart your computer. You can restart by either using the ON/OFF switch, the RESET button or by pressing <CTRL>, <ALT> and <Delete> at the same time.

The best advice is to only alter settings that you thoroughly understand. In particular, do not change settings in the Chipset screen without good reason. The Chipset defaults have been carefully chosen by *PEP Modular Computers* for optimum performance and reliability. Even a seemingly small change to the Chipset setup may result in the system becoming unstable.

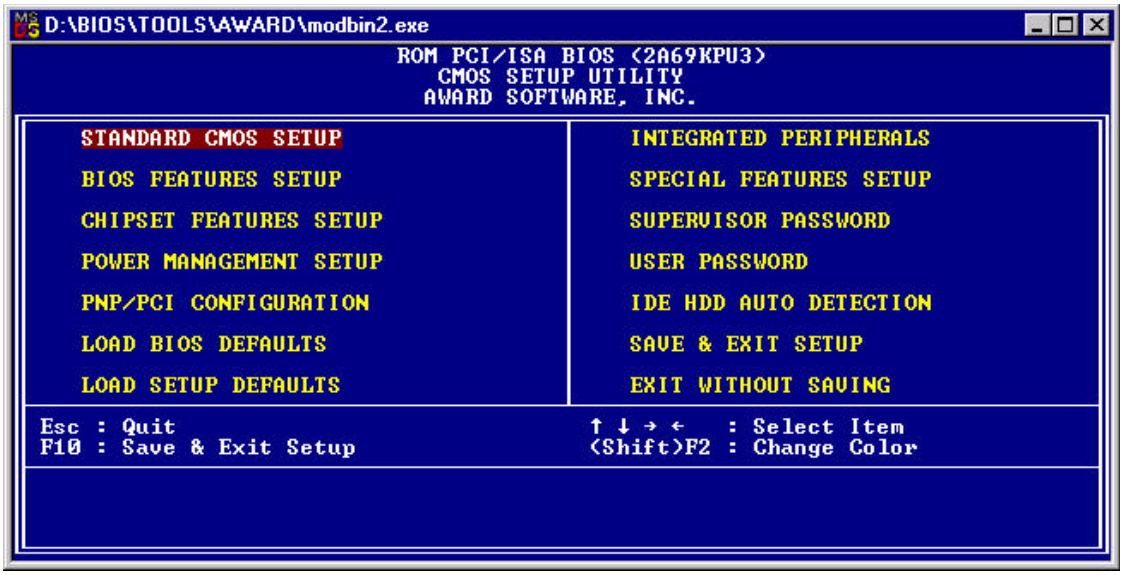
Setup Variations

Not all systems have the same Setup. While the basic look and function of the Setup program remains the same for all systems, the appearance of your Setup screens may differ from the screens shown here. Each system design and chipset combination require customized configurations. In addition, the final appearance of the Setup program depends on your system designer. Your system designer may decide that certain items should not be available for user configuration and remove them from the Setup program.

4.3 Main Setup Menu

When you enter the Award BIOS CMOS Setup Utility, a Main Menu, similar to the one shown below, appears on the screen. The Main Menu allows you to select from several Setup functions and two exit choices. Use the arrow keys to select items and press ↵ to accept and enter the sub-menu.

Figure 4-1: CMOS Setup Utility Main Menu — Screen Display



A brief description of each highlighted selection appears at the bottom of the screen.

Following is a brief summary of each Setup category.

Standard CMOS Setup

Options in the original PC AT-compatible BIOS.

BIOS Features Setup

Award enhanced BIOS options.

Chipset Features Setup

Options specific to your system chipset.

Power Management Setup

Advanced Power Management (APM) options.

PNP/PCI Configuration

PlugandPlay standard and PCI Local Bus configuration options.

Integrated Peripherals

I/O subsystems, that depend on the integrated peripherals controller in your system.

Special Features Setup

Items related to features of this board, which are not common to standard motherboard designs.

Supervisor/User Password

Change, set, or disable a password. In BIOS versions that allow separate user and supervisor passwords, only the supervisor password permits access to Setup. The user password generally allows only power-on access.

IDE HDD Auto Detection

Automatically detect and configure IDE hard disk parameters.

Load BIOS Defaults

BIOS defaults are factory settings for the most stable, minimal-performance system operations.

Load Setup Defaults

Setup defaults are factory settings for optimal-performance system operations.

Save & Exit Setup

Save settings in non-volatile CMOS RAM and exit Setup.

Exit Without Save

Abandon all changes and exit Setup.

4.4 Standard CMOS Setup

In the Standard CMOS menu you can set the system clock and calendar, record disk drive parameters and the video subsystem type, and select the type of errors that stop the BIOS POST.

Date

The BIOS determines the day of the week from the other date information. This field is for information only.

Press the → or ← key to move to the desired field (date, month, year). Press the “PgUp” or “PgDn” key to increment the setting, or type the desired value into the field.

Time

The time format is based on the 24-hour military-time clock. For example, 1 p.m. is 13:00:00. Press the → or ← key to move to the desired field. Press the PgUp or PgDn key to increment the setting, or type the desired value into the field.

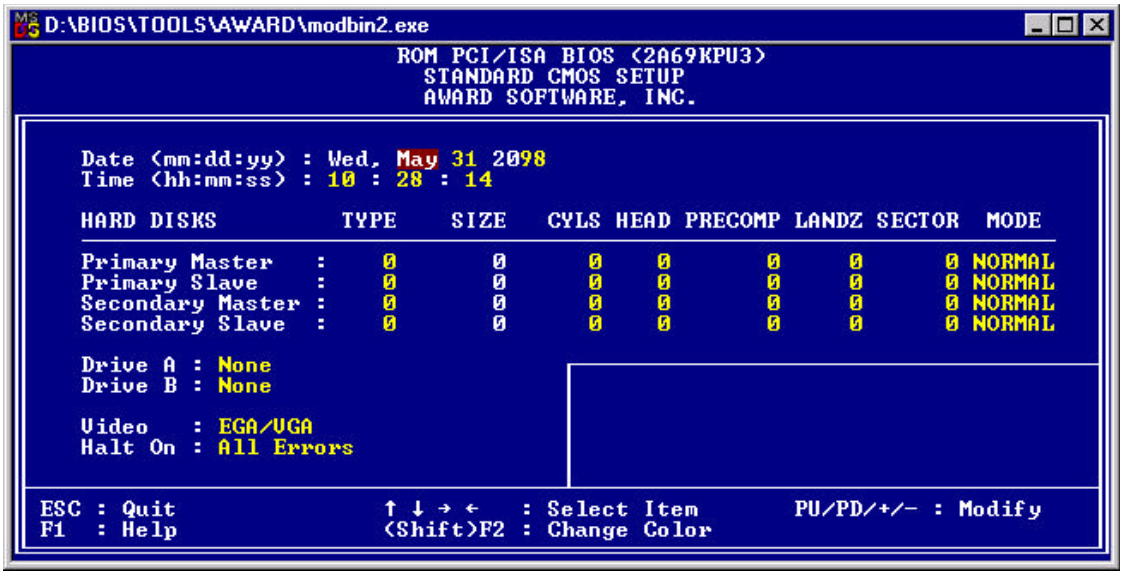
Hard Disks

The BIOS supports up to four IDE drives. This section does not show information relating to other IDE devices, such as a CD-ROM drive, or about other hard drive types, such as SCSI drives.

Important!

We recommend that you select the AUTO type for all drives.

Figure 4-2: Standard CMOS Setup Menu — Screen Display



The BIOS has the capability to automatically detect the specifications and optimal operating mode of almost all IDE hard drives. When you select type AUTO for a hard drive, the BIOS detects its specifications during POST, every time the system boots.

If you do not want to select drive type AUTO, other methods of selecting the drive type are available as follows:

1. Match the specifications of your installed IDE hard drive(s) with the pre-programmed values for drive types 1 through 45.
2. Select USER and enter values into each drive parameter field.
3. Use the IDE HDD AUTO DECTECTION function in “Setup”.

The following table provides a brief explanation of drive specifications:

Table 4-2: Description of Drive Specifications

Spec.		Description
Type		The BIOS contains a table of pre-defined drive types. Each defined drive type has a specified number of cylinders, number of heads, write pre-compensation factor, landing zone, and number of sectors. Drives whose specifications do not accommodate any pre-defined type are classified as type USER.
Size		Disk drive capacity (approximate). Note that this size is usually slightly greater than the size of a formatted disk given by a disk-checking program.
Cyls.		Number of cylinders
Head		Number of heads
Precomp.		Write pre-compensation cylinder
Landz		Landing zone
Sector		Number of sectors
Mode	Auto	Auto: The BIOS automatically determines the optimal mode.
	Normal	The maximum number of cylinders, heads, and sectors supported are 1024, 16, and 63 respectively.
	Large	For drives that do not support LBA and have more than 1024 cylinders.
	LBA	During drive accesses, the IDE controller transforms the data address described by sector, head, and cylinder number into a physical block address, significantly improving data transfer rates. For drives with greater than 1024 cylinders.

Drive A / Drive B

Selects the correct specifications for the diskette drive(s) installed in the computer.

Table 4-3: Diskette Drives

None	No diskette drive installed
360K, 5.25 in	5-1/4 inch PC-type standard drive; 360 kilobyte capacity
1.2M, 5.25 in	5-1/4 inch AT-type high-density drive; 1.2 megabyte capacity
720K, 3.5 in	3-1/2 inch double-sided drive; 720 kilobyte capacity
1.44M, 3.5 in	3-1/2 inch double-sided drive; 1.44 megabyte capacity
2.88M, 3.5 in	3-1/2 inch double-sided drive; 2.88 megabyte capacity

Video

Selects the type of primary video subsystem in your computer. The BIOS usually detects the correct video type automatically. The BIOS supports a secondary video subsystem, however, this is not selected in Setup.

Table 4-4: Primary Video Subsystem Selection

EGA/VGA	Enhanced Graphics Adapter/Video Graphics Array. For EGA, VGA, SEGA, SVGA or PGA monitor adapters.
CGA 40	Color Graphics Adapter, power-up in 40 column mode
CGA 80	Color Graphics Adapter, power-up in 80 column mode
MONO	Monochrome adapter, includes high resolution monochrome adapters

Halt On

During the power-on self-test (POST), the computer stops if the BIOS detects a hardware error. You can program the BIOS to ignore certain errors during POST and continue the boot-up process. The possible selections are listed in the following table.

Table 4-5: POST Specific Commands

Command	POST Action
No errors	POST does not stop for any errors.
All errors	If the BIOS detects any non-fatal error, POST stops and prompts you to take corrective action.
All, But Keyboard	POST does not stop for a keyboard error, but stops for all other errors.
All, But Diskette	POST does not stop for diskette drive errors, but stops for all other errors.
All, But Disk/Key	POST does not stop for a keyboard or disk error, but stops for all other errors.

Memory

You cannot change any values in the Memory fields; they are only for your information. The fields show the total installed random access memory (RAM) and amounts allocated to base memory, extended memory, and other (high) memory. RAM is counted in kilobytes (KB: approximately one thousand bytes) and megabytes (MB: approximately one million bytes).

RAM is the computer's working memory, where the computer stores programs and data currently being used, so they are accessible to the CPU. Modern personal computers may contain up to 64 MB, 128 MB, or more.

Base Memory

Typically 640 KB. Also called conventional memory. The DOS operating system and conventional applications use this area.

Extended Memory

Above the 1 MB boundary. Early IBM personal computers could not use memory above 1 MB, but current PCs and their software can use extended memory.

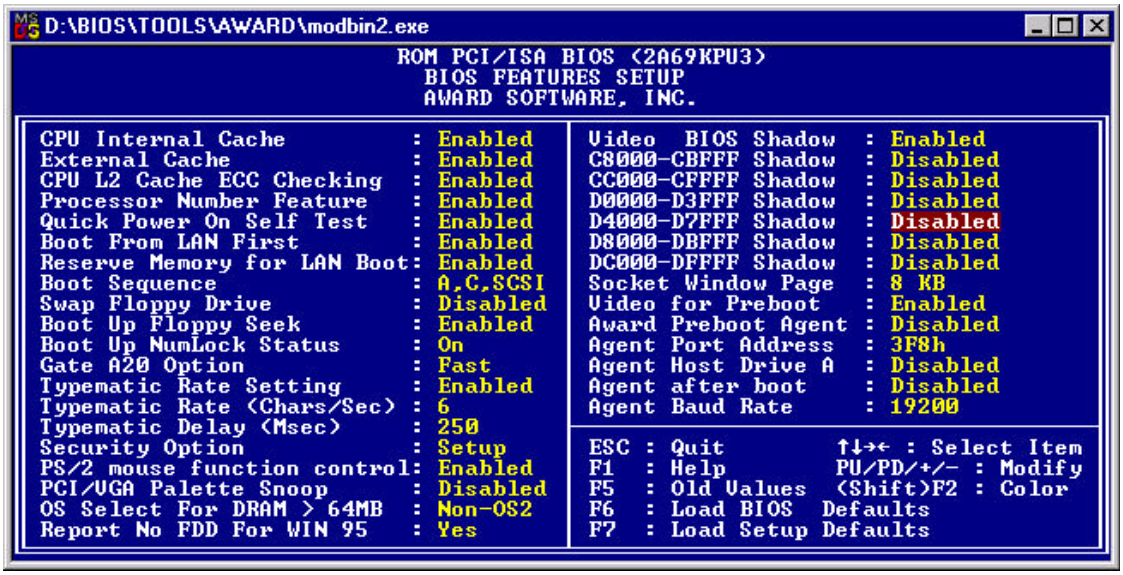
Other Memory

Between 640 KB and 1 MB; often called High Memory. DOS may load terminate-and-stay-resident (TSR) programs, such as device drivers, in this area, to free as much conventional memory as possible for applications. Lines in your CONFIG.SYS file that start with LOADHIGH load programs into high memory.

4.5 BIOS Features Setup

This screen contains industry-standard options additional to the core PC AT BIOS. This section describes all fields presented by Award Software in this screen. The example screen below may vary somewhat from the one in your Setup program; your system board designer may omit or modify some fields

Figure 4-3: BIOS Features Setup — Screen Display



CPU Internal Cache / External Cache

Cache memory is additional memory that is much faster than conventional DRAM (system memory). CPU's from 486-type on up contain internal cache memory, and most, but not all, modern PC's have additional (external) cache memory. When the CPU requests data, the system transfers the requested data from the main DRAM into cache memory, for even faster access by the CPU.

The External Cache field may not appear if your system does not have external cache memory.

CPU L2 Cache ECC Checking

When you select *Enabled*, memory checking is enabled when the external cache contains ECC SRAM's.

Quick Power-on Self Test

Select Enabled to reduce the amount of time required to run the power-on self-test (POST). A quick POST skips certain steps. We recommend that you normally disable quick POST. Better to find a problem during POST than lose data during your work.

Boot from LAN first

If your BIOS if capable of Booting from LAN via DHCP/BOOTP – protocol (option), you can switch this option on/off here.

Boot Sequence

The original IBM PC's loaded the operating system from drive A (floppy disk), so IBM PC-compatible systems are designed to search for an operating system first on drive A, and then on drive C (hard disk). However, modern computers usually load the operating system from the hard drive, and may even load it from a CD-ROM drive. The BIOS now offers 10 different boot sequence options of three drives each. In addition to the traditional drives A and C, options include IDE hard drives D, E and F; plus an SCSI hard drive and a CD -ROM drive.

Swap Floppy Drive

This field is effective only in systems with two floppy drives. Selecting Enabled assigns physical drive B to logical drive A, and physical drive A to logical drive B.

Boot Up Floppy Seek

When Enabled, the BIOS tests (seeks) floppy drives to determine whether they have 40 or 80 tracks. Only 360-KB floppy drives have 40 tracks; drives with 720 KB, 1.2 MB, and 1.44 MB capacity all have 80 tracks. Because very few modern PC's have 40-track floppy drives, we recommend that you set this field to Disabled to save time.

Boot Up Numlock Status

Toggle between On or Off to control the state of the NumLock key when the system boots. When toggled On, the numeric keypad generates numbers instead of controlling cursor operations.

Boot Up System Speed

Select High to boot at the default CPU speed; select Low to boot at the speed of the AT bus. Some add-in peripherals or old software (such as old games) may require a slow CPU speed. The default setting is High.

Gate A20 Option

Gate A20 refers to the way the system addresses memory above 1 MB (extended memory). When set to Fast, the system chipset controls Gate A20. When set to Normal, a pin in the keyboard controller controls Gate A20. Setting Gate A20 to Fast improves system speed, particularly with OS/2 and Windows.

Typematic Rate Setting

When Disabled, the following two items (Typematic Rate and Typematic Delay) are irrelevant. Keystrokes repeat at a rate determined by the keyboard controller in your system.

When Enabled, you can select a typematic rate and typematic delay.

Typematic Rate (Chars/Sec)

When the typematic rate setting is enabled, you can select a typematic rate (the rate at which a character repeats when you hold down a key) of 6, 8, 10, 12, 15, 20, 24 or 30 characters per second.

Typematic Delay (ms)

When the typematic rate setting is enabled, you can select a typematic delay (the delay before key strokes begin to repeat) of 250, 500, 750 or 1000 milliseconds.

Security Option

If you have set a password, select whether the password is required every time the System boots, or only when you enter Setup.

PS/2 Mouse Function Control

If your system has a PS/2 mouse port and you instal a serial pointing device, select *Disabled*.

PCI/VGA Palette Snoop

Your BIOS Setup may not contain this field. If the field is present, leave at Disabled.

OS Select for DRAM>64 MB

Select OS2 only if you are running the OS/2 operating system with greater than 64 MB of RAM in your system.

Report No FDD for WIN 95

Select *Yes* to release IRQ6 when the system contains no floppy drive, for compatibility with Windows 95 logo certification. In the **Integrated Peripherals** screen, select *Disabled* for the **Onboard FDC Controller** field.

Shadow

Software that resides in a read-only memory (ROM) chip on a device is called *firmware*. The Award BIOS permits *shadowing* of firmware such as the system BIOS, video BIOS, and similar operating instructions that come with some expansion peripherals, such as, for example, a SCSI adaptor.

Shadowing copies firmware from ROM into system RAM, where the CPU can read it through the 16-bit or 32-bit DRAM bus. Firmware not shadowed must be read by the system through the 8-bit X-bus. Shadowing improves the performance of the system BIOS and similar ROM firmware for expansion peripherals, but it also reduces the amount of high memory (640 KB to 1 MB) available for loading device drivers, etc.

Enable shadowing into each section of memory separately. Many system designers hardwire shadowing of the system BIOS and eliminate a System BIOS Shadow option.

Video BIOS shadows into memory area C0000-C7FFF. The remaining areas shown on the BIOS Features Setup screen may be occupied by other expansion card firmware. If an expansion peripheral in your system contains ROM-based firmware, you need to know the address range the ROM occupies to shadow it into the correct area of RAM.

Socket Window Page

The CP603 is equipped with a 32-pin socket to take additional Flash-ROM. This Flash-ROM may be addressed by a paging mechanism. The size of one Flash page can be set at this point as follows:

Table 4-6: Setting Flash Page Size

Page Size	Address Space used by Socket Flash EPROM
8 KB	0xDE000 - 0xDFFFF
32 KB	0xD8000 - 0xDFFFF
64 KB	0xD0000 - 0xDFFFF

Award Preboot Agent

Agent software may be enabled and disabled. The default is Disabled.

Agent Port Address

Select which UART address Agent software should use. Note to have set a UART in the INTEGRATED PERIPHERALS page to one of the below allowed settings. Recommended is 03F8h, which means COM1 (03F8h / IRQ 4); “auto” must not be selected.

The Agent system must have a serial (RS-232C) peripheral subsystem, to support a null modem (direct) connection.

If the Agent and host connect, but a session is not established, check the Agent COM port settings which should read as follows:

3F8h - IRQ4
2F8h - IRQ3
3E8h - IRQ4
2E8h - IRQ3

Agent Host Drive A

When the administrative host is using the Preboot Manager application, the Agent can boot and run applications from host floppy drive A. INT13 calls intended for the Agent floppy drive A are redirected by the Agent extension to the host floppy drive A. All other INT13 calls are passed along to the original interrupt handler. The Manager application can receive the Agent drive A interrupt and interpret the commands. It then calls its own INT13 handler to read or write the requested sectors to host drive A. Both Manager and Agent serial version software use Xmodem protocol for all transfers.

The floppy drive redirection feature permits support personnel to remotely administer two vital tools on the Agent system:

- PC DIAG diagnostics package from Unicore Software (available through Award Software as part of the Manager application).
- AWDFLASH BIOS flash upgrade utility. (in batch mode, this means giving the parameters at the command line; e.g. awdflash <filename> /Sn/Py, DO NOT USE INTERACTIVE MODE!!!)

Select Enabled to enable this feature, default is Disabled.

Agent after Boot

In the "standard" Agent product, Agent software continues to function after the operating system loads. However, some non-DOS operating systems are not compatible with the Agent BIOS extension, so the Agent should disable when the OS loads. Selecting Disabled turns off the Agent software just as the BIOS transfers control to the operating system. Default is Disabled.

Award Baud Rate

Select the speed at which the UART is to operate. Default is 19200. When using the Preboot Manager on the host, always select 19200 baud.

Null-Modem Cable Pinout

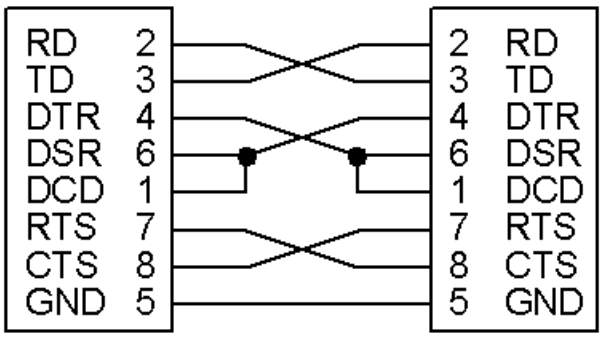


Figure 4-4: Null-Modem Cable Connection

A null-modem cable is a serial cable designed to connect two PC's. Each end has a 9-pin, female RS-232C connector. If you are creating your own 9-pin cable, connect the two ends through the cable as shown here.

Further Information

For further information please refer to the manual for the Award Preboot Agent™ 2.0 which accompanies the manual for the Award Preboot Manager™ 2.0.

4.6 Chipset Features Setup

This section describes features of the PIIX4 PCIset. If your system contains a different chipset, this section will bear little resemblance to what you see on your screen..

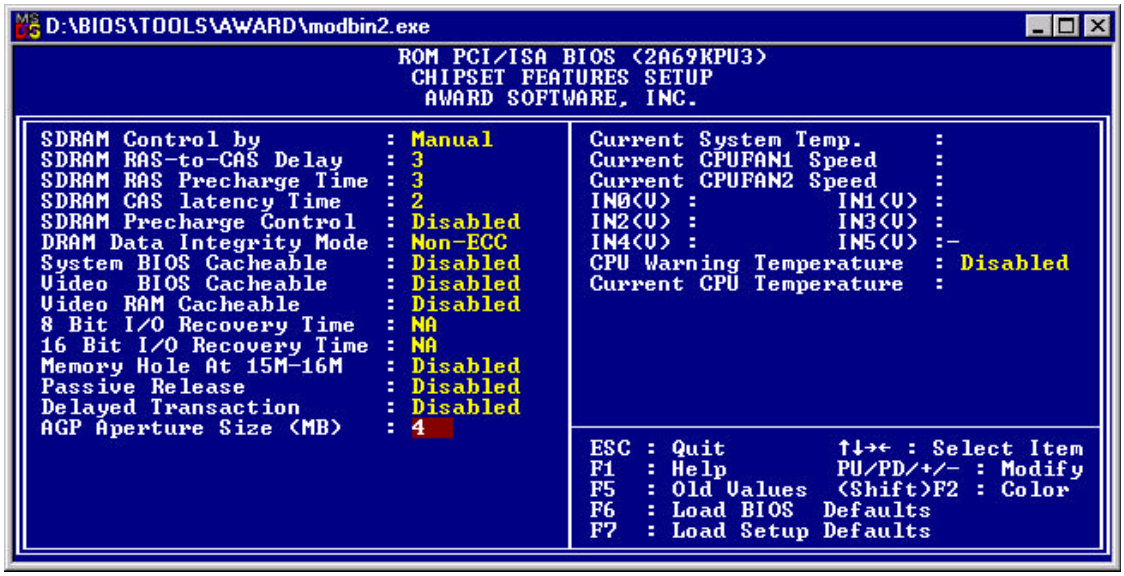
PEP Advantage

This section describes all the fields presented on this screen display. Please note that your system board designer may omit or modify some of the fields described in the following.

Advanced Options

The parameters in this screen are for system designers, service personnel, and technically competent users only. Do not reset these values unless you understand the consequences of your changes.

Figure 4-5: Chipset Features Setup — Screen Display



SDRAM Control by Manual / Auto

Auto Configuration selects predetermined optimal values for chipset parameters. When *Disabled*, chipset parameters revert to setup information stored in the CMOS. Many fields in this screen are not available when Auto Configuration is *Enabled*.

SDRAM RAS To CAS Delay

Select the RAS to CAS delay time. See Refresh Cycle Time for information about the Auto Configuration of this value.

SDRAM RAS Precharge Time

The precharge time is the number of cycles it takes for the RAS to accumulate its charge before DRAM refresh. If insufficient time is allowed, refresh may be incomplete and the DRAM may fail to retain data.

SDRAM CAS Latency Time

When synchronous DRAM is installed, you can control the number of CLK's between the SDRAM's sample of a read command and the time when the controller samples read data from the SDRAM's. Do not reset this field from the default value specified by the system designer.

SDRAM Precharge Control

When *Enabled*, all CPU cycles to SDRAM result in an All Banks Precharge Command on the SDRAM interface.

DRAM Data Integrity Mode

Select *Non-ECC* or *ECC* (error-correcting code), according to the type of installed DRAM.

System BIOS Cacheable

Selecting *Enabled* allows caching of the system BIOS ROM at 0xF0000 to 0xFFFFF, resulting in better system performance. However, if any program writes to this memory area, a memory access error may result.

Video BIOS Cacheable

Selecting *Enabled* allows caching of the video BIOS ROM at 0xC0000 to 0xC7FFF, resulting in better video performance. However, if any program writes to this memory area, a memory access error may result.

Video RAM Cacheable

Selecting *Enabled* allows caching of the video memory (RAM) at 0xA0000 to 0xAFFFF, resulting in better video performance. However, if any program writes to this memory area, a memory access error may result.

8/16-bit I/O Recovery Time

The I/O recovery mechanism adds bus clock cycles between PCI-originated I/O cycles to the ISA bus. This delay takes place because the PCI bus is so much faster than the ISA bus.

These two fields let you add recovery time (in bus clock cycles) for 16-bit and 8-bit I/O.

Memory Hole at 15M-16M

You can reserve this area of system memory for ISA adaptor ROM. When this area is reserved, it cannot be cached. The user information for peripherals that need to use this area of system memory usually discusses their memory requirements.

Passive Release

When *Enabled*, CPU to PCI bus accesses are allowed during passive release. Otherwise, the arbiter only accepts another PCI master access to local DRAM.

Delayed Transaction

The chipset has an embedded 32-bit posted write buffer to support delay transactions cycles. Select *Enabled* to support compliance with PCI specification version 2.1.

AGP Aperture Size (MB)

Select the size of the Accelerated Graphics Port (AGP) aperture. The aperture is a portion of the PCI memory address range dedicated for graphics memory address space. Host cycles that hit the aperture range are forwarded to the AGP without any translation. See http://www.agpforum.org for AGP information.

CPU Warning Temperature

Select the combination of lower and upper limits for CPU temperature, if your computer contains an environmental monitoring system. If the CPU temperature extends beyond either limit, any warning mechanism programmed into your application is activated.

Current CPU Temperature

This field displays the *current* CPU temperature, if your computer contains an environmental monitoring system.

Current CPU Fan 1

Monitors the onboard Fan mounted on the CPU heat sink, if available.

Current CPU Fan 2

Monitors the Fan signal routed to the rear I/O connector.

Voltage Monitor

Displays all onboard voltages for diagnostic purposes.

Shutdown Temperature

Select the combination of lower and upper limits for the system shutdown temperature, if your computer contains an environmental monitoring system. If the temperature extends beyond either limit, the system shuts down.

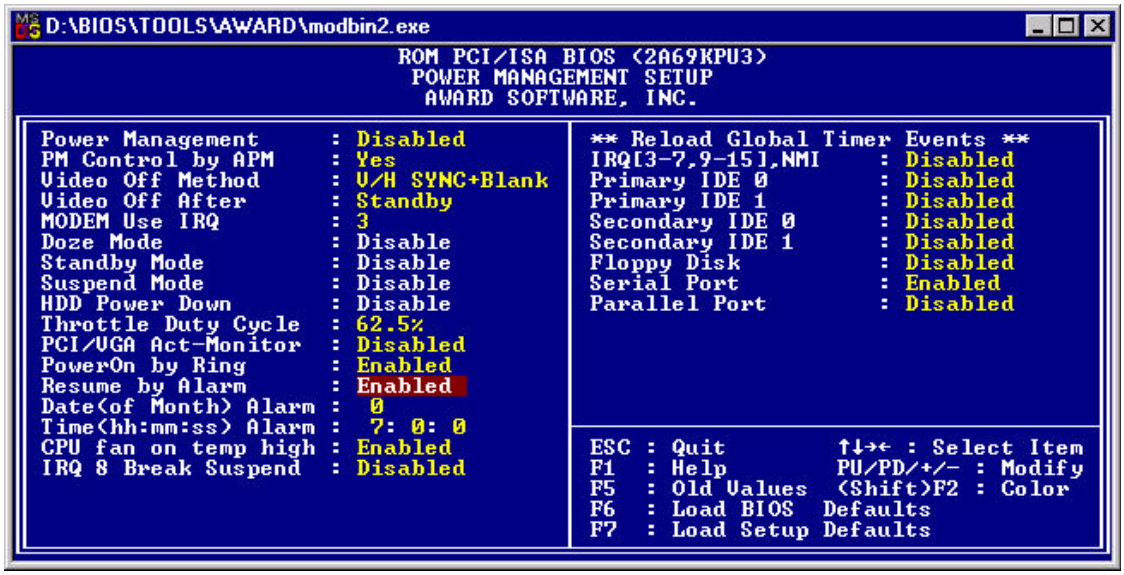
Field Shutdown Temperature: this does not exist for the CP603

4.7 Power Management

PEP Advantage

This section describes all fields presented on this screen display. Please note that your system board designer may omit or modify some of the fields described in the following.

Figure 4-6: Power Management Setup — Screen Display



ACPI Function

Select *Enabled* only if your computer's operating system supports the Advanced Configuration and Power Interface (ACPI) specification. Currently, Windows 98, Windows 2000 and Windows NT support ACPI.

Power Management

This option allows you to select the type (or degree) of power saving for Doze, Standby, and Suspend modes. See the section *PM Timers* for a brief description of each mode.

The following table describes each power management mode:

Table 4-7: Power Management Modes

Mode	Description
Max. Saving	Maximum power savings. **Only Available for SL CPU's**. Inactivity period is 1 minute in each mode.
User Defined	Sets each mode individually. Select time-out periods in the *PM Timers* section, which follows.
Min. Saving	Minimum power savings. Inactivity period is 1 hour in each mode (except the hard drive).

PM Control by APM

If Advanced Power Management (APM) is installed in your system, selecting *Yes* gives improved power savings.

Video-Off Method

Determines the manner in which the monitor is blanked.

Table 4-8: Video-Off Commands

V/H SYNC+Blank	System switches off vertical and horizontal synchronization ports and writes blanks to the video buffer.
DPMS Support	Select this option if your monitor supports the Display Power Management Signaling (DPMS) standard of the Video Electronics Standards Association (VESA). Use the software supplied for your video subsystem to select video power management values.
Blank Screen	System writes blanks only to the video buffer.

Video-Off Option

This item determines the power management modes the monitor will enter before entering the Off-state as defined by the Video Off Method below. The Video Off Option moves from the low (doze) to the medium (standby) to high (suspend) power saving modes.

Modem Use IRQ

Name the interrupt request (IRQ) line assigned to the modem (if any) on your system. Activity by the selected IRQ always awakens the system.

4.8 PM Timers

The following modes are Green PC power saving functions. They are user-configurable only during User Defined Power Management mode.

Doze Mode

After the selected period of system inactivity (1 minute to 1 hour), the CPU clock runs at a slower speed while all other devices still operate at full speed.

Stand-By Mode

After the selected period of system inactivity (1 minute to 1 hour), the fixed disk drive and the video shut down while all other devices still operate at full speed.

Suspend Mode

After the selected period of system inactivity (1 minute to 1 hour), all devices except the CPU shut down.

HDD Power Down

After the selected period of drive inactivity (1 to 15 minutes), the hard disk drive powers down while all other devices remain active.

Throttle Duty Cycle

When the system enters Doze mode, the CPU clock runs only part of the time. You may select the percentage of the time that the clock runs.

Soft-Off by PWR-BTTN

When you select *Instant Off* or *Delay 4 Sec*., turning the system off with the on/off button places the system in a very low power usage state, either immediately or after 4 seconds, with only enough circuitry receiving power to detect power button activity or Resume by Ring activity.

Power-on by Ring

When *Enabled*, an input signal on the serial Ring Indicator (RI) line (in other words, an incoming call on the modem) awakens the system from a soft off state.

Resume by Alarm

When *Enabled*, you can set the date and time at which the RTC (real-time clock) alarm awakens the system from suspend mode.

Date (of Month) Alarm

Select a date in the month when you want the alarm to go off.

Time (hh:mm:ss) Alarm

Set the time at which you want the alarm to go off.

IRQ8 Break (Event From) Suspend

You can select *Enabled* or *Disabled* for monitoring of IRQ8 (the Real Time Clock) so that it does not awaken the system from Suspend mode.

Reload Global Timer Events

When Enabled, an event occurring on each of the devices listed below restarts the global timer for Standby mode:

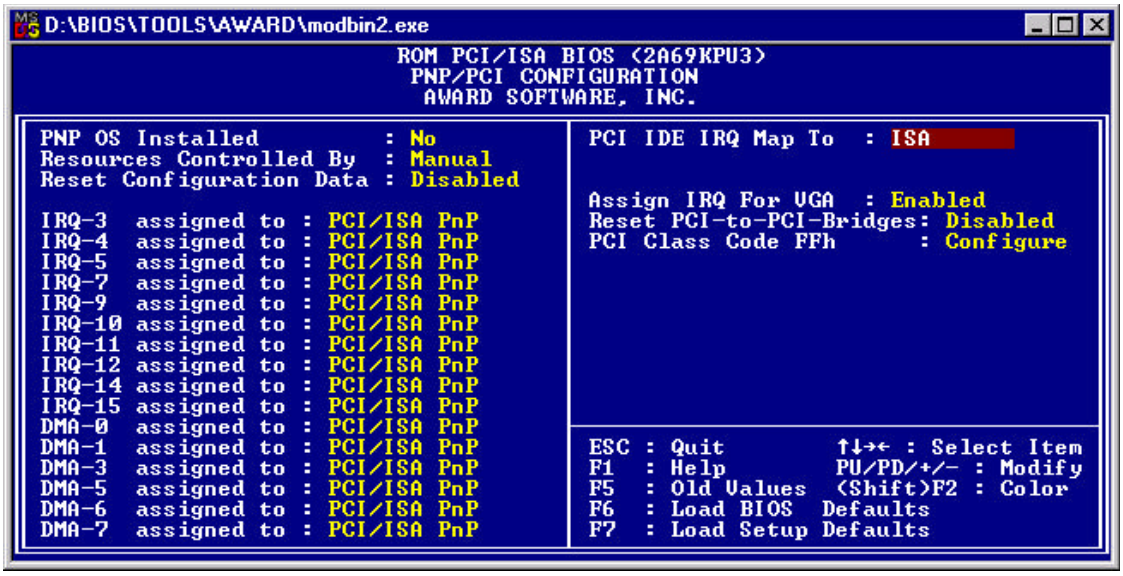
- IRQ§-7, 9-15, NM1,
- Primary IDE 0,
- Primary IDE 1,
- Secondary IDE 0,
- Secondary IDE 1,
- Floppy Disk,
- Serial Port,
- Parallel Port, and
- IRQ9 (IRQ2 Redir).

4.9 PNP/PCI Configuration

PEP Advantage

This section describes all the fields presented by this screen display. Please note that your system board designer may omit or modify some of the fields described in the following.

Figure 4-7: PNP/PCI Configuration — Screen Display



PNP OS Installed

Select “Yes” if the system operating environment is PlugandPlay aware (e.g. Win 95).

Resources Controlled by

The Award PlugandPlay BIOS can automatically configure all the boot and PlugandPlay-compatible devices. If you select *Auto*, all the interrupt request (IRQ) and DMA assignment fields disappear, as the BIOS automatically assigns them.

Reset Configuration Data

Normally this field is left *Disabled*. Select *Enabled* to reset Extended System Configuration Data (ESCD) when you exit Setup if you have installed a new add-on and the system re-configuration has caused such a serious conflict that the operating system cannot boot.

IRQ *n* Assigned to

When resources are controlled manually, assign each system interrupt as one of the following types, depending on the type of device using the interrupt.

Legacy ISA	Devices compliant with the original PC AT bus specification, requiring a specific interrupt (such as IRQ4 for serial port 1).
PCI/ISA PnP	Devices compliant with the PlugandPlay standard, whether designed for PCI or ISA bus architecture.

DMA *n* Assigned to

When resources are controlled manually, assign each system interrupt as one of the following types, depending on the type of device using the interrupt.

Legacy ISA	Devices compliant with the original PC AT bus specification, requiring a specific DMA channel
PCI/ISA PnP	Devices compliant with the PlugandPlay standard, whether designed for PCI or ISA bus architecture.

PCI IDE IRQ Map to

This field lets you select PCI IDE IRQ mapping or PC AT (ISA) interrupts. If your system does not have one or two PCI IDE connectors on the system board, select values according to the type of IDE interface(s) installed in your system (PCI or ISA). Standard ISA interrupts for IDE channels are IRQ14 for primary and IRQ15 for secondary.

Primary/Secondary IDE INT#

Each PCI peripheral connection is capable of activating up to four interrupts: *INT# A*, *INT# B*, *INT# C* and *INT# D*. By default, a PCI connection is assigned *INT# A*. Assigning *INT# B* has no meaning unless the peripheral device requires two interrupt services rather than just one. Because the PCI IDE interface in the chipset has two channels, it requires two interrupt services. The primary and secondary IDE INT# fields default to values appropriate for two PCI IDE channels, with the primary PCI IDE channel having a lower interrupt than the secondary.

Reset PCI-to-PCI Bridges

The BIOS may reset the PCI-to-PCI Bridges in the system using a software reset mechanism. Especially in conjunction with Hotswap compatible boards, it should be disabled. Default is disabled.

PCI Class Code FFh:

Some PCI boards generate a class code 0FFh. Although this code does not conform with the PCI standard, boards of this kind are distributed by some vendors.

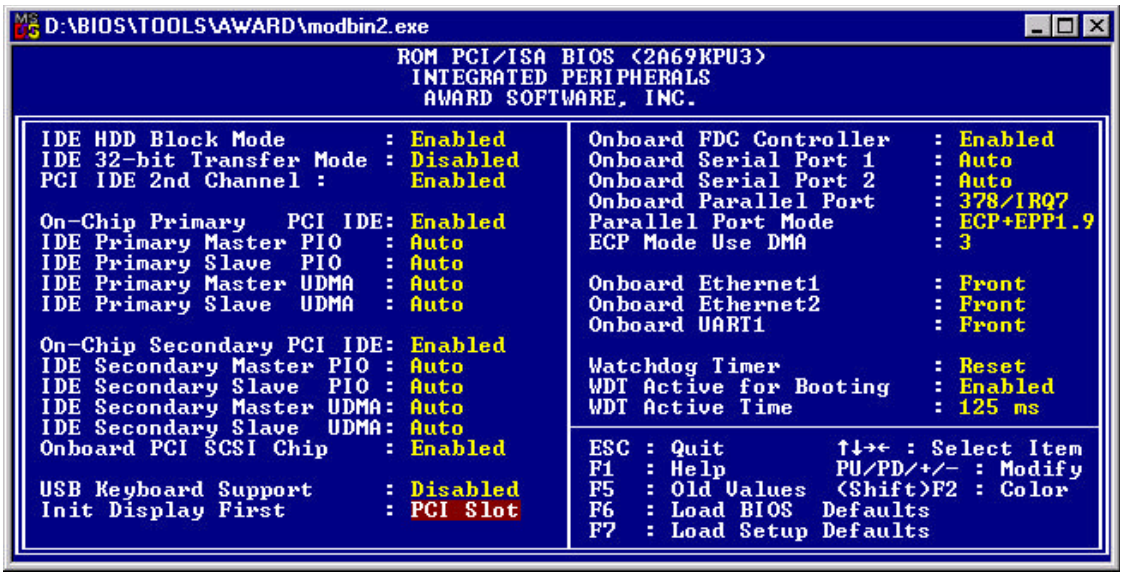
By setting this field to configure, these non-standard boards will be ignored
By setting this field to ignore, these non-standard boards will also be configured by the BIOS and made operable.

4.10 Integrated Peripherals

Important!

This section describes all the fields presented by Award Software in this screen display. Please note that your system board designer may omit or modify some fields.

Figure 4-8: Integrated Peripherals — Screen Display



PCI IDE 2nd Channel

Used to enable the 2nd PCI IDE interface

IDE HDD Block Mode

Select *Enabled* only if your hard drives support block mode.

IDE 32-bit Transfer Mode

Enables or disables 32-bit Data transfers.

On-Chip PCI IDE (Primary/Secondary)

The Intel® 82C440BX chipset contains a PCI IDE interface with support for two IDE channels. Select *Enabled* to activate the primary and/or secondary IDE interface. Select *Disabled* to deactivate this interface if you instal a primary and/or secondary add-in IDE interface.

IDE PIO Modes (Primary/Secondary Master/Slave)

The four IDE PIO (Programmed Input/Output) fields let you set a PIO mode (0-4) for each of up to four IDE devices that the internal PCI IDE interface supports. Modes 0 through 4 provide successively increased performance. In *Auto* mode, the system automatically determines the best mode for each device.

IDE Primary/Secondary Master/Slave UDMA

UDMA (Ultra DMA) is a DMA data transfer protocol that utilizes ATA commands and the ATA bus to allow DMA commands to transfer data at a maximum burst rate of 33 MB per second. When you select *Auto* in the four IDE UDMA fields (for each of up to four IDE devices that the internal PCI IDE interface supports), the system automatically determines the optimal data transfer rate for each IDE device.

Onboard PCI SCSI chip

Enables the onboard Symbios Logic Controller and BIOS expansion.

USB Keyboard Support

Select *Enabled* if your system contains a Universal Serial Bus (USB) controller and you have a USB keyboard.

Init Display First

Initialize the AGP video display before initializing any other display device on the system. Thus the AGP display becomes the primary display.

Onboard FDC Controller

Select *Enabled* if your system has a floppy disk controller (FDC) installed on the system board and you wish to use it. If you install an add-on FDC or the system has no floppy drive, select *Disabled* in this field.

Onboard Serial Ports: 1, 2

Select a logical COM port address and corresponding interrupt for the first and second serial ports.

Onboard Parallel Port

Select a logical LPT port address and corresponding interrupt for the physical parallel port.

Parallel Port Mode

Select an operating mode for the onboard parallel port. Select *Normal* unless you are certain that both your hardware and software support one of the other available modes.

ECP Mode Use DMA

Select a DMA channel for the parallel port for use during ECP mode.

Onboard Ethernet (1,2)

Select the physical connector to be used; Front or Rear I/O.

Onboard UART 1

The physical connector of the first serial port selects Front or Rear I/O.

Watchdog Timer

Select the watchdog routing.

WDT Active for Booting

Select *Enable* if the watchdog timer requires to be started before the operating system is booted from the BIOS.

WDT Active Time

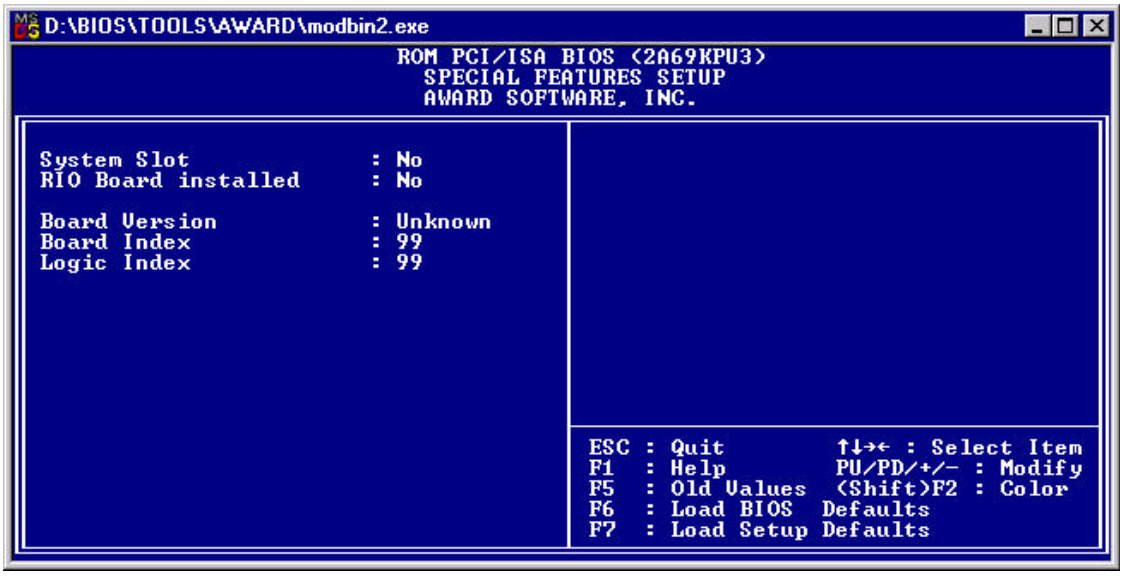
Select the time after which the action selected occurs, if the watchdog timer is not retriggered.

4.11 Special Setup Features

Important!

This section describes all the fields presented by Award Software in this screen display. Your system board designer may omit or modify some fields.

Figure 4-9: Special Features Setup — Screen Display



System Slot

This is a display only field. Yes indicates that this CPU is the system controller configuring the backplane and handling all interrupts relating to the backplane. No indicates that this CPU is a slave CPU.

Board Version

This is a display only field, which reflects the value of an onboard register. This must always correspond with the CPU on which the BIOS is installed.

Board Index

This is a display only field, which reflects the value of an onboard register. It shows the index of the hardware.

Logic Index

This is a display only field, which reflects the value of an onboard register. It shows the index of the onboard logic. When the Board Index is 00 this item is not displayed.

4.12 Password Setting

When you select this function, the following message appears at the center of the screen:

`Enter password:`

Type the password, up to eight characters in length, and press "↵". Typing a password clears any previously entered password from the CMOS memory.

After having pressed "↵" the message changes to:

`Confirm password:`

Type the password again and press "↵". To abort the process at any time, press "Esc".

In the "Security Option" item in the "BIOS Features Setup" screen, select `System` or `Setup`:

Table 4-9: Security Options

System	Enter a password each time the system boots and whenever you enter Setup.
Setup	Enter a password whenever you enter Setup.

Important!

To clear the password, simply press "↵" when asked to enter a password. Then the password function is disabled.

4.13 POST Messages

During the Power-on Self Test (POST), the BIOS displays a message whenever it detects a correctable error. Any error message is followed by this prompt:

```
Press “F1” to continue, “Ctrl-Alt-Esc” or “Del” to enter setup.
```

Following is a list of POST error messages for both the ISA and the EISA BIOS.

CMOS Battery Has Failed

The CMOS battery is no longer functional. It should be replaced.

CMOS Checksum Error

Checksum of CMOS is incorrect. This can indicate that the CMOS has become corrupted. This error may have been caused by a weak battery. Check the battery and replace it, if necessary.

Disk Boot Failure, Insert System Disk and Press Enter

No boot device was found. This could mean that either a boot drive was not detected or that the drive does not contain proper system boot files. Insert a system disk into Drive A: and press <Enter>. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also be sure the disk is formatted as a boot device. Then reboot the system.

Diskette Drives or Types Mismatch Error - Run Setup

Type of floppy-disk drive installed in the system is different from the CMOS definition. Run “Setup” to reconfigure the drive type correctly.

Display Switch is Set Incorrectly

Display switch on the motherboard can be set to either monochrome or color. This error message indicates that the switch has a setting other than that indicated in Setup. Determine which setting is correct, and then either turn off the system and change the jumper, or enter Setup and change the VIDEO selection.

Display Type Has Changed Since Last Boot

Since the last powering-down of the system, the display adapter has been changed. You must configure the system for the new display type.

EISA Configuration Checksum Error - Please Run EISA Configuration Utility

The EISA non-volatile RAM checksum is incorrect or cannot correctly read the EISA slot. This can indicate either the EISA non-volatile memory has become corrupted or the slot has been configured incorrectly. Ensure also that the card is installed firmly in the slot.

EISA Configuration Is Not Complete - Please Run EISA Configuration Utility

The slot configuration information stored in the EISA non-volatile memory is incomplete.

Note:

When either of the above EISA error messages appears, the system boots in ISA mode so that you can run the EISA Configuration Utility.

Error Encountered Initializing Hard-Drive

Hard drive cannot be initialized. Make sure that the adapter is installed correctly and that all cables are correctly and firmly attached. Ensure also that the correct hard drive type is selected in “Setup”.

Error Initializing Hard-Disk Controller

Cannot initialize controller. Make sure that the cord is correctly and firmly installed in the bus. Ensure also that the correct hard drive type is selected in Setup. Also check to see if any jumper needs to be set correctly on the hard drive.

Floppy-Disk Controller Error or No Controller Present

Cannot find or initialize the floppy drive controller. Make sure that the controller is installed correctly and firmly. If there are no floppy drives installed, ensure that the floppy-disk drive selection in “Setup” is set to `NONE`.

Invalid EISA Configuration - Please Run EISA Configuration Utility

The non-volatile memory containing EISA configuration information was programmed incorrectly or has become corrupted. Re-run EISA configuration utility to correctly program the memory.

Note:

When this error appears, the system boots in ISA mode so that you can run the EISA configuration utility.

Keyboard Error or No Keyboard Present

Cannot initialize the keyboard. Make sure that the keyboard is attached correctly and that no keys are being pressed during the boot process.

If you are deliberately configuring the system without a keyboard, set the “Error Halt” condition in “Setup” to `HALT ON ALL, BUT KEYBOARD`. This causes the BIOS to ignore the missing keyboard and continue the boot process.

Memory Address Error at ...

Indicates a memory address error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory chips.

Memory Parity Error at ...

Indicates a memory parity error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory chips.

Memory Size Has Changed Since Last Boot

Memory has been added or removed since the last boot. In EISA mode use the configuration utility to reconfigure the memory configuration. In ISA mode enter “Setup” and enter the new memory size into the memory fields.

Memory Verify Error at ...

Indicates an error verifying a value already written to memory. Use the location along with your system's memory map to locate the bad chip.

Offending Address not Found

This message is used in conjunction with the “I/O Channel Check” and “RAM Parity Error” messages whenever the segment that has caused the problem cannot be isolated.

Offending Segment

This message is used in conjunction with the “I/O Channel Check” and “RAM Parity Error” messages whenever the segment that has caused the problem has been isolated.

Press a Key to Reboot

This message appears at the bottom of the screen when an error occurs that requires you to reboot. Press any key to reboot the system.

Press “F1” to Disable NMI, “F2” to Reboot

When the BIOS detects a non-maskable interrupt condition during boot, you can disable the NMI and continue to boot, or you can reboot the system with the NMI enabled.

RAM Parity Error - Checking for Segment ...

Indicates a parity error in the random access memory.

Should Be Empty But EISA Board Found - Please Run EISA Configuration Utility

A valid board ID was found in a slot that was configured as having no board ID.

Note:

When this error appears, the system boots in ISA mode so that you can run the EISA configuration utility.

Should Have EISA Board but not Found - Please Run EISA Configuration Utility

The board installed is not responding to the ID request, or no board ID has been found in the indicated slot.

Note:

When this error appears, the system boots in ISA mode so that you can run the EISA configuration utility.

Slot not Empty

Indicates that a slot designated as empty by the EISA Configuration Utility actually contains a board.

Note:

When this error appears, the system boots in ISA mode so that you can run the EISA configuration utility.

System Halted, <CTRL-ALT-DEL> to Reboot ...

Indicates that the present boot attempt has been aborted and that the system must be rebooted. Press and hold down the “CTRL” and “ALT” keys and press “DEL”.

Wrong Board in Slot - Please Run EISA Configuration Utility

The board ID does not match the ID stored in the EISA non-volatile memory.

Note:

When this error appears, the system boots in ISA mode so that you can run the EISA configuration utility.

4.14 POST Codes

ISA and PCI POST codes are routed to port address 80H.

Table 4-10: Early POST Codes before System BIOS is Shadowed

POST Code	Action
Reset	RTC & KBC initialization
0CFh	Early CPU Detection
0C0h	Early Chipset initialization
0C1h	Memory presence test: detects memory modules and programs chipset accordingly
0C6h	L2 Cache sizing test
0C3h	Decompresses Bios
0C5h	Shadows Main Bios and jumps to POST

Table 4-11: Normal POST Codes after System BIOS is Shadowed

POST Code	Action
03h	Set 40h, 72h to 1234h if it was a warm boot
04h	Reserved
05h	SuperIO early programming Clear Screen Initializes KBC
06h	Tests whether F000-Segment read/writeable Detects flash type
07h	Tests CMOS access If supported: Test if overide key (Insert) pressed during reset
08h 0BEh	-- Programs chipset defaults
09h	Reads CPU ID Cache initialization if necessary If supported: Restores CMOS from flash backup if required
0Ah	Initializes interrupt vectors Copies CMOS to stack If supported: Checks for dual processor

Table continued on following page

Table 4-11: Normal POST Codes after System BIOS is Shadowed

POST Code	Action
0Bh	Detects Coprocessor Initializes Power Management chipset Updates CPU microcode if P6 CPU Reads existing ESCD Scans PCI devices and busses, assigns I/O and Memory to PCI devices Initializes Clock generator Initializes Hardware monitoring / temperature sensor
0Ch	Initializes keyboard buffer in BDA
0Dh 0BFh 0Dh	-- Program chipset Measures CPU core speed Initializes VGA video If VGA video not found: Checks for CGA If none found: Beepcode -..
0Eh	If CGA video found: Checks video memory If supported: Tries to init Award preboot agent If supported: Shows graphic logo, otherwise shows EPA logo If not full screen graphic logo, shows copyright message and CPU type and speed If ISA VGA video: Switches on ISA video ROM shadowing
0Fh	Tests DMA Channel 0
10h	Tests DMA Channel 1
11h	Tests DMA Page Registers
12h	--
13h	--
14h	Tests and init timer (8254)
15h	If not warm boot: tests MasterPIC mask register bits
16h	If not warm boot: tests SlavePIC mask register bits
17h	--
18h	Tests PIC’s by use of timer. Restores timer
19h	--
1Ah	--
1Bh	--
1Ch	--
1Dh	--
1Eh	--
30h	Measures total memory size

Table continued on following page

Table 4-11: Normal POST Codes after System BIOS is Shadowed

POST Code	Action
31h	Initialize USB Tests all memory above 1 MB, shows memory size
32h	Scans for ISA PnP devices, isolates and assigns CSN to ISA PnP devices Disables SuperIO COM/LPT ports Detects and records COM/LPT ports Programs Super IO according to setup and probably detected other COM/LPT ports Programs Audio system Initializes chipset IDE channels
33h	--
34h	--
35h	--
36h	--
37h	--
38h	--
39h	--
3Ah	--
3Bh	--
3Ch	Enables going to setup
3Dh	Installs PS/2 mouse if present If ACPI supported: checks for compressed ACPI table
3Eh	Attempts to enable L2 Cache
3Fh	--
40h	--
41h 0BFh	-- Programs chipset Chipset auto configuration if required SuperIO COM/LPT auto configuration if required Records system device nodes Assigns resources to ISA PnP devices Installs Floppy disk
42h	Installs IDE hard disk and ATAPI drives
43h	Checks and initializes COM/LPT ports
44h	--
45h	Initializes coprocessor
46h	--
47h	Saves boot sector buffer

Table continued on following page

Table 4-11: Normal POST Codes after System BIOS is Shadowed

POST Code	Action
48h	--
49h	--
4Ah	--
4Bh	--
4Ch	--
4Dh	--
4Eh	Checks for USB keyboard Displays previously detected POST errors. If any, checks for "Halt on" condition setting and if necessary, waits for keys "F1" or "Del".
4Fh	Checks for password entry if necessary
50h	Saves CMOS values in stack back to CMOS
51h	Switches all ISA PnP devices into "Wait For Key" state
52h	USB final initialization Decompresses embedded PCI Option ROM's Assigns IRQ's to PCI devices Programs onboard SCSI if present and activated If ACPI supported: Decompresses and installs ACPI table Checks for and runs non-video option ROM's Switches on ISA option ROM shadowing Fetches and runs embedded SCSI Option ROM's Fetches and runs embedded ISA Option ROM's Disables unused shadow areas Releases lower 32KB of E000 Segment
53h	--
54h	--
55h	--
56h	--
57h	--
58h	--
59h	--
5Ah	--
5Bh	--
5Ch	--
5Dh	--
5Eh	--
5Fh	--

Table continued on following page

Table 4-11: Normal POST Codes after System BIOS is Shadowed

POST Code	Action
60h	Prepares IDE/ATAPI/SCSI for boot
61h	Sets speed turbo/deturbo Final chipset initialization Final power management initialization Clears screen Shows system info
62h	Programs keyboard numlock/typerate
63h	Builds ESCD and saves ESCD in flash Checks for correct century in CMOS Setup timer tick in BDA Clears any pending keys in BDA Flushes cache Releases upper 32KB of E000 Segment if Award Preboot Agent not present and active
0FFh	Boot

Appendix A

Rear I/O Module CP-RIO6-02

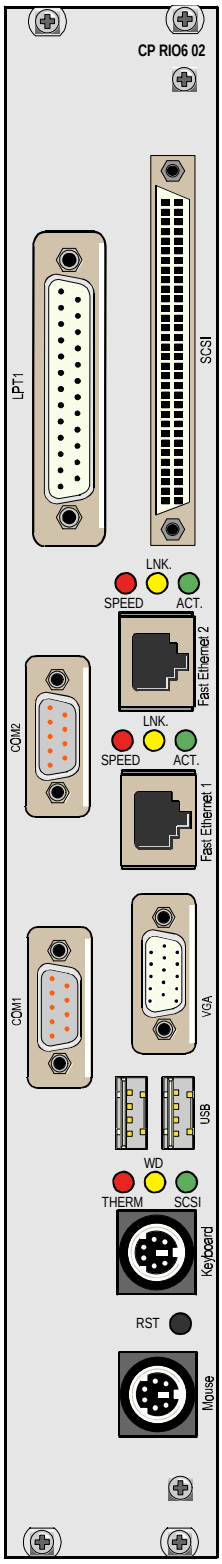
Rear I/O Module CP-RIO6-02

Rear I/O Module CP-RIO6-02

A Rear I/O Module CP-RIO6-02

A.1 CP-RIO6-02 Front Panel

Figure A-1: CP-RIO6-02 Front Panel



The front panel includes three LED's placed under the keyboard/mouse interface connector ("Board LED's") and three LED's placed over the two Ethernet connectors ("Ethernet LED's"). The functions of the LEDs are as follows:

Board LED's:

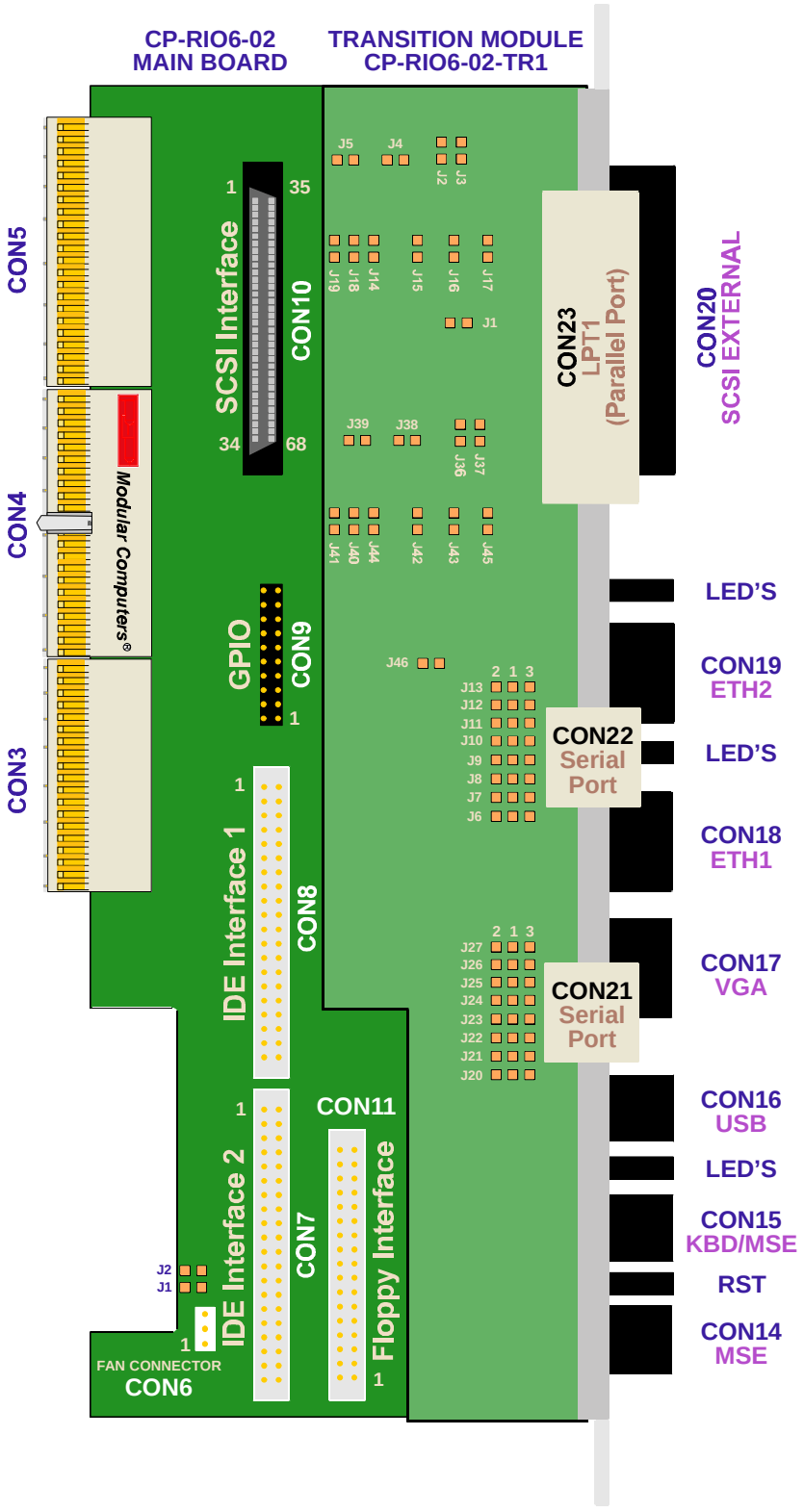
- "SCSI" (green) = if ON, The SCSI interface is active
- "WD" (yellow) = Watchdog timer status; if ON, the watchdog is active.
- "THERM" (red) = Temperature alarm; if ON, an overtemperature has occurred. To rectify, reduce the CPU clock speed.

Ethernet LED's (green):

- Left = Active; if ON, the Ethernet link is active.
- Middle = Link; if ON, transmission is in progress via the Ethernet link.
- Right = Speed; if ON transmission speed is 100 MBit/s.

A.2 CP-RIO6-02 Board Layout

Figure A-2: CP-RIO6-02 Module Board Layout



A.3 Introduction

Two different Rear I/O Modules may be used by the CP603 - the CP-RIO6-02 and the CP-RIO6-10 (which is the one used by the CP600 board family generally).

The CP-RIO6-02 provides comprehensive Rear I/O functionality. Everything that can be routed through the Front Panel can also be routed through this Rear I/O.

The CP-RIO6-10, described in a separate chapter in this manual, is the basic module which is suitable for applications which require Rear I/O functionality only for the principal interfaces.

A particular advantage of the Rear I/O capability is that there is no cabling on the CPU board which makes it much easier to remove the CPU in the rack.

A.4 Module Description

The CP-RIO6-02 is a Rear I/O module designed to be used with the 6U CPCI CPU board CP603 from *PEP Modular Computers*. The CP-RIO6-02 comprises a board plus an integral Transition Module, the RIO6-02-TR1. It is plugged in from the back of the system to the backplane P3, P4 and P5 connectors in line with the CPU board.

A.4.1 Dimensions

The dimensions of the 6U Rear I/O module CP-RIO6-02 are as follows:

233.35mm * 80mm (6U Rear I/O card size)

A.4.2 CP-RIO6-02 Front Panel (width 8HP) Interfaces

Interfaces located directly on the CP-RIO6-02, available via the Front Panel connectors

- one Ultra SCSI interface, 68pin female D-sub
- two Fast Ethernet Channels, each with 8pin RJ45 Modular Jack
- VGA interface, 15pin female High Density D-sub
- two USB ports, double USB connector
- PS/2 keyboard and/or mouse connector, 6-Pin MiniDIN
- PS/2 mouse connector, 6-Pin MiniDIN
- reset button

Interfaces located on the integral Transition Module RIO6-02-TR1, available via the Front Panel connectors.

- two serial interfaces COM1 and COM2, 9pin male D-sub
- one parallel port LPT1, 25pin female D-sub

A.4.3 CP-RIO6-02 Internal interfaces (Accessible via Onboard Connectors)

- CompactPCI specification 6U Rear I/O on J3, J4, J5
- Floppy Disk interface with a 34-pin connector
- 2 IDE interfaces (IDE1, IDE2) with 40-pin connectors
- one Ultra SCSI interface onboard, 68pin female plastic D-sub
- 20-pin connector for General Purpose I/O
- 3-pin fan connector
- 50-pin socket connector for adapting the transition module RIO6-02-TR1
- optional 10-pin serial interface COM2,

A.4.4 Other Features

- two triple LEDs indicating ACT, LNK, SPEED (one LED for each Ethernet channel)
- triple LED indicating the function of SCSI, Watchdog and Temperature Control
- Speaker onboard

Important!

- To ensure the proper functioning of the Rear I/O serial interfaces, the drivers for COM1 and COM2 on the CP603 and CP602-VGA1 must be disabled.
- To ensure functioning of the Rear I/O VGA interface, the solder jumpers on the graphics module CP602-VGA1 must be configured for Rear I/O.

A.5 CP-RIO6-02 Rear I/O Module Interfaces

A.5.1 Keyboard/Mouse Interfaces

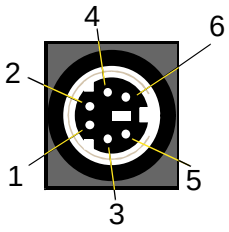


Figure A-3: Keyboard/Mouse Connectors

The PC/AT standard keyboard/mouse connector is a PS/2-type 6-pin shielded mini-DIN connector.

A.5.1.1 Keyboard/Mouse Connectors CON14 and CON15 Pinout

Table A-1: Keyboard/Mouse Connectors CON14 and CON15 Pinout

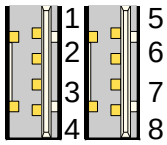
Pin	6-pin MiniDIN for Mouse CON 14	6-pin MiniDIN for Keyboard/Mouse CON 15
1	MDATA	KDATA
2	NC	MDATA
3	GND	GND
4	VCCPS2	VCCPS2
5	MCLK	KCLK
6	NC	MCLK

Note:

The keyboard/mouse power supply units are each protected by a 500 mA fuse. All signal lines are EMI-filtered.

A.5.2 USB Interfaces

Figure A-4: USB Connector CON16



There are two identical USB interfaces on the CP-RIO6-02 module each with a maximum transfer rate of 12 Mbit provided for connecting USB devices. One USB peripheral may be connected to each port. To connect more than two USB devices an external hub is required.

A.5.2.1 USB Connector CON16 Pinout

Table A-2: USB Connector CON16 Pinout

Pin	Name	Function	In/Out
1	VCC	VCC signal	--
2	UV0-	Differential USB-	--
3	UV0+	Differential USB+	--
4	GND	GND signal	--
5	VCC	VCC signal	--
6	UV0-	Differential USB-	--
7	UV0+	Differential USB+	--
8	GND	GND signal	--

Note:

The USB power supply feeding the two ports is protected by a 1.5 A fuse. All signal lines are EMI-filtered.

A.5.3 VGA Interface

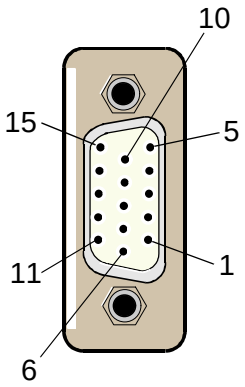


Figure A-5: D-sub VGA Connector CON17

A.5.3.1 VGA Connector CON17 Pinout

The 15-pin female connector CON17 is used to connect a VGA monitor to the CP-RIO6-02 Rear I/O board.

Table A-3: VGA connector CON17

D-sub 15	Signal	Function	In/Out
1	Red	Red video signal output	Out
2	Green	Green video signal output	Out
3	Blue	Blue video signal output	Out
13	Hsync	Horizontal sync.	TTL Out
14	Vsync	Vertical sync.	TTL Out
12	Sdata	I2C™ data	In/Out
15	Sclk	I2C™ clock	Out
9	VCC	Power +5V 200 mA no fuse protection	Out
5,6,7,8,10	GND	Signal ground	--
4,11	Free	--	--

Note:

To ensure functioning of the Rear I/O VGA interface, the solder jumpers on the graphics module CP602-VGA1 must be configured for Rear I/O.

A.5.4 Serial Port Interfaces

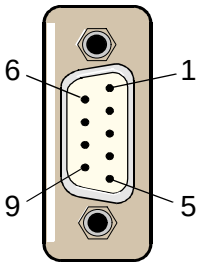


Figure A-6: PC-compatible D-Sub Serial Connectors CON21and CON22

Two PC-compatible serial 9-pin D-sub ports are available with 5V charge-pump technology eliminating the need for a +12V and -12V supply. The two COM ports, which are fully compatible with the 16550 controller, include a complete set of handshaking and modem control signals, maskable interrupt generation and data transfer of up to 460.8 kB/s.

The two COM interfaces may be configured as RS232, RS422 or RS485 ports by setting the appropriate solder jumpers. The standard setting of the two COM ports envisages the RS232 configuration.

RS-422 configuration:

The RS-422 interface use two differential data lines RX and TX for communication (Full-Duplex)

RS-485 configuration:

The RS-485 interface use one differential data line. It differs from the RS-422 modes in that it provides the ability to transmit and receive over the same wire. The RTS signal is used to control the direction of the RS-485 buffer.

The Serial Port connector pinouts appear on the next page

A.5.4.1 Serial Port Connectors CON21 and CON22 Pinout

The pinout of the 9-pin D-sub connectors depends on the configuration.

Table A-4: Serial Port Connectors CON21 and CON22 Pinout

Pin	RS232 (Standard PC)	RS422	RS485
1	DCD	+RXD	NC
2	RXD	+CTS	NC
3	TXD	+TXD	+TRXD
4	DTR	+RTS	NC
5	GND	GND	GND
6	DSR	-RXD	NC
7	RTS	-CTS	NC
8	CTS	-TXD	-TRXD
9	RIN	-RTS	NC

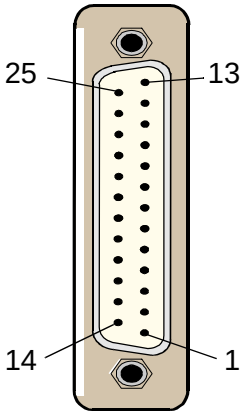
Note:

- The RS422 connector is *PEP*-specific and the signals DTR und DCD are not available.
- To ensure the proper functioning of the Rear I/O serial interfaces, the drivers for COM1 and COM2 on the CP603 and CP602-VGA1 must be disabled.

A.5.5 Parallel Port Interface

Figure A-7: PC-Compatible D-Sub Parallel Interface

The CP603 is provided with an IEEE1284, ECP/EPP-compatible parallel port/printer interface. The parallel port is a 25-pin D-sub female connector mounted on the front panel.



A.5.5.1 Parallel Port Connector CON23

The CP-RIO6-02 module is provided with a PC-compatible 25-pin D-sub connector CON23.

Table A-5: Parallel Port Connector CON23 Pinout

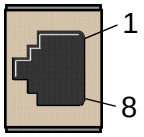
D-sub Pin	Signal	Description	Direction	D-sub Pin	Signal	Description	Direction
1	-STB	Strobe data	Out	14	-AFD	Auto feed	Out
2	PD0	LSB of printer data	Out	15	-ERR	Printer error	In
3	PD1	Printer data 1	Out	16	-INIT	Initialize printer	Out
4	PD2	Printer data 2	Out	17	-SLIN	Select printer	Out
5	PD3	Printer data 3	Out	18	GND	Signal ground	N/A
6	PD4	Printer data 4	Out	19	GND	Signal ground	N/A
7	PD5	Printer data 5	Out	20	GND	Signal ground	N/A
8	PD6	Printer data 6	Out	21	GND	Signal ground	N/A
9	PD7	Printer data 7	Out	22	GND	Signal ground	N/A
10	-ACK	Character accepted	In	23	GND	Signal ground	N/A
11	BSY	Busy	In	24	GND	Signal ground	N/A
12	PE	Paper end	In	25	GND	Signal ground	N/A
13	SLCT	Ready to receive	In	N/A	GND	Signal ground	N/C

A.5.6 Fast Ethernet Interfaces

The selection of Rear I/O or Front Panel Fast Ethernet Ports is made via the BIOS settings or via the Rear I/O Configuration Registers.

Figure A-8: Ethernet/Fast Ethernet Connectors

The Ethernet connector is realized as an RJ45 twisted-pair connector. The Interface provides automatic detection and switching between 10Base-T and 100Base-TX data transmission.



A.5.6.1 Fast Ethernet Connectors CON18 and CON19 Pinout

The CON18 and CON19 connectors provide the 10Base-TX/100Base-TX interface to the Ethernet controller. These connectors are enabled/disabled via the BIOS setting or the Rear I/O Configuration Register.

Table A-6: Fast Ethernet Connectors CON18 and CON19 Pinout

RJ45	Signal	Function
1	TX+	Transmit +
2	TX-	Transmit -
3	RX+	Receive +
4	NC	--
5	NC	--
6	RX-	Receive -
7	NC	--
8	NC	--

A.5.7 Ethernet LED Status

Yellow: Link: This LED monitors 10Base-T and 100Base-TX connections. The LED lights up to indicate a successful network connection. If this indicator is off, the cable connection may be faulty.

Green: Activity: This LED monitors network activity. The LED lights up when network packets are sent or received through the RJ45 port. When off, the computer is not sending or receiving network data.

Red: Speed: The LED lights up to indicate a successful 100Base-TX connection. While off the connection is operating at 10Base-T

A.5.8 Fan Control Interface

A fan for CPU cooling can be connected via the power connector CON6.

A.5.8.1 Fan Control Connector CON6 Pinout

Table A-7: Fan Control Connector CON6 Pinout

Pin	Function
1	Ground
2	Fan Supply Voltage
3	Fansense

A.5.9 IDE Connectors

A.5.9.1 IDE Connectors IDE1 (CON8) and IDE2 (CON7) Pinouts

The following table sets out the pin numbers of connectors CON8 and CON7 and details their corresponding signal names and functions.

Table A-8: Pinout of AT Standard Connectors IDE1 and IDE2

Pin	Signal	Function	In/Out
1	IDERESET	Reset HD	Out
2	GND	Ground signal	--
3	HD7	HD data 7	In/Out
4	HD8	HD data 8	In/Out
5	HD6	HD data 6	In/Out
6	HD9	HD data 9	In/Out
7	HD5	HD data 5	In/Out
8	HD10	HD data 10	In/Out
9	HD4	HD data 4	In/Out
10	HD11	HD data 11	In/Out
11	HD3	HD data 3	In/Out
12	HD12	HD data 12	In/Out

Table continued on following page

Table A-8: Pinout of AT Standard Connectors IDE1 and IDE2

Pin	Signal	Function	In/Out
13	HD2	HD data 2	In/Out
14	HD13	HD data 13	In/Out
15	HD1	HD data 1	In/Out
16	HD14	HD data 14	In/Out
17	HD0	HD data 0	In/Out
18	HD15	HD data 15	In/Out
19	GND	Ground signal	--
20	N/C	--	--
21	IDEDRQ	DMA request	In
22	GND	Ground signal	--
23	IOW	I/O write	Out
24	GND	Ground signal	--
25	IOR	I/O read	Out
26	GND	Ground signal	--
27	IOCHRDY	I/O channel ready	In
28	GND	Ground signal	--
29	IDEDACKA	DMA Ack	Out
30	GND	Ground signal	--
31	IDEIRQ	Interrupt request	In
32	N/C		--
33	A1	Address 1	Out
34	N/C	--	--
35	A0	Address 0	Out
36	A2	Address 2	Out
37	HCS0	HD select 0	Out
38	HCS1	HD select 1	Out
39	LED	LED driving	In
40	GND	Ground signal	--

A.5.10 Floppy Drive Interface

The CP-RIO6-02 is provided with a 2-row 34-pin male standard connector, CON11, realized as a connector which provides the signals for up to two floppy-drives.

Important!

If the floppy-disk drive connection cable is inverted (pin 1 in place of pin 34), at "power on", the floppy-disk drive will work uninterruptedly, with consequent risk of damage to the floppy-disk inserted.

A.5.10.1 Floppy Drive Connector CON11 Pinout

Table A-9: Floppy Drive Connector CON11 Pinout

Pin	Signal	Function	In/Out
2	RWC	Write precompensation	Out
4	N/C	--	--
6	N/C	--	--
8	INDEX	Index pulse	In
10	MOTEN1	Motor 1 enable	Out
12	DRVSEL2	Driver select 2	Out
14	DRVSEL1	Driver select 1	Out
16	MOTEN2	Motor 2 enable	Out
18	DIRECTION	Step direction	Out
20	STEP	Step pulse	Out
22	WRDATA	Write data	Out
24	WREN	Write enable	Out
26	TRACK0	Track 0 signal	In
28	WRPROT	Write protect	In
30	RDDATA	Read data	In
32	HEADSEL	Head select	Out
34	DSKCHG	Disk change	In
ODD NR.	GND	Ground signal	--

A.5.10.2 Floppy-Drive "A+B" Configuration

Important!

The floppy-drive connection cable is suitable for access by two PC-compatible floppy-disk drives. Make sure you plug the cable into the connector assigned to floppy-drive "A:". If it is plugged into the drive "B:" connector, no boot from the floppy drive is possible.

A.5.11 SCSI Interface Internal

Note:

The SCSI interface is identical to that on the CP603 baseboard. For a description and advisory notes, please refer to section 2.6.9 on page 2-22 in chapter 2, Functional Description and Configuration.

A.5.11.1 SCSI Connector Internal CON10 Pinout

Table A-10: SCSI Connector Internal CON10 Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	**18**	TERMPWR	**35**	-DB12	**52**	TERMPWR
2	GND	**19**	NC	**36**	-DB13	**53**	NC
3	GND	**20**	GND	**37**	-DB14	**54**	GND
4	GND	**21**	GND	**38**	-DB15	**55**	-ATN
5	GND	**22**	GND	**39**	-DB_P1	**56**	GND
6	GND	**23**	GND	**40**	-DB0	**57**	-BSY
7	GND	**24**	GND	**41**	-DB1	**58**	-ACK
8	GND	**25**	GND	**42**	-DB2	**59**	-RST
9	GND	**26**	GND	**43**	-DB3	**60**	-MSG
10	GND	**27**	GND	**44**	-DB4	**61**	-SEL
11	GND	**28**	GND	**45**	-DB5	**62**	-C/D
12	GND	**29**	GND	**46**	-DB6	**63**	-REQ
13	GND	**30**	GND	**47**	-DB7	**64**	-I/O
14	GND	**31**	GND	**48**	-DB_P	**65**	-DB8
15	GND	**32**	GND	**49**	GND	**66**	-DB9
16	GND	**33**	GND	**50**	DET_CON1	**67**	-DB10
17	TERMPWR	**34**	GND	**51**	TERMPWR	**68**	-DB11

A.5.12 SCSI Interface External

A.5.12.1 SCSI Connector External CON20 Pinout

Table A-11: SCSI Connector External CON20 Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	**18**	TERMPWR	**35**	-DB12	**52**	TERMPWR
2	GND	**19**	NC	**36**	-DB13	**53**	NC
3	GND	**20**	GND	**37**	-DB14	**54**	GND
4	GND	**21**	GND	**38**	-DB15	**55**	-ATN
5	GND	**22**	GND	**39**	-DB_P1	**56**	GND
6	GND	**23**	GND	**40**	-DB0	**57**	-BSY
7	GND	**24**	GND	**41**	-DB1	**58**	-ACK
8	GND	**25**	GND	**42**	-DB2	**59**	-RST
9	GND	**26**	GND	**43**	-DB3	**60**	-MSG
10	GND	**27**	GND	**44**	-DB4	**61**	-SEL
11	GND	**28**	GND	**45**	-DB5	**62**	-C/D
12	GND	**29**	GND	**46**	-DB6	**63**	-REQ
13	GND	**30**	GND	**47**	-DB7	**64**	-I/O
14	GND	**31**	GND	**48**	-DB_P	**65**	-DB8
15	GND	**32**	GND	**49**	GND	**66**	-DB9
16	GND	**33**	GND	**50**	DET_CON2	**67**	-DB10
17	TERMPWR	**34**	GND	**51**	TERMPWR	**68**	-DB11

A.5.13 Rear I/O CP-RIO6-02 CompactPCI Interface

A.5.13.1 Rear I/O CompactPCI Connectors CON3 (J3), CON4 (J4), CON5 (J5)

The CP-RIO6-02 is provided with three female Rear I/O connectors J3, J4 and J5. The same pinouts apply to the matching Rear I/O connectors P3, P4 and P5 of the CP603 baseboard. For convenience these tables are presented both here and in the "Functional Description and Configuration" chapter.

Table A-12: Backplane CON3 (J3) Pin Definitions

Pin	Z	A	B	C	D	E	F
19	GND	IDE.PWRGD	IDE.IOCS16#	IDE.IOCHRDY	IDES.IRQ	IDEP.IRQ	GND
18	GND	IDES.CS3#	IDES.CS1#	IDEP.CS3#	IDEP.CS1#	IDES.DAK#	GND
17	GND	IDEP.D15	IDEP.D14	IDEP.D13	IDEP.D12	IDES.DRQ	GND
16	GND	IDEP.D11	IDEP.D10	IDEP.D9	IDEP.D8	IDEP.DAK#	GND
15	GND	IDEP.A0	IDEP.A1	VCC	IDEP.A2	IDEP.DRQ	GND
14	GND	IDEP.D7	IDEP.D6	IDEP.D5	IDEP.D4	IDEP.IOW#	GND
13	GND	IDEP.D3	IDEP.D2	IDEP.D1	IDEP.D0	IDEP.~IOR	GND
12	GND	FD.DS0#	FD.MSEN0	FD.MTR0#	FD.INDEX#	FD.WDATA#	GND
11	GND	FD.DS1#	FD.DSKCHG#	FD.MTR1#	FD.DENSEL	FD.RDATA#	GND
10	GND	FD.WP#	FD.HDSEL#	FD.DIR#	FD.TRK0#	FD.STEP#	GND
9	GND	FD.WGATE#	IDES.D15	IDES.D14	IDES.D13	USB0+	GND
8	GND	IDES.D12	IDES.D11	VCC	IDES.D10	USB0-	GND
7	GND	IDES.D9	IDES.D8	IDES.D7	IDES.D6	IDES.IOW#	GND
6	GND	IDES.D5	IDES.D4	IDES.D3	IDES.D2	IDES.IOR#	GND
5	GND	ABORT#	MSDAT	SPKR	KBDAT	RSV	GND
4	GND	PRST#	MSCLK	VCC	KBCLK	S2RXD	GND
3	GND	S2CTS	S2RTS	S2DSR	S2DCD	S2TXD	GND
2	GND	IDES.D1	IDES.D0	S2RIN	S2DTR	--	GND
1	GND	IDES.A0	IDES.A1	IDES.A2	RSV	--	GND

Legend: *The greyed table cells indicate the power grouping*

IDE Primary and shared Primary/Secondary signals
IDE Secondary signals
CON22 (COM2), and USB signals
Mouse, keyboard, reset, speaker, and reserved signals
Floppy signals

Table A-13: Backplane CON4 (J4) Pin Definitions

Pin	Z	A	B	C	D	E	F
25	GND	VCC	S1DTR	USB1+	+3.3V	VCC	GND
24	GND	S1CTS	PD0	Init	GND	Link LED 2	GND
23	GND	+3.3V	S1RXD	USB1-	VCC	GND	GND
22	GND	S1RTS	PD1	Active LED 2	GND	Transmit – 2	GND
21	GND	+3.3V	S1TXD	AutoFD	GND	GND	GND
20	GND	S1DSR	PD2	SelectIN	GND	Transmit + 2	GND
19	GND	+3.3V	PD3	Strobe	GND	GND	GND
18	GND	S1RIN	PD4	Speed LED 2	GND	Receive – 2	GND
17	GND	+3.3V	PD5	BUSY	GND	GND	GND
16	GND	S1DCD	PD6	VIO	GND	Receive + 2	GND
15	GND	+3.3V	PD7	ACK	GND	GND	GND
12-14	GND	Key	Area	--	--	--	GND
11	GND	DCLKVGA	OCO	PE	GND	GND	GND
10	GND	DATAVGA	WDLED	Active LED 1	GND	Transmit - 1	GND
9	GND	HSYVGA	TEMPLED	Select	GND	GND	GND
8	GND	VSYVGA	SCSILED	VIO	GND	Transmit + 1	GND
7	GND	GND	PIIX4 GPO30	Error	GND	GND	GND
6	GND	BVGA	PIIX4 GPO29	Speed LED 1	GND	Receive - 1	GND
5	GND	GND	PIIX4 GPO28	PIIX4 GPI16	GND	GND	GND
4	GND	GVGA	GND	VIO	GND	Receive + 1	GND
3	GND	GND	PIIX4 GPO27	PIIX4 GPI15	VCC	GND	GND
2	GND	RVGA	VCC	PIIX4 GPI14	GND	Link LED 1	GND
1	GND	VCC	-12V	PIIX4 GPI13	+12V	VCC	GND

Legend: *The greyed table cells indicate the power grouping*

Ethernet1 and Ethernet2 signals
Parallel Port signals
GPIO
CON21 (COM1) and USB signals
LED signals
VGA and reserved signals

Table A-14: Backplane CON5 (J5) Pin Definitions

Pin	Z	A	B	C	D	E	F
22	GND	NC	NC	NC	NC	NC	GND
21	GND	NC	NC	NC	NC	NC	GND
20	GND	NC	NC	NC	NC	NC	GND
19	GND	NC	NC	NC	NC	NC	GND
18	GND	NC	NC	NC	NC	NC	GND
17	GND	NC	NC	NC	NC	NC	GND
16	GND	NC	NC	NC	NC	NC	GND
15	GND	NC	NC	NC	NC	NC	GND
14	GND	NC	NC	NC	NC	NC	GND
13	GND	NC	NC	NC	NC	NC	GND
12	GND	NC	NC	NC	NC	NC	GND
11	GND	RS232 Cont.	GND	VIO	Fan Sense	Free	GND
10	GND	Free	-DB11	-DB10	GND	-DB9	GND
9	GND	-DB8	GND	VIO	-I/O	-REQ	GND
8	GND	-C/D	-SEL	-MSG	GND	-RST	GND
7	GND	-ACK	GND	VIO	-BSY	-ATN	GND
6	GND	TERMPWR	TERMPWR	TERMPWR	GND	TERMPWR	GND
5	GND	TERMPWR	GND	VIO	TERMPWR	TERMPWR	GND
4	GND	VIO	DET_CON1	DET_CON2	GND	-DB_P	GND
3	GND	-DB7	GND	-DB6	-DB5	-DB4	GND
2	GND	-DB3	-DB2	-DB1	-DB0	-DB_P1	GND
1	GND	-DB15	RIOPRESENT	-DB14	-DB13	-DB12	GND

Legend: *The greyed table cells indicate the power grouping*

SCSI signals

Control signals

A.5.14 General Purpose I/O Interface

These general purpose inputs and outputs are directly connected to the PIIX4 chip on the CP603.

Note:

To use these general purpose I/O's on the CP603 two resistor networks must be set.

A.5.14.1 General Purpose I/O Connector CON9 Pinout

Table A-15: General Purpose I/O Connector CON9 Pinout

Pin	Signal	Pin	Signal
1	GND	**2**	GND
3	GPI13	**4**	GPI14
5	GPI15	**6**	GPI16
7	GND	**8**	GND
9	GPO27	**10**	GPO28
11	GPO29	**12**	GPO30
13	GND	**14**	GND
15	+3.3V	**16**	+3.3V
17	VCC	**18**	VCC
19	VCC	**20**	VCC

A.5.15 Pinout of Adapter Connector CON13 for Transition Module TR1

Table A-16: Pinout of Adapter Connector CON13 for Transition Module TR1

Pin	Signal	Pin	Signal
1	PD0	**2**	PD1
3	PD2	**4**	PD3
5	PD4	**6**	PD5
7	PD6	**8**	PD7
9	SLCTIN	**10**	INIT
11	AUTOFD	**12**	STROBE
13	BUSY	**14**	ACK
15	PE	**16**	SLCT
17	ERROR	**18**	GND
19	GND	**20**	GND
21	S1CTS	**22**	S2CTS
23	S1RTS	**24**	S2RTS
25	S1DSR	**26**	S2DSR
27	S1RIN	**28**	S2RIN
29	S1DCD	**30**	S2DCD
31	S1DTR	**32**	S2DTR
33	S1RXD	**34**	S2RXD
35	S1TXD	**36**	S2TXD
37	GND	**38**	GND
39	NC	**40**	NC
41	NC	**42**	NC
43	NC	**44**	NC
45	NC	**46**	NC
47	VCC	**48**	VCC
49	VCC	**50**	VCC

A.6 Jumper Setting

A.6.1 Serial Interfaces COM1 and COM2

The serial interfaces CON3 (COM1) and CON2 (COM2) on the **CP-RIO6-02-TR1** module may be configured for either RS232, RS485 or RS422 by setting solder jumpers.

Table A-17: Serial Interfaces CON3 (COM1) and CON2 (COM2) Jumper Setting

COM2	COM1	RS232	RS422	RS485	Disable
J1	**J46**	Open	Closed	Closed	Closed
J2	**J36**	Open	Open	Closed	--
J3	**J37**	Open	Open	Closed	Open
J4	**J38**	Open	Closed	Open	Open
J5	**J39**	Open	Closed	Open	Open
J6	**J20**	2 - 1	3 - 1	3 - 1	--
J7	**J21**	2 - 1	3 - 1	3 - 1	--
J8	**J22**	2 - 1	3 - 1	3 - 1	--
J9	**J23**	2 - 1	3 - 1	3 - 1	--
J10	**J24**	2 - 1	3 - 1	3 - 1	--
J11	**J25**	2 - 1	3 - 1	3 - 1	--
J12	**J26**	2 - 1	3 - 1	3 - 1	--
J13	**J27**	2 - 1	3 - 1	3 - 1	--
J14	**J44**	Open	Open	Open	--
J15	**J42**	Open	Open	Open	--
J16	**J43**	Open	Open	Open	--
J17	**J45**	Open	Open	Open	--
J18	**J40**	Open	Closed	Open	--
J19	**J41**	Open	Closed	Open	--

Default jumper setting for each interface is RS232

.

Notes on the RS485 settings:

To enable the 390 Ohm termination of the +TRXD line to VCC, close J14 for COM1, J44 for COM2.

To enable the 150 Ohm termination between the two lines +TRXD and -TRXD, close J15 and J16 for COM1, J42 and J43 for COM2.

To enable the 390 Ohm termination of the -TRXD line to GND, close J17 for COM1, J45 for COM2.

A.6.2 Fan Power Supply Voltage Selection

The voltage for the cooling fan may be configured for either 5V or 12V using jumpers J1 and J2

Table A-18: Fan Supply Voltage

Jumper Setting	Voltage
J1 closed	Supply voltage 5V
J2 closed	Supply voltage 12V (default)

A.7 CP603 Rear I/O Routing Possibilities

Using the Rear I/O modules in conjunction with CP603 results in different possibilities to connect peripheral devices. The following summary shows possible combinations and the required configuration settings / rules.

A.7.1 Serial Ports

Table A-19: Serial Ports

Port	Connector On	Function	Configured	Enabled
COM1	CP603-Base	RS232	--	BIOS or Rear I/O registers
	or CP-RIO6-02 + CP-RIO6-02-TR1	RS232/RS422/RS485	J20-J27,J36-J46 CP-RIO6-02-TR1	J46,J37-J39
COM2	CP603-Base + CP602-VGA1	CP603-Base + CP602-VGA1	J1-J19 CP602-VGA1	J1,J3-J5
	or CP-RIO6-10	RS232/RS422/RS485	J1-J19 CP-RIO6-10	J1,J3-J5
	or CP-RIO6-02 + CP-RIO6-02-TR1	RS232/RS422/RS485	J1-J19 CP-RIO6-02-TR1	J1,J3-J5
	or CP-RIO6-02 optional com2	RS232	--	J3

Important!

Only one connector may be used, make sure all other connectors and there respective drivers are disabled.

A.7.2 Parallel Ports

Table A-20: Parallel Ports

Port	Connector On	Function	Connector Type
LPT1	CP603-Base + CP602-VGA1 or CP-RIO6-02 + CP-RIO6-02-TR1	Parallel Port	25-pin D-sub

Important!

Both possible parallel ports are electrically identical and not separated. Do not connect devices at both connectors at the same time.

A.7.3 VGA Port

Table A-21: VGA Port

Port	Connector On	Selected
VGA	CP603-Base + CP602-VGA1 or CP-RIO6-02	SJ J20-J26 on CP602-VGA1

Note:

Video output may be routed either to the front panel or the CP-RIO6-02 Rear I/O. It is not possible to use both connectors in parallel.

A.7.4 Keyboard/Mouse Ports

Table A-22: Keyboard/Mouse Ports

Port	Connector On	Function	Connector Type
Keyboard/ Mouse	CP603-Base Keyboard	Keyboard + Mouse	6-pin mini din
	or CP-RIO6-02 Keyboard	Keyboard + Mouse	6-pin mini din
	or CP-RIO6-10 Keyboard	Keyboard + Mouse	6-pin mini din
	or CP-RIO6-10 Keyboard +Mouse	Keyboard + Mouse	9-pin sub min D
	or CP-RIO6-02 Keyboard CP RIO6-02 Mouse	Keyboard Mouse	6-pin mini din 6-pin mini din
	or CP-RIO6-10 Keyboard CP-RIO6-10 Mouse	Keyboard Mouse	6-pin mini din 6-pin mini din

Note

All PS2 connectors are electrically identical. Due to this it is not possible to use a mouse at the front panel and a second mouse at the Rear I/O port at the same time.

A.7.5 Ethernet Ports

Table A-23: Ethernet Ports

Port	Connector On	Selected
Ethernet 1/2	CP603-Base or CP-RIO6-02	BIOS setting or Rear I/O Configuration Register.

Note:

Both fast ethernet channels are decoupled, but enabled separately. It is not possible to operate both the Rear and Front I/O at the same time. Switching over from front to rear or vice versa is effected under Software control without the need to plug/unplug ethernet cables.

A.7.6 SCSI Ports

Table A-24: SCSI Ports

Port	Connector On	Configured
Onboard SCSI	CP603-Base onboard or CP-RIO6-02 onboard or CP-RIO6-02 backpanel	Auto termination No termination No termination

Important!

There is no termination on the RIO6-02; if one of the connectors on the RIO6-02 is used, an external terminator must be provided.

A.7.6.1 SCSI Cabling Illustrative Diagrams

Figure A-9: CP603: SCSI with Rear I/O

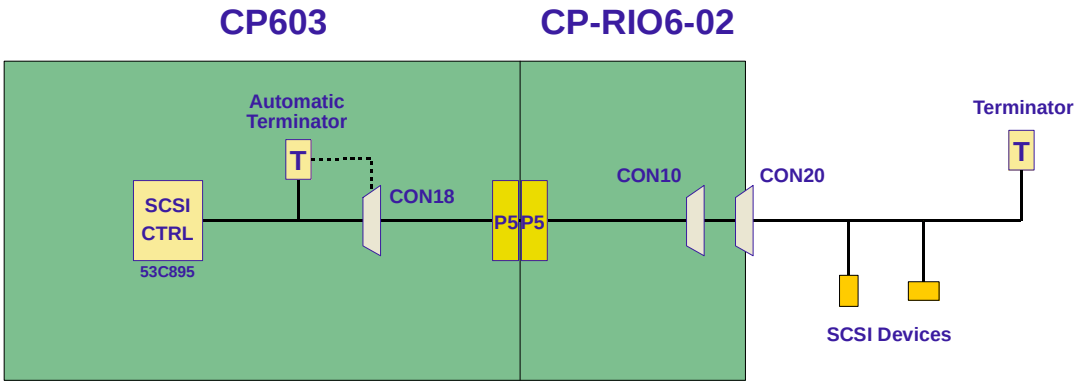


Figure A-10: SCSI using both Rear I/O and onboard CP603 connectors

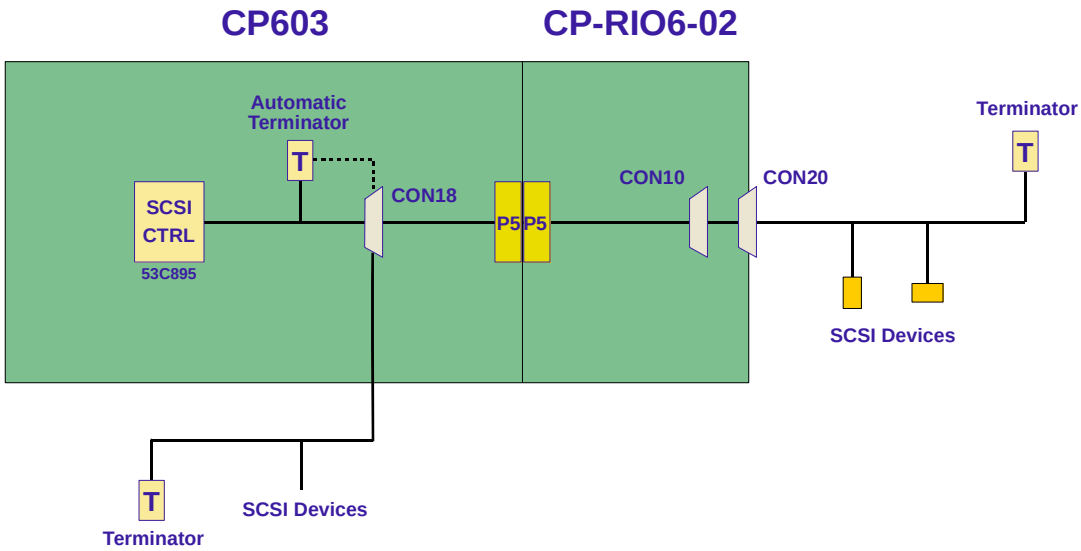
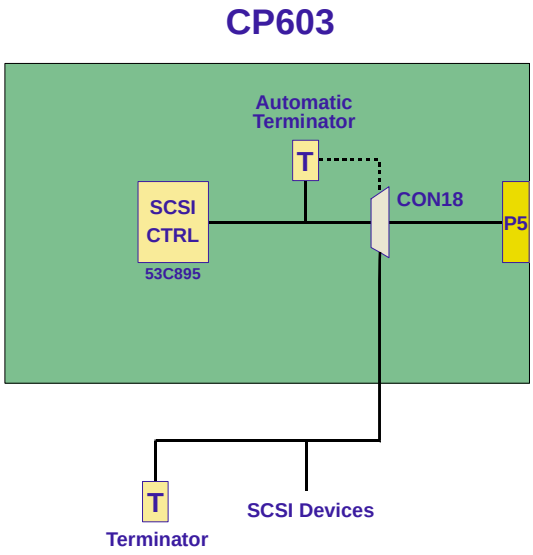


Figure A-11: SCSI without Rear I/O



A.7.7 USB Ports

Table A-25: USB Ports

Port	Connector On
USB	CP603-Base 2 ports
	or CP-RIO6-02 2 ports
	or CP-RIO6-10 1 port

Important!

All ports are electrically connected and in relation to the power supply should be treated as if operating as a single device. Take care that the available current is not overloaded when multiple ports are used.

A.7.8 Floppy Disk Port

Table A-26: Floppy Disk Port

Port	Connector On	Function
Floppy	CP603-Base	20-pin High Density connector
	or CP-RIO6-02	Standard 34-pin connector
	or CP-RIO6-10	Standard 34-pin connector

Important!

Only one floppy connector may be used at a time; connecting both floppy drives to the CP603 baseboard and the CP-RIO6-10 simultaneously will result in malfunction and data loss.

A.7.9 IDE Ports

Table A-27: IDE Ports

Port	Connector On	Function
IDE 1/2	CP603-Base	Standard 40-pin connector
	or CP-RIO6-02	Standard 40-pin connector
	or CP-RIO6-10	Standard 40-pin connector

Attention!

Only one IDE connector may be used at a time through the same port; connecting both IDE devices to the CP603 baseboard and the CP-RIO6-10 simultaneously will result in malfunction and data loss. IDE channels 1 and 2 are separate channels - it is possible to use IDE channel 1 on the CP603 onboard and channel 2 via the Rear I/O.

Appendix B

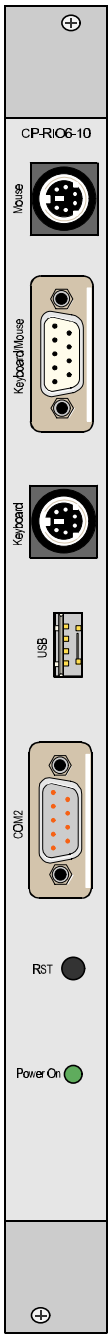
Rear I/O Module CP-RIO6-10

This page was intentionally left blank.

B Rear I/O Module CP-RIO6-10

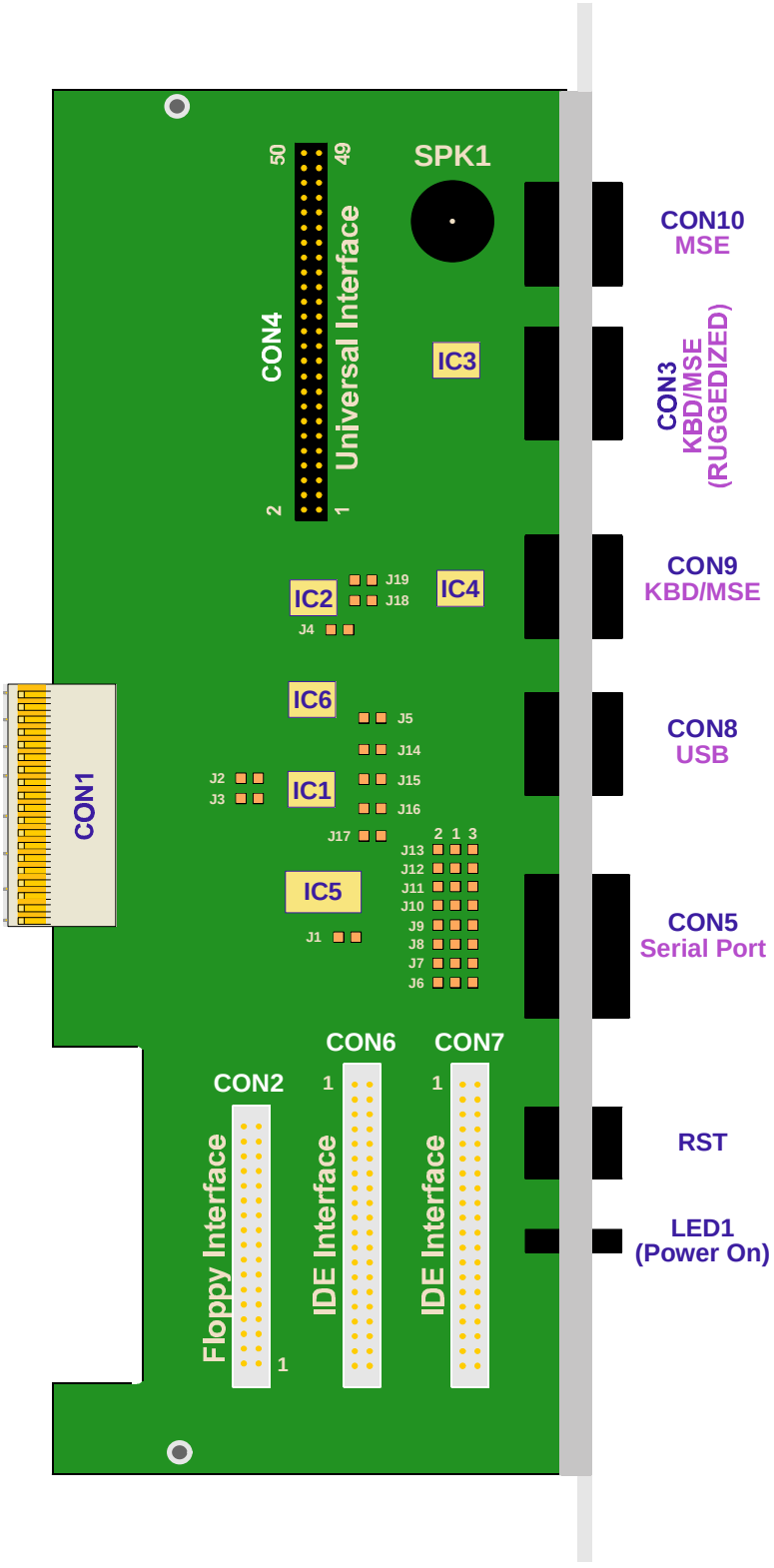
B.1 Front Panel

Figure B-1: Front Panel View of CP-RIO6-10 Rear I/O Module



B.2 Board Layout

Figure B-2: CP-RIO6-10 Rear I/O Module Board Layout



B.3 Introduction

All 6U CPU boards provided with a P3 Rear I/O connector can be upgraded with the Rear I/O module CP-RIO6-10 which is inserted at the back of the system. It is plugged into the backplane CompactPCI connector P3 in line with the CPU board.

If a Rear I/O module is used, the signals of some (all signals in the case of the CP-RIO6-02 Rear I/O) of the main board/front panel connectors are routed to the module interfaces. Thus, the use of Rear I/O modules makes it much easier to remove the CPU in the rack as there is practically no cabling on the CPU board.

B.3.1 Dimensions

The size of the 6U Rear I/O module CP-RIO6-10 is as follows:

- 233.35mm x 80mm

The Rear I/O module CP-RIO6-10 is provided with the following front panel interfaces:

B.3.2 CP-RIO6-10 Front panel Interfaces

Interfaces available via the Front Panel connectors

- serial interface COM2
- USB port
- PS/2 mouse connector
- PS/2 keyboard and/or mouse connector
- keyboard/ mouse connector for rugged applications
- reset button
- green LED indicating "Power On"

B.3.3 CP-RIO6-10 Internal interfaces (Accessible via Onboard Connectors)

In addition, the CP-RIO6-10 is provided with the following internal interfaces

- Rear I/O connector
- floppy-disk connector
- two IDE connectors
- universal connector (signals from front panel elements)
- onboard speaker

B.4 Rear I/O Module CP-RIO6-10 Interfaces

The CP-RIO6-10 Rear I/O module is provided with the front panel and internal interfaces described below. When this module is used, the signals of some of the main board/front panel connectors are routed to the module interfaces..

Note:

If the functionality of a main board/front panel interface is routed to the respective module interfaces, any of these connectors may be used, but only one connector at a time.

B.4.1 Rear I/O Module CP-RIO6-10 CompactPCI Interface

B.4.1.1 CompactPCI Connector CON1 (J3)

The CP-RIO6-10 is provided with a 2 mm x 2 mm female Rear I/O connector J3. The same pinout applies to the matching Rear I/O connector P3 of the CP600/CP610 baseboard. For convenience this table is presented both here and in the “Functional Description and Configuration” chapter.

Table B-1: Rear I/O CompactPCI Connector CON1 (J3)

Pin	Z	A	B	C	D	E	F
19	GND	IDE.PWRGD	IDE.IOCS16#	IDE.IOCHRDY	IDES.IRQ	IDEP.IRQ	GND
18	GND	IDES.CS3#	IDES.CS1#	IDEP.CS3#	IDEP.CS1#	IDES.DAK#	GND
17	GND	IDEP.D15	IDEP.D14	IDEP.D13	IDEP.D12	IDES.DRQ	GND
16	GND	IDEP.D11	IDEP.D10	IDEP.D9	IDEP.D8	IDEP.DAK#	GND
15	GND	IDEP.A0	IDEP.A1	VCC	IDEP.A2	IDEP.DRQ	GND
14	GND	IDEP.D7	IDEP.D6	IDEP.D5	IDEP.D4	IDEP.IOW#	GND
13	GND	IDEP.D3	IDEP.D2	IDEP.D1	IDEP.D0	IDEP.~IOR	GND
12	GND	FD.DS0#	FD.MSEN0	FD.MTR0#	FD.INDEX#	FD.WDATA#	GND
11	GND	FD.DS1#	FD.DSKCHG#	FD.MTR1#	FD.DENSEL	FD.RDATA#	GND
10	GND	FD.WP#	FD.HDSEL#	FD.DIR#	FD.TRK0#	FD.STEP#	GND
9	GND	FD.WGATE#	IDES.D15	IDES.D14	IDES.D13	USB+	GND
8	GND	IDES.D12	IDES.D11	VCC	IDES.D10	USB-	GND
7	GND	IDES.D9	IDES.D8	IDES.D7	IDES.D6	IDES.IOW#	GND
6	GND	IDES.D5	IDES.D4	IDES.D3	IDES.D2	IDES.IOR#	GND
5	GND	ABORT#	MSDAT	SPKR	KBDAT	RSV	GND
4	GND	PRST#	MSCLK	VCC	KBCLK	S1RXD	GND
3	GND	S1CTS	S1RTS	S1DSR	S1DCD	S1TXD	GND
2	GND	IDES.D1	IDES.D0	S1RIN	S1DTR	S2RXD	GND
1	GND	IDES.A0	IDES.A1	IDES.A2	RSV	S2TXD	GND

Legend:

- IDE primary and shared primary/secondary signals
- IDE secondary signals
- Floppy-disk signals
- COM1, COM2, and USB serial signals
- Mouse, keyboard, reset, speaker, and reserved signals

B.4.2 Serial Port Interface

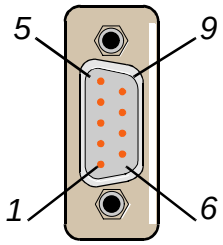


Figure B-3: PC-Compatible D-Sub Serial Connector COM2

Depending on whether the rear I/O module is used with the single-width or double-width version of the 6U CPU board, an additional and/or alternative 9-pin male connector, COM2, is available on the module which can alternatively support an RS232, RS422 or RS485 interface, the standard configuration being RS232. This interface includes a complete set of handshaking and modem control signals, maskable interrupt generation and data transfers of up to 460.8 kB/s..

Table B-2: Serial Interface Configuration with CP-RIO6-10 Module

CP603 baseboard	The main board serial interface CON5 (COM2) signals are routed to the Rear I/O module interface CON5 (COM2). Only one serial port maybe used at a time.

Note:

The functionality of the Rear I/O module and main board/transition module serial interfaces depends on whether the Rear I/O module is used in combination with a transition module (double-width board) or not (single-width board). If a Rear I/O module is used in combination with a transition module, either the drivers for the serial interface on the rear I/O module or the drivers for CON5 (COM2) on the transition module must be disabled to ensure proper functionning.

B.4.2.1 Serial Port Connector CON5 (COM2) Pinout

Table B-3: Serial Port Connector CON5 (COM2) Pinout

Pins	RS232	RS422*	RS485
1	DCD	+RXD	N/C
2	RXD	+CTS	N/C
3	TXD	+TXD	+TRXD
4	DTR	+RTS	N/C
5	GND	GND	GND
6	DSR	-RXD	N/C
7	RTS	-CTS	N/C
8	CTS	-TXD	-TRXD
9	RI	-RTS	N/C

* The RS422 pinout is *PEP*-specific. The signals “DTR” and “DCD” are not pinned out.

B.4.3 Keyboard/Mouse Connectors

The CP-RIO6-10 module is provided with three keyboard and/or mouse connectors; two normal and one ruggedised..

Table B-4: Keyboard/Mouse Connectors

6-Pin Mini-DIN for Mouse	CON 10
6-Pin Mini-DIN for Keyboard/Mouse	CON 9
9-Pin Female D-sub for Keyboard/Mouse	CON 3

B.4.3.1 Normal Keyboard/Mouse PS/2 Interfaces

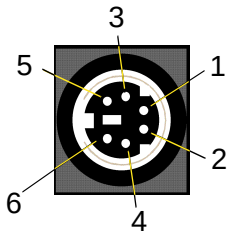


Figure B-4: Keyboard/Mouse PS/2 Connector

The CP-RIO6-10 module is provided with two PC/AT standard keyboard/mouse connectors realized as PS/2-type 6-pin shielded mini-DIN connectors. The keyboard power supply unit is protected by a 500 mA fuse. All signal lines are EMI-filtered.

B.4.3.2 Ruggedized Keyboard/Mouse Interface CON3

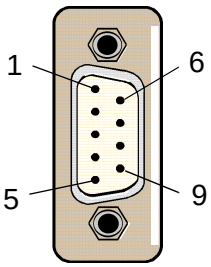


Figure B-5: Keyboard/Mouse D-sub Connector CON3

A special 9-pin female D-sub connector is provided on the CP-RIO6-10 module for rugged industrial applications where there is danger of disconnection of ordinary connectors due to vibration. All the signals from the keyboard/mouse connectors CON9 and CON10 are routed to this connector.

Note:

To use the keyboard/mouse connector CON3 a special cable is necessary (for pinout please see table 4-6 on page 11 of this chapter).

B.4.3.3 Keyboard/Mouse Connector Pinouts

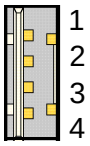
The pinouts of the keyboard/mouse connectors are described in the following table.

Table B-5: Keyboard/Mouse Connector Pinouts

Pin	CON10	CON9	CON3
1	MDATA	KDATA	MDATA
2	NC	MDATA	GND
3	GND	GND	VCCPS2
4	VCCPS2	VCCPS2	NC
5	MCLK	KCLK	KCLK
6	NC	MCLK	MCLK
7	--	--	GND
8	--	--	VCCPS2
9	--	--	KDATA

B.4.4 USB Interface

Figure B-6: USB Connector CON8



When the CP-RIO6-10 module is used, the signals from pins 1 through 4 of the main board connector BU7 are routed to the module interface CON8.

One USB interface with a maximum transfer rate of 12 Mbit each is provided. The USB power supply feeding the connector is protected by a 1.5 A fuse. All signal lines are EMI-filtered..

Note:

Only one USB connector is accessible from the CP-RIO6-10 module front panel.

B.4.4.1 USB Connector CON8 Pinout.

Table B-6: USB Connector CON8 Pinout

Pin	Name	Function	In/Out
1	VCC	VCC signal	--
2	UV0-	Diff. USB-	--
3	UV0+	Diff. USB+	--
4	GND	GND signal	--

B.4.5 IDE Interfaces

When the CP-RIO6-10 module is used, the main board IDE interfaces IDE1 and IDE2 are routed to the module interfaces IDE0, IDE1 respectively.

B.4.5.1 IDE Interface CON6 and CON7 Pinouts

Table B-7: Pinout of AT Standard Connectors CON6 and CON7

Pin	Signal	Function	In/Out
1	IDERESET	Reset HD	Out
2	GND	Ground signal	--
3	HD7	HD data 7	In/Out
4	HD8	HD data 8	In/Out
5	HD6	HD data 6	In/Out
6	HD9	HD data 9	In/Out
7	HD5	HD data 5	In/Out
8	HD10	HD data 10	In/Out
9	HD4	HD data 4	In/Out
10	HD11	HD data 11	In/Out
11	HD3	HD data 3	In/Out
12	HD12	HD data 12	In/Out
13	HD2	HD data 2	In/Out
14	HD13	HD data 13	In/Out
15	HD1	HD data 1	In/Out
16	HD14	HD data 14	In/Out
17	HD0	HD data 0	In/Out
18	HD15	HD data 15	In/Out
19	GND	Ground signal	--
20	N/C	--	--
21	IDEDRQ	DMA request	In
22	GND	Ground signal	--
23	IOW	I/O write	Out
24	GND	Ground signal	--

Table continued on following page

Table B-7: Pinout of AT Standard Connectors CON6 and CON7

Pin	Signal	Function	In/Out
25	IOR	I/O read	Out
26	GND	Ground signal	--
27	IOCHRDY	I/O channel ready	In
28	GND	Ground signal	--
29	IDEDACKA	DMA Ack	Out
30	GND	Ground signal	--
31	IDEIRQ	Interrupt request	In
32	N/C	--	--
33	A1	Address 1	Out
34	N/C	--	--
35	A0	Address 0	Out
36	A2	Address 2	Out
37	HCS0	HD select 0	Out
38	HCS1	HD select 1	Out
39	LED	LED driving	In
40	GND	Ground signal	--

B.4.6 Universal Interface CON4

This 50-pin 2.54mm connector provides all the signals for the front panel elements and for the speaker as set out below.

Table B-8: Universal Connector CON4 Pinouts

Pin	Signal	FP Element	Pin	Signal	FP Element
1	COM, Pin 1	COM	2	COM, Pin 6	COM
3	COM, Pin 2	COM	4	COM, Pin 7	COM
5	COM, Pin 3	COM	6	COM, Pin 8	COM
7	COM, Pin 4	COM	8	COM, Pin 9	COM
9	GND	COM	10	GND	COM
11	NC	--	12	NC	--
13	VCCUSB	USB	14	VCCUSB	USB
15	UV0-	USB	16	UV0+	USB
17	GNDUSB	USB	18	GNDUSB	USB
19	NC		20	NC	
21	MDATA	Key-board/Mouse	22	MCLK	Keyboard/ Mouse
23	VCCPS2	Key-board/Mouse	24	VCCPS2	Keyboard/ Mouse
25	KDATA	Key-board/Mouse	26	KCLK	Keyboard/ Mouse
27	GND	Key-board/Mouse	28	GND	Keyboard/ Mouse
29	NC	--	30	NC	--
31	RST	Reset button	32	GND	Reset button
33	NC		34	NC	
35	VCC	Speaker	36	SPKR	Speaker
37	NC	--	38	NC	--
39	NC	--	40	NC	--
41	VCC	--	42	VCC	--
43	VCC	--	44	VCC	--
45	NC	--	46	NC	--
47	GND	--	48	GND	--
49	GND	--	50	GND	--

B.4.7 Floppy-Drive Interface

The CP-RIO6-10 is provided with a 34-pin, 2.54-mm connector.

Warning!

If the floppy-disk drive connection cable is inverted (pin 1 in place of pin 34), at “power on”, the floppy-disk drive will work uninterruptedly, with consequent risk of damaging the floppy-disk inserted.

B.4.7.1 Floppy Drive Connector CON2 Pinout

Table B-9: Floppy Drive Connector CON2 Pinout

Pin	Signal	Function	In/Out
2	RWC	Write precompensation	Out
4	N/C	--	--
6	N/C	--	--
8	INDEX	Index pulse	In
10	MOTEN1	Motor 1 enable	Out
12	DRVSEL2	Driver select 2	Out
14	DRVSEL1	Driver select 1	Out
16	MOTEN2	Motor 2 enable	Out
18	DIRECTION	Step direction	Out
20	STEP	Step pulse	Out
22	WRDATA	Write data	Out
24	WREN	Write enable	Out
26	TRACK0	Track 0 signal	In
28	WRPROT	Write protect	In
30	RDDATA	Read data	In
32	HEADSEL	Head select	Out
34	DSKCHG	Disk change	In
ODD NR.	GND	Ground signal	--

More detailed information about the floppy-disk connector, in particular its configuration, is available in section 2.6.8 in chapter 2, “Functional Description and Configuration”.

B.5 Jumper Setting

B.5.1 Serial Port Connector CON5 (COM2) Jumper Settings

The serial port CON5 (COM2) of the module may be set to either RS232, RS422 or RS485 mode by setting solder jumpers ”J1” through “J19” of the module. The standard configuration is RS232.

Table B-10: Serial Port Connector CON5 (COM2) Jumper Settings

Jumper	RS232	RS422	RS485
J1	*Open*	Closed	Closed
J2	*Open*	Open	Closed
J3	*Open*	Open	Closed
J4	*Open*	Closed	Open
J5	*Open*	Closed	Open
J6	*2 - 1*	3 - 1	3 - 1
J7	*2 - 1*	3 - 1	3 - 1
J8	*2 - 1*	3 - 1	3 - 1
J9	*2 - 1*	3 - 1	3 - 1
J10	*2 - 1*	3 - 1	3 - 1
J11	*2 - 1*	3 - 1	3 - 1
J12	*2 - 1*	3 - 1	3 - 1
J13	*2 - 1*	3 - 1	3 - 1
J14	*Open*	Open	Please refer to notes below for settings
J15	*Open*	Open	
J16	*Open*	Open	
J17	*Open*	Open	
J18	*Open*	Closed	Open
J19	*Open*	Closed	Open

The default setting is indicated by italics.

Notes on the RS485 settings:

To enable the 390 Ohm termination of the +TRXD line to VCC, close J14 for COM2.

To enable the 150 Ohm termination between the two lines +TRXD and -TRXD, close J15 and J16 for COM2.

To enable the 390 Ohm termination of the -TRXD line to GND, close J17 for COM2.

Appendix C

Transition Module VGA1

This page was intentionally left blank.

C Transition Module VGA1

C.1 Introduction

The *PEP* CP603 VGA1 module has been designed to provide the CP603 user with an effective gateway to the world of additional standard PC interfaces, via its COM port, Parallel port and VGA interface. This additional capability opens up a wide range of expansion possibilities.

C.2 Board Layout

Figure C-1: VGA1 Transition Module Layout (Front Side)

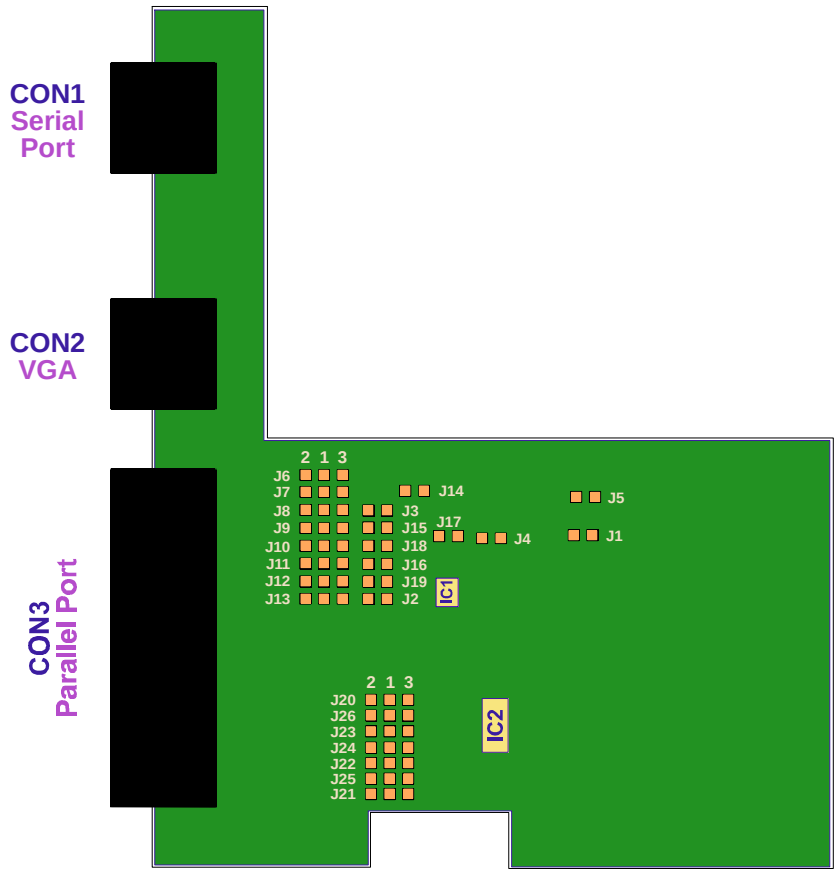
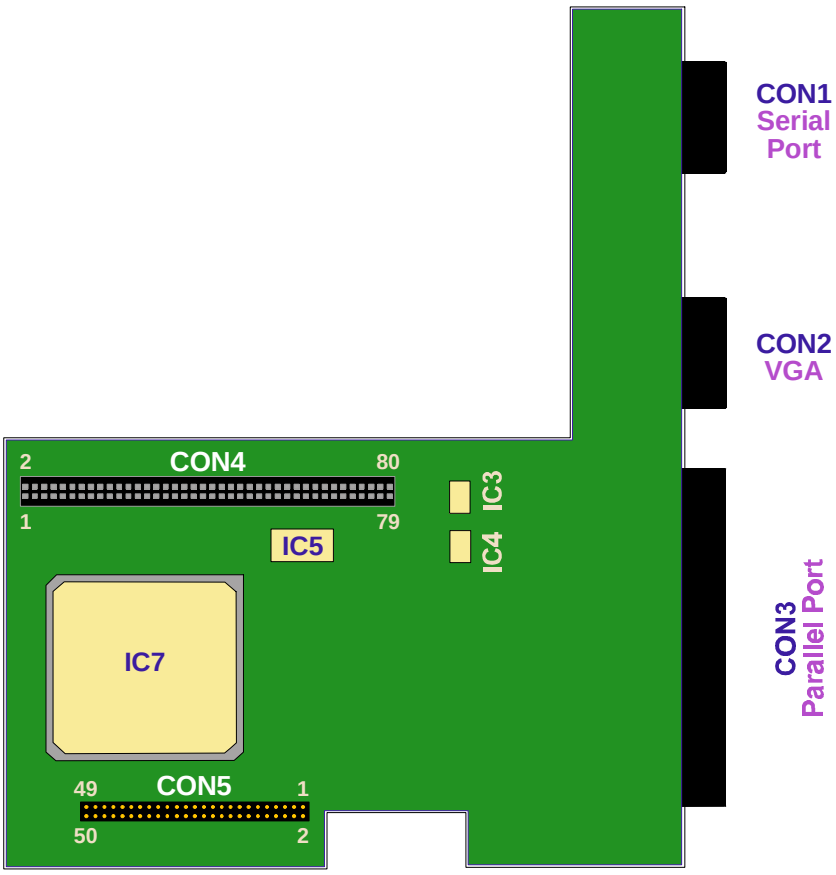


Figure C-2: VGA1 Transition Module Layout (Reverse Side)



C.3 Technical Specifications

Table C-1: Technical Specifications

CP302 I/O Module	Specifications
Parallel port	IEEE 1284; SPP/EPP/ECP parallel mode 25-pin D-sub connector
Serial port	COM2 RS-232/RS422/RS485 one 9-pin D-sub connector
VGA port	AGP video controller: C&T 69030 with 4 MB Resolution: up to 1600x1200x16 @ 60 Hz
Power Supply	3.3V and 5V
Temperature Range	Operating temperature: 0°C to +60ºC -25ºC to +75ºC (optional) E1 Storage temperature: -55ºC to +85ºC

C.4 Transition Module VGA1 Interfaces

C.4.1 VGA Interface

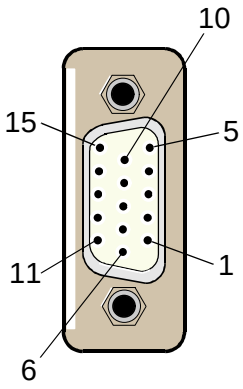


Figure C-3: D-sub VGA Connector CON2

The CP603-VGA1 module is equipped with the integrated Chips&Technologies 69030 VGA chip with 4 MB memory. This chip contains an SVGA controller that is fully compatible with the CGA, EGA, Hercules Graphics, MDA, and VGA video standards. The controller connects directly to the onboard 66 MHz AGP Interface with a maximum data transfer rate of 266 MB per second. The video controller supports pixel resolutions of up to 1600 x 1200 or up to 16.7 M colors. The SVGA controller supports analog VGA monitors on a 15-pin female D-sub connector, with a maximum vertical retrace non-interlaced frequency of 85 Hz.

C.4.1.1 VGA Connector CON2 Pinout

Table C-2: VGA Connector CON2 Pinout

D-sub 15	Signal	Function	In/Out
1	Red	Red video signal output	Out
2	Green	Green video signal output	Out
3	Blue	Blue video signal output	Out
13	HSYNC	Horizontal sync.	TTL out
14	VSYNC	Vertical sync.	TTL out
12	SDATA	I2C data	In/out
15	SCLK	I2C clock	Out
9	VCC	Power +5V 200 mA no fuse protection	Out
5,6,7,8,10	GND	Signal ground	--
4,11	Reserved	--	--

C.4.1.2 Video Resolutions

The CP603 supports different video resolutions to produce different display parameters. A complete list of possible video resolutions and the relating display parameters is shown in the following table:

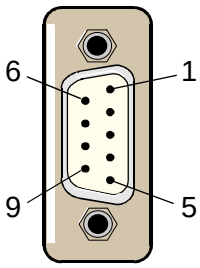
Table C-3: Video Resolutions and Display Parameters

Resolution	Color Depth		Refresh Rate	Comments
	Bits per Pixel	Colors Total		
640 x 480	24	16.7 M	60, 75, 85	True color
800 x 600	24	16.7 M	60, 75, 85	True color
1024 x 768	24	16.7 M	60, 75, 85	True color
1280 x 1024	24	16.7 M	60, 75, 85	True color
1600 x 1200	16	65,536	60	High color

C.4.2 Serial Interface

The CP603 VGA-1 transition module provides an additional serial port COM2. This interface may be configured as an RS-232, RS-422 or RS-485 interface by setting the appropriate solder jumpers. This interface includes the complete signal set for handshaking, modem control, maskable interrupt generation and data transfer of up to 460.8 kB/s.

Figure C-4: PC-Compatible D-sub Serial Port Connector CON1



The COM interface may be configured as RS-232, RS-422 or RS-485 ports by setting the appropriate solder jumpers. The standard setting of the COM port envisages the RS-232 configuration.

RS-422 configuration:

The RS-422 interface use two differential data lines RX and TX for communication (Full-Duplex)

RS-485 configuration:

The RS-485 interface use one differential data line. It differs from the RS-422 modes in that it provides the ability to transmit and receive over the same wire. The RTS signal is used to control the direction of the RS-485 buffer.

C.4.2.1 Serial Port Connector CON1 Pinout.

Table C-4: Serial Port Connector CON1 Pinout (RS232 Mode)

D-sub 9	Signal	Function	In/Out
1	DCD	Data carrier detect	In
2	RXD	Receive data	In
3	TXD	Transmit data	Out
4	DTR	Data terminal ready	Out
5	GND	Signal ground	--
6	DSR	Data send request	In
7	RTS	Request to send	Out
8	CTS	Clear to send	In
9	RI	Ring indicator	In

Table C-5: Serial Port Connector CON1 (RS422 Mode)

D-sub 9	Signal	Function	In/Out
1	+RXD	Receive data	In
3	+TXD	Transmit data	Out
6	-RXD	Inverted receive data	In
8	-TXD	Inverted transmit data	Out
5	GND	Signal ground	--
2, 4, 7	NC	--	--

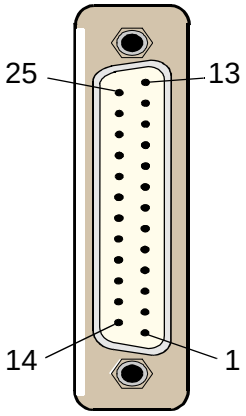
Table C-6: Serial Port Connector CON1 (RS485 Mode)

D-sub 9	Signal	Function
3	+TRXD	+Recieve/Transmit
5	GND	Signal Ground
8	-TRXD	-Receive/Transmit
1,2,4,6,7,9	NC	--

C.4.3 Parallel Port Interface

Figure C-5: PC-Compatible D-sub Parallel Connector

The CP603 VGA-1 Transition Module is provided with an IEEE1284, ECP/EPP-compatible parallel port/printer interface. The parallel port is a 25-pin D-sub female connector mounted on the front panel.



C.4.3.1 Parallel Port Connector CON3 Pinout

Table C-7: Parallel Port Connector CON3 Pinout

D-sub Pin	Signal	Description	Direction	D-sub Pin	Signal	Description	Direction
1	-STB	Strobe data	Out	14	-AFD	Auto feed	Out
2	PD0	LSB of printer data	Out	15	-ERR	Printer error	In
3	PD1	Printer data 1	Out	16	-INIT	Initialize printer	Out
4	PD2	Printer data 2	Out	17	-SLIN	Select printer	Out
5	PD3	Printer data 3	Out	18	GND	Signal ground	N/A
6	PD4	Printer data 4	Out	19	GND	Signal ground	N/A
7	PD5	Printer data 5	Out	20	GND	Signal ground	N/A
8	PD6	Printer data 6	Out	21	GND	Signal ground	N/A
9	PD7	Printer data 7	Out	22	GND	Signal ground	N/A
10	-ACK	Character accepted	In	23	GND	Signal ground	N/A
11	BSY	Busy	In	24	GND	Signal ground	N/A
12	PE	Paper end	In	25	GND	Signal ground	N/A
13	SLCT	Ready to receive	In	N/A	GND	Signal ground	N/C

C.4.4 Transition Module Connection Interface

The VGA1 module connectors located on the baseboard are 2-row, 50-pin and 80-pin female connectors. The matching male connectors CON4 and CON5 on the transition module allow transmission of signals between the two boards.

C.5 Transition Module Jumper Settings

C.5.1 VGA Connector CON2 Jumper Setting

If a rear I/O module is used, the signals of the transition board VGA interface can be routed either to the onboard connector CON2 or to the Rear I/O interface.

Table C-8: VGA Connector CON2 --- Jumper Setting

Jumper	Front I/O	Rear I/O
J20	*1-2*	1-3
J21	*1-2*	1-3
J22	*1-2*	1-3
J23	*1-2*	1-3
J24	*1-2*	1-3
J25	*1-2*	1-3
J26	*1-2*	1-3

The default setting is indicated by italics

C.5.2 Serial Port CON1 Jumper Setting

The additional serial port COM2 of the CP603 VGA-1 transition module can be set to either RS232, RS422 or RS485 mode by setting solder jumpers J1 through J19 of the module. The standard configuration is RS232.

Table C-9: Serial Port CON1 Jumper Setting

COM2	RS232	RS422	RS485	Disable
J1	*Open*	Closed	Closed	Closed
J2	*Open*	Open	Closed	--
J3	*Open*	Open	Closed	Open
J4	*Open*	Closed	Open	Open
J5	*Open*	Closed	Open	Open
J6	*2 - 1*	3 - 1	3 - 1	--
J7	*2 - 1*	3 - 1	3 - 1	--
J8	*2 - 1*	3 - 1	3 - 1	--
J9	*2 - 1*	3 - 1	3 - 1	--
J10	*2 - 1*	3 - 1	3 - 1	--
J11	*2 - 1*	3 - 1	3 - 1	--
J12	*2 - 1*	3 - 1	3 - 1	--
J13	*2 - 1*	3 - 1	3 - 1	--
J14	*Open*	Open	Open	--
J15	*Open*	Open	Open	--
J16	*Open*	Open	Open	--
J17	*Open*	Open	Open	--
J18	*Open*	Closed	Open	--
J19	*Open*	Closed	Open	--

The default setting is indicated by italics

Notes on the RS485 settings appear on the next page.

Notes on the RS485 settings:

To enable the 390 Ohm termination of the +TRXD line to VCC, close J14 for COM2.

To enable the 150 Ohm termination between the two lines +TRXD and -TRXD, close J15 and J16 for COM2.

To enable the 390 Ohm termination of the -TRXD line to GND, close J17 for COM2.

This page was intentionally left blank.