CP303

3U CompactPCI
Processor-M Based CPU Board

(including CP303-V)

Manual ID: 23984, Rev. Index 05
October 20, 2005

User Guide

The product described in this manual is in compliance with all applied CE standards.

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Revision History

Publication Title:	CP303: 3U CompactPCI Processor-M Based CPU Board	
ID Number:	23984	
Rev. Index	**Brief Description of Changes**	**Date of Issue**
01	Initial Issue	Sept. 2001
02	Revision	Dec. 2001
03	Addition of chapter for VGA module and CMOS chapter updated	Apr. 2002
04	General update and addition of appendix D, “CP303-V”	Aug. 2004
05	General update of appendix C, “CP-RIO3-02 Rear IO Module”	Oct 20, 2005

Imprint

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Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements where possible. Many of the components used (structural parts, printed circuit boards, connectors, batteries, etc.) are capable of being recycled.

Final disposition of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

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Explanation of Symbols

CE Conformity

This symbol indicates that the product described in this manual is in compliance with all applied CE standards. Please refer also to the section “Applied Standards” in this manual.

Caution, Electric Shock!

This symbol and title warn of hazards due to electrical shocks (> 60V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.

Please refer also to the section “High Voltage Safety Instructions” on the following page.

Warning, ESD Sensitive Device!

This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Please read also the section “Special Handling and Unpacking Instructions” on the following page.

Warning!

This symbol and title emphasize points which, if not fully understood and taken into consideration by the reader, may endanger your health and/or result in damage to your material.

Note ...

This symbol and title emphasize aspects the reader should read through carefully for his or her own advantage.

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For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions

Warning!

All operations on this device must be carried out by sufficiently skilled personnel only.

Caution, Electric Shock!

Before installing your new Kontron product into a system always ensure that the mains power is switched off. This applies also to the installation of piggybacks.

Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing work.

Special Handling and Unpacking Instructions

ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

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General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron Modular Computers GmbH and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board, please re-pack it as nearly as possible in the manner in which it was delivered. In the event that the original packaging material is not available for storage or warranty shipments, packaging which complies with the standards indicated in section 1.8 may be used to ensure the proper protection of this product.

Special care is necessary when handling or unpacking the product. Please consult the special handling and unpacking instruction on the previous page of this manual.

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If the customer's eligibility for warranty has not been voided, in the event of any claim, he may return the product at the earliest possible convenience to the original place of purchase, together with a copy of the original document of purchase, a full description of the application the product is used on and a description of the defect. Pack the product in such a way as to ensure safe transportation (see our safety instructions).

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Chapter 1

Introduction

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1. Introduction

1.1 System Overview

The CompactPCI board described in this manual operates with the PCI bus architecture to support additional I/O and memory-mapped devices as required by various industrial applications. For detailed information concerning the CompactPCI standard, please consult the complete Peripheral Component Interconnect (PCI) and CompactPCI Specifications. For further information regarding these standards and their use, visit the home page of the *PCI Industrial Computer Manufacturers Group (PICMG)*.

Many system-relevant CompactPCI features that are specific to Kontron Modular Computers CompactPCI systems may be found described in the Kontron CompactPCI System Manual. Due to its size, this manual cannot be downloaded via the internet. Please refer to the section “Related Publications” at the end of this chapter for the relevant ordering information.

The CompactPCI System Manual includes the following information:

- Common information that is applicable to all system components, such as safety information, warranty conditions, standard connector pinouts etc.
- All the information necessary to combine Kontron’s racks, boards, backplanes, power supply units and peripheral devices in a customized CompactPCI system, as well as configuration examples.
- Data on rack dimensions and configurations as well as information on mechanical and electrical rack characteristics.
- Information on the distinctive features of Kontron CompactPCI boards, such as functionality, hot swap capability. In addition, an overview is given for all existing Kontron CompactPCI boards with links to the relating data sheets.
- Generic information on the Kontron CompactPCI backplanes, such as the slot assignment, PCB form factor, distinctive features, clocks, power supply connectors and signalling environment, as well as an overview of the Kontron CompactPCI standard backplane family.
- Generic information on the Kontron CompactPCI power supply units, such as the input/ output characteristics, redundant operation and distinctive features, as well as an overview of the Kontron CompactPCI standard power supply unit family.

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1.2 Kontron Single-Height CPU Boards

1.2.1 Socket 7 Family

The CP312 is a highly integrated 32-bit / 33 MHz CompactPCI single-board computer designed around the Intel® Pentium® and the AMD® K6™ microprocessors. The VGA interface is integrated within the chipset. To achieve high CPU and memory performance the board includes 512 kB L2 Cache. DRAM is 32 MB or 64 MB (soldered) which together with the SODIMM provides up to 128 MB main memory.

1.2.2 Intel® Mobile Pentium® III Family

The CP302 is a high performance 64-bit/33 MHz CompactPCI system controller board designed to utilize the Intel® Mobile Pentium® III microprocessors and future processors. This board is based on the Intel® 440BX AGP sets and can support CPU speeds of 400 MHz through 700 MHz and host bus speeds up to 100 MHz.

The CP301 is a system controller which is identical to the CP302 in every respect except that it has an additional 4HP front panel interface. The CP301 supports two COM ports and one Fast Ethernet connector on the 4HP interface. The USB and keyboard connector are not available on the 4HP version.

The CP302-PM is a non-system controller which is identical to the CP302 apart from having a different PCI/PCI (non-transparent) bridge at J1/J2. This makes possible the addition of further CP302-PMs together with a system controller CPU on one CompactPCI bus, i.e. multiprocessing.

1.2.3 Intel® Pentium® III Processor-M™ Family

The CP303 is an advanced 64-bit / 33 MHz CompactPCI system controller board designed to utilize the Intel® Pentium® III Processor-M™ microprocessors and future processors. The board is based on the Intel® 815-B0 chipset and can support CPU speeds of 800 MHz through 1200 MHz and host bus speeds up to 133 MHz.

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1.3 Board Overview

1.3.1 Board Introduction

The CP303 is designed around the Intel® Pentium® III Processor-M™ family of microprocessors and the Intel® i815-B0 Chipset. The Mobile Processor-M™ microprocessor is based on the same core as existing mobile processors. A key performance factor is the higher processor system bus speed of 133 MHz and the 512 kB integrated L2 cache which runs at full speed. CPU speeds start at 800 MHz and are available up to 1200 MHz.

The CP303 offers more features and expandability than other CompactPCI boards in its class. The board comes with an onboard Ultra ATA/100 interface, up to two 10BASE-T/100BASE-TX Fast Ethernet ports, one integrated in the chipset (82559 type) and one external device based on the Intel® 82559 chip, one CompactFlash type II socket and a built-in Intel® 3D Graphics accelerator for enhanced graphics performance. Several onboard connectors provide flexible 8HP expandability.

To achieve high system performance the board includes up to 256 MB soldered SDRAM suitable for rugged environments and one SODIMM socket for flexible memory upgrading up to 512 MB. The board supports one 64-bit/33 MHz CompactPCI interface.

The specially designed optional CP303-VGA module provides multimedia capabilities on 8HP and features a high performance AGP 4x VGA controller from SMI (Cougar 3DR) optimized for MPEG2 and MPEG4 video decoding with up to 32 MB DDR memory. The video output configuration is very flexible, allowing a choice of CRT-VGA, DVI, two independent LVDS ports, one TV output and one TV input port for the connection of TV cameras. Additional features include a 1394a-2000 OHCI-compliant FireWire™ interface with two connectors, an Audio interface and a 2.5" onboard hard disk interface.

The optional CP303-IDE1 module has been designed to make available all the legacy PC I/O ports. It includes two COM ports, a PS/2 keyboard and mouse port, a parallel port, floppy and a 2.5” onboard hard disk interface.

Designed for stability and packaged in a rugged format, the board fits into all applications situated in industrial environments making it a perfect core technology for long life applications. Components have been selected from embedded technology programs and therefore offer long term availability.

The board is compatible with the Microsoft Windows® NT and Windows® 2000 operating system. However, the performance of CompactPCI can be tailored to suit real-time applications and operating systems such as Linux, or VxWorks®, which are instrumental to the success of CompactPCI in these market sectors.

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1.3.2 Board-Specific Information

The CP303 is a CompactPCI Pentium® III Processor-M™ based single-board computer specifically designed for use in highly integrated platforms with solid mechanical interfacing for a wide range of industrial environment applications.

Some of the CP303's outstanding features are:

- Intel® Pentium® III Processor-M™ microprocessor up to 1200 MHz
- 512 kB L2 cache on-die, running at CPU speed
- 133 MHz processor system bus
- 815-B0 and ICH2 chipset
- Up to 512 MB SDRAM memory
- Integrated 3D high performance VGA controller
- Analog display support up to 1600 x 1200 x 8-bit
- Two Fast Ethernet interfaces
- One EIDE Ultra ATA/100 interface
- Onboard CompactFlash type II socket
- Four USB 1.1 ports
- One PCI-to-PCI bridge 32-bit to 64-bit at 33 MHz
- Compatible with CompactPCI spec. Rev. 3.0
- 1 MB onboard flash (512 KB for BIOS and 512 KB for VxWorks)
- Integrated Hardware Monitor
- Watchdog timer
- Two COM ports (four on 8HP version)
- AGP 4x extension connector
- PCI extension connector
- I/O extension connector (LPC, AC97 Link)
- Several rear I/O configurations
- Jumperless board configuration
- Extended temperature range -40°C to + 85°C
- Passive heat sink solution

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1.4 Optional Modules

1.4.1 CP303-IDE1 Module

The CP303-IDE1 module has been designed to make available all legacy PC I/O ports. It includes two COM ports, a PS/2 keyboard and mouse port, a parallel port plus floppy and hard disk interfaces. This additional capability opens up the broadest range of expansion possibilities.

For standalone applications the module provides the mounting for a 2.5” hard disk drive or FLASH disk.

See Appendix A for more details.

1.4.2 CP303-VGA1 Module

The CP303-VGA1 module has been designed to provide the CP303 user with full access to the multimedia world. The board includes a highly integrated VGA controller from SMI (the Cougar 3DR) with up to 32 MB DDR memory with two high performance graphic engines supporting dual independent graphic displays optimized for MPEG2 and MPEG4 video decoding. The video output configuration is very flexible, allowing a choice of CRT-VGA, DVI, two independent LVDS ports, one TV output and one TV input port for the connection of TV cameras.

A further highlight are two 1394a-2000 OHCI-compliant 400/100 Mbit/s FireWire™ ports, one for internal connection and one routed via the front panel. Additionally, the module includes a very flexible audio interface with several input and output configuration possibilities.

For standalone applications the module provides the mounting for a 2.5” HDD or Flash Disk.

Note ...

When the CP303 VGA1 module is plugged onto the CP303 baseboard, the onboard VGA cannot be used.

1.4.3 CP-RIO3-02 Rear I/O Module

Designed for use with a 32-bit rear I/O variant of the CP303 and a backplane with system slot rear I/O capability, this module provides rear I/O interfacing for the two standard RS232 serial interfaces and one of two Fast Ethernet interfaces.

See Appendix C for more details.

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1.5 System Relevant Information

The following system relevant information is general in nature but should still be considered when developing applications using the CP303.

Table 1-1: System Relevant Information

SUBJECT	INFORMATION
System Configuration	A CP303 master board can support up to 7 peripheral boards with 64-bit and 33 MHz.
Master/Slave Functionality	The CP303 can operate only as a master board.
Board Location in the System	The CP303 board must be installed in a master slot of a CompactPCI backplane.
Hot Swap Compatibility	The CP303 supports the addition or removal of other boards whilst in a powered-up state. Individual clocks for each slot and ENUM signal handling are in compliance with the PICMG 2.1 Hot Swap Specification.
Hardware Requirements	The CP303 can be installed in any CompactPCI 3U rack.
Operating Systems	The CP303 can operate under the following operating systems: Microsoft NT, Microsoft W2000, Linux, VxWorks®

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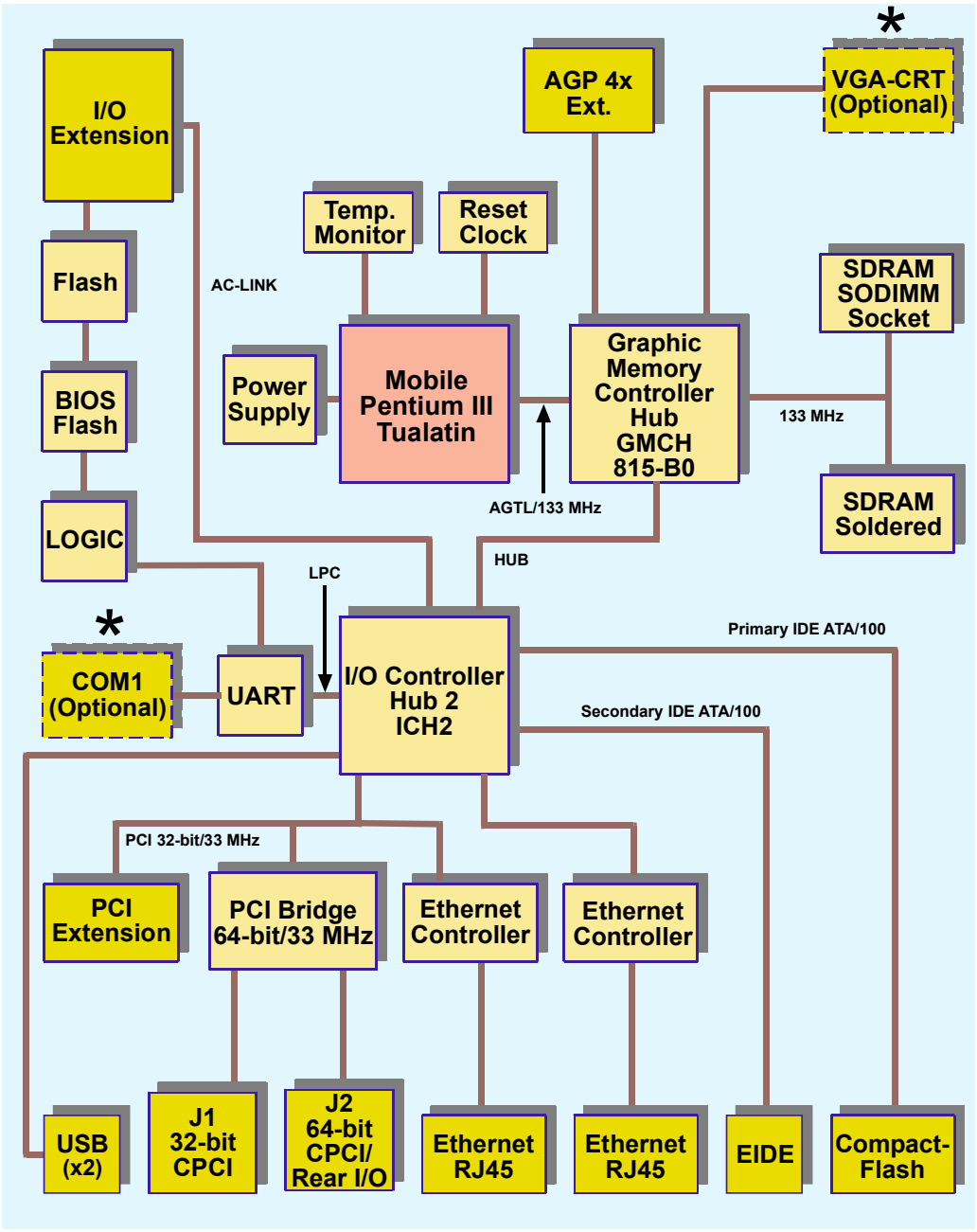
1.6 Board Diagrams

The following diagrams provide additional information concerning board functionality and component layout.

1.6.1 Functional Block Diagram

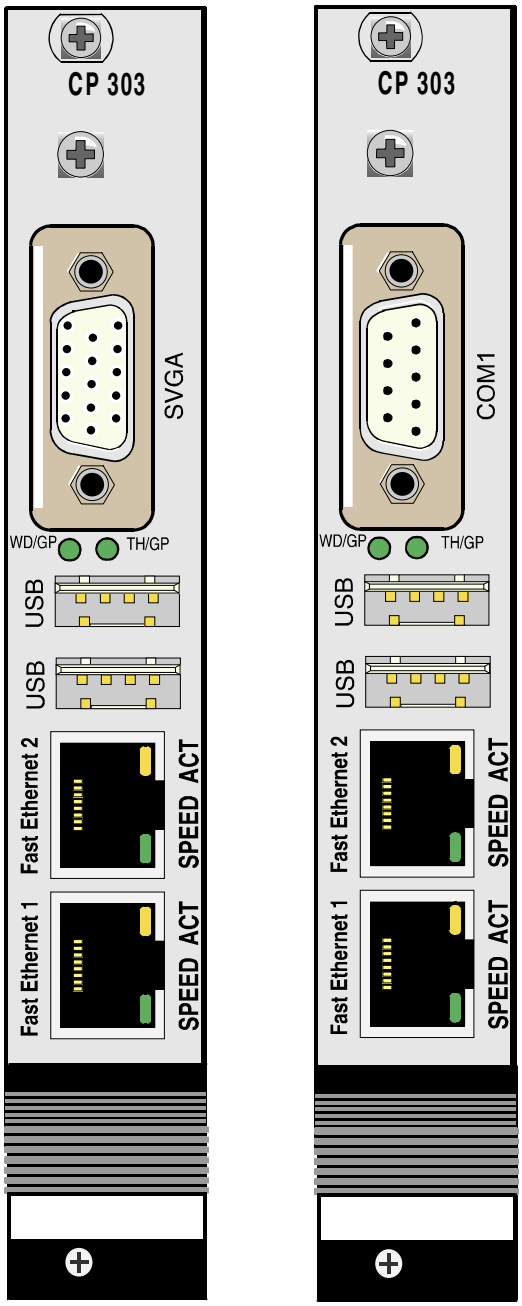
Figure 1-1: CP303 Functional Block Diagram



* either COM1 or VGA-CRT port

1.6.2 Front Panels

Figure 1-2: CP303 4HP Front Panels



LEGEND:

Left CP303: 4HP VGA version

Right CP303: 4HP COM version

General Purpose LEDs

- WD/GP (green): Watchdog or General Purpose
- TH/GP (green): Overtemperature Status or General Purpose

Integral Ethernet LEDs

- ACT (yellow): Ethernet Link/Activity
- SPEED (green): Ethernet Speed

Note ...

For an illustration of the 8HP version front panel, please see Appendix A, CP303-IDE1 module.

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1.6.3 Board Layouts

Figure 1-3: CP303 Board Layout (Front View)

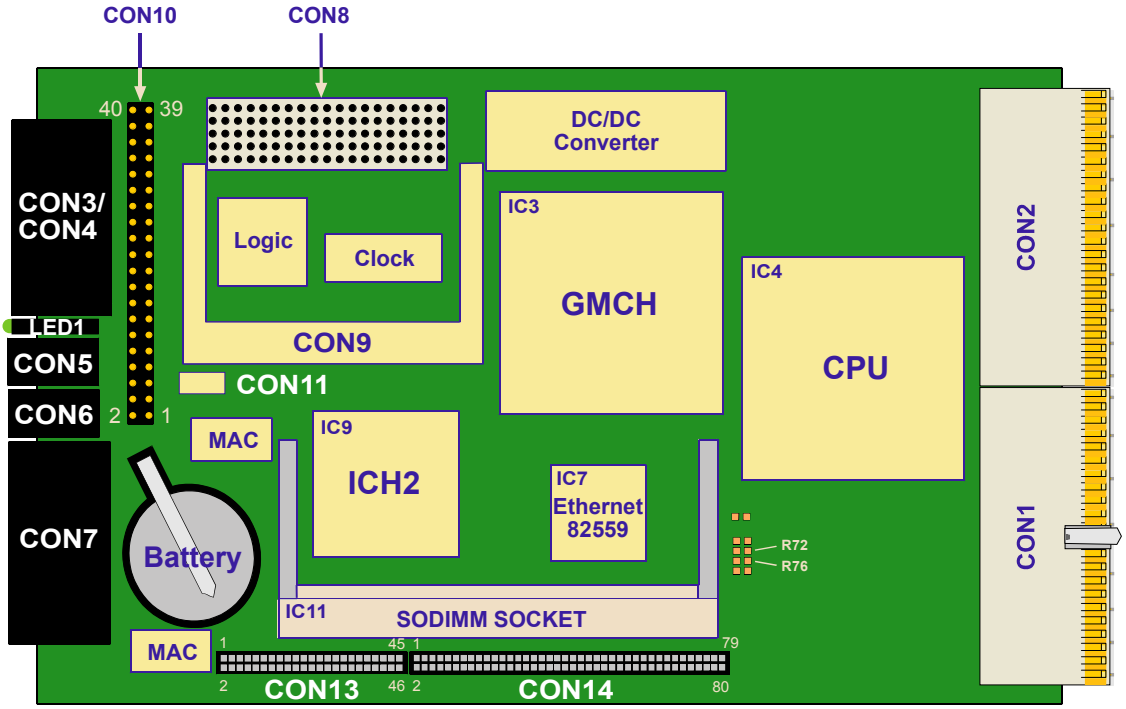
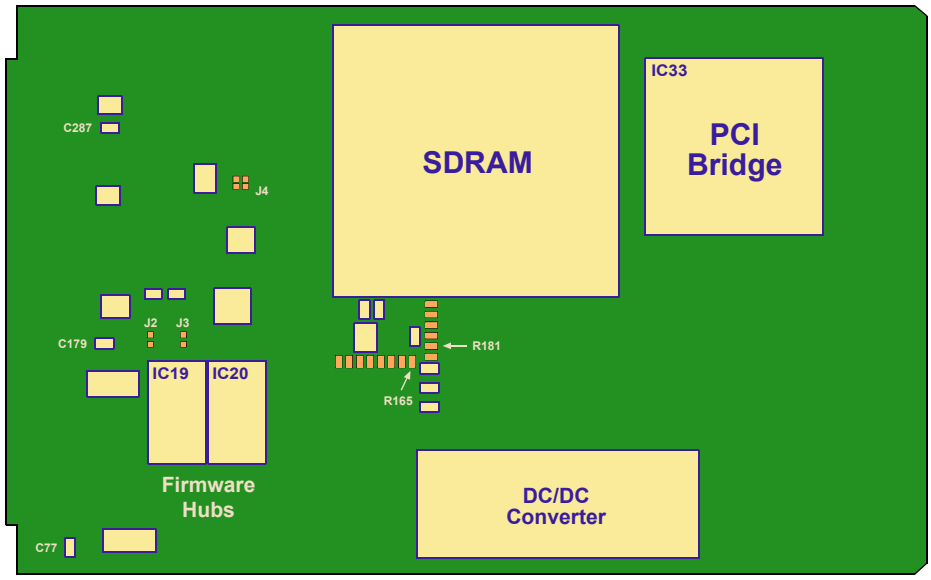


Figure 1-4: CP303 Board Layout (Reverse View)



1.7 Technical Specifications

Table 1-2: CP303 4HP Version Main Specifications

	CP303	Specifications
Processor and Memory	CPU	Intel® Pentium® III Processor-M™ microprocessor up to 1200 MHz with 512 kB L2 on-die cache in 479 Micro-7CBGA packaging.
	Memory	Main Memory (up to 512 MB total memory): up to 256 MB SDRAM via one SODIMM socket running at 133 MHz up to 256 MB SDRAM soldered running at 133 MHz Cache structure: 512 kB L2 on-die full speed processor cache Flash Memory: 512 kB Flash for BIOS and 512 kB Flash extension Memory Extension: CompactFlash socket type II (true IDE mode) EEPROM: Two 256 byte EEPROMs for storing CMOS data when operating without battery and two 256 byte EEPROM for user purposes
Chipset	Intel 815-B0 Graphics Memory Controller Hub (GMCH) chipset	Support for a single Pentium® III microprocessor 64-bit AGTL/AGTL+ based System Bus interface at 66/100/133 MHz 64-bit System Memory interface with optimized support for SDRAM at 133 MHz Integrated 2D and 3D Graphics Engines Integrated H/W Motion Compensation Engine Integrated 230 MHz DAC Integrated Digital Video Out Port AGP 1X/2X/4X Controller
	Intel ICH2 I/O Controller Hub (ICH)	PCI Rev 2.2 compliant with support for 32-bit/33 MHz PCI operations Supports up to six Req/Gnt pairs Power management logic support Enhanced DMA controller, interrupt controller, and timer functions Integrated IDE controller Ultra ATA/100/66/33 USB host interface with two host controllers; supports 4 USB ports Integrated LAN controller (82559 style) System Management Bus (SMBus) compatible with most I2C devices AC™97 2.1 compliant link for audio codecs Low Pin Count (LPC) interface Firmware Hub (FWH) interface support

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Table 1-2: CP303 4HP Version Main Specifications (Continued)

	CP303	Specifications
External Interfaces	AGP/VGA interface	Built-in Intel® 3D Graphics accelerator for enhanced graphics performance. Supports resolutions of up to 1600 x 1200 x 8-bit colors at a 75 Hz refresh rate or 1280 x 1024 x 24-bit true colors at an 85 Hz refresh rate. Hardware motion compensation for software MPEG2 and MPEG4 decoding The graphics controller provides flexible allocation of video memory (frame buffer) up to 16 MB and 1MB legacy video memory for real-time operating systems (e.g. MS DOS). The 8HP CP303-VGA features the Cougar 3DR high performance graphics controller.
	Fast Ethernet Interface	Dual Channel Ethernet by Intel® 82801 (ICH2) chipset integrated LAN controller and Intel 82559 Ethernet controller. Data Rate: 10 & 100 MBit/s Ethernet: Full 802.2 & 802.3 IEEE compliance supporting 10Base-T and 100Base-TX. Cabling: Category 5 two-pair cabling
	USB Interface	The ICH2 contains two USB 1.1 UHCI compliant host controllers with a data transfer rate of up to 12 Mbit/s. Each Host controller includes a root hub with two separate USB ports for each, making a total of four USB ports (two at front I/O, two at rear I/O).
	Serial Ports	Up to Four UARTs, 16C550 compatible. Two on the 4HP version (rear I/O) and two on the CP303 IDE1 module
	CompactPCI Bus Interface	Compatible with CompactPCI Specification V 2.0, Rev. 3.0 64-bit/33 MHz master interface 3.3V/5.0V compatible (default configuration 5.0 V)
	Hot Swap Compatible	The CP303 supports the addition or removal of other boards whilst in a powered-up state. Individual clocks for each slot and Enum signal handling are in compliance with the PICMG 2.1 Hot Swap Specification.
	Rear I/O	When the rear I/O is enabled the CompactPCI interface is configured for 32-bit/33 MHz. The 32-bit CompactPCI bus has rear I/O capability. The following interfaces are routed to the rear I/O connector J2: COM1 and COM2 (TTL signaling), 2xUSBs, CRT VGA, 2xEthernets and general purpose signals.
General	Dimensions, Operating Temperatures, Climatic Humidity, Weight	Dimensions: 100 mm x 160 mm Operating temp.: 0°C to +60°C E1 (optional): -25°C to +75°C E2 (optional): -40°C to +85°C Storage temp.: -55°C to +85°C Climatic humidity: 93% RH at 40 °C, non-condensing Weight: CP303 4HP with heat sink: 337 grams

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Table 1-2: CP303 4HP Version Main Specifications (Continued)

	CP303	Specifications
Interfaces	Front Panel Interfaces - 4HP COM Version	COM: 9-pin D-SUBconnector USB: two 4-pin connectors Ethernet: two RJ-45 connectors Two LEDs yellow: (integrated in Ethernet RJ45 jack): Ethernet Link/Activity Two LEDs green: (integrated in Ethernet RJ45 jack): Ethernet Speed Two LEDs green: Watchdog, Overtemperature Status or General Purpose
	Front Panel Interfaces - 4HP VGA Version	VGA: 15-pin D-SUB connector USB: two 4-pin connectors Ethernet: two RJ-45 connectors Two LEDs yellow: (integrated in Ethernet RJ45 jack): Ethernet Link/Activity Two LEDs green: (integrated in Ethernet RJ45 jack): Ethernet Speed Two LEDs green: Watchdog, Overtemperature Status or General Purpose
	Onboard interfaces	One EIDE interface supporting Ultra ATA/100/66/33 for two devices (hard disks or CD-ROMs) on a 40-pin 2.54mm connector. CompactFlash socket for type II devices (primary EIDE interface) I/O extension connector PCI extension connector AGP4x extension connector
Hardware Monitoring	Thermal Management/ System Monitoring	Watchdog: software configurable watchdog generates IRQ, NMI or hardware reset. Hardware monitor: LM81 monitoring temperature, fan speed and all onboard voltages. Temperature monitor: MAX 1617 monitoring the CPU on-die and board temperature.
	Common Features	DC power monitors (3.3V and 5V) Battery socket and 3.0V lithium battery for RTC: VARTA Type CR2025 PANASONIC BR2020

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Table 1-2: CP303 4HP Version Main Specifications (Continued)

	CP303	Specifications
Software	Software BIOS and Operating System Support	Award BIOS within 512 kB of Flash memory and having the following features: - Award Preboot Agent included; this allows BIOS updates and service functions without VGA or a local disk - LAN-boot capability for diskless systems - Boot from USB floppy and CD-ROM - BIOS boot support for USB keyboards - Software enable/disable function for the rear I/O, Ethernet and COM port configuration for the 4 HP version - Plug and Play capability - Dual BIOS support - The BIOS parameters are saved in the EEPROM - Board serial number in EEPROM - PC Health Monitoring, which allows you to protect your system from problems even before they occur Operating systems supported: Linux, VxWorks®, Windows NT®4.0, Windows 2000 etc.

Note ...

For a description of the additional 8HP version interfaces, please refer to the Technical Specifications table in Appendix A, CP303-IDE1 module.

1.8 Software Support

Real-time operating systems such as VxWorks® and others are supported. The standard PC features supported by the BIOS also allow for PC operating systems such as Linux, MS-DOS®, Windows 9X®, Windows 2000® and Windows NT 4.0® Embedded.

1.8.1 Windows® 2000® Windows NT Embedded

The Microsoft® platforms Windows® 2000/NT and Windows® NT Embedded are rapidly gaining popularity as the solution for embedded application requirements, such as medical systems, industrial automation and, in network devices, routers and switches.

In addition to being a modern, powerful 32-bit operating system platform, Windows provides a number of unique advantages not found in any other embedded operating system.

The familiar Windows Win32® API, with its associated broad range of development tools and knowledge base, provides a broad base of development talent, tools, and expertise.

Windows also offers comprehensive networking support and connectivity to non-embedded and enterprise information systems.

For systems with advanced operator interfaces, there is also the familiar Windows Graphical User Interface (GUI).

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A major benefit of the Windows operating system in embedded applications is the ability to leverage existing off-the-shelf software components, either those in Windows itself or components from a wide range of third party developers.

Embedded system designers who create applications that maximize the use of existing components, and minimize the number of software components that must be written, will realize the lowest development costs and fastest time to market.

Any application, device driver, or service that runs on Windows® NT can be adapted to run on Windows® Embedded. Windows® Embedded is becoming the foundation of a growing number of embedded designs.

Any hardware that supports Windows® NT automatically supports Windows® NT Embedded. With Windows® NT Embedded, developers use off-the-shelf hardware and software to reduce their development costs and accelerate the time to market.

Windows® NT Embedded includes the following embedded enabling features and tools:

- Flash memory support for diskless operation.
- Flexible page file support, including support for "No page file".
- CD-ROM boot support (El Torito).
- Headless operation for systems without display, keyboard, and mouse.
- Remote management tools including a remote command shell and remote GUI desktop.
- Enhanced error support for auto-handling and logging of error dialogs.
- Target Designer - a GUI tool for selecting the Windows® NT Embedded components your system needs.
- Component Designer - a GUI tool for making your application, or any software your application may need, a Windows® NT Embedded component.

Using Target Designer, developers can configure Windows® NT Embedded as a stand-alone system requiring only 8 MB of persistent storage and 12 MB of RAM.

Windows® NT Embedded provides unprecedented benefits for embedded system developers, especially for those deploying applications with high software content and high performance requirements. By combining the capabilities of the Windows® NT operating system with design and operating system creation tools such as the Target Designer and Component Designer, Windows® NT Embedded is destined to become an outstanding solution in the embedded systems marketplace.

1.8.2 WindRiver: VxWork®, RTOS

Tornado was originally designed to solve the problems inherent in a cross-development environment, such as limited host-target communication, limited target resources, and poorly integrated tools. With Tornado® II, WindRiver built upon the Tornado® framework, focusing developer time-to-productivity.

VxWorks®, the run-time component of the Tornado® II embedded development platform, is the most widely adopted real-time operating system (RTOS) in the embedded industry.

Tornado® II also includes a comprehensive suite of core and optional cross-development tools and utilities and a full range of communications options for the target connection to the host.

The flexible VxWorks RTOS comprises the core capabilities of the WindRiver® microkernel along with advanced networking support, powerful file system and I/O management and C++ and other standard run-time support (more than 1800 powerful application program interfaces (HPIS)).

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These core capabilities can be combined with add-on components available from Wind River Systems and Kontron Modular Computers GmbH (e.g. VxWorks driver support for various Kontron CompactPCI boards).

The VxWorks is designed for scalability, enabling developers to allocate scarce memory resources to their application, rather than to the operating system. From deeply embedded designs requiring a few kilobytes of memory, to complex high-end real-time systems where more operating system functions are needed, the developer may choose from over 100 different options to create hundreds of configurations. Individual modules may be used in development and omitted in production systems.

Furthermore, these individual subsystems are themselves scalable, allowing the developer to optimally configure VxWorks run-time software for the widest range of applications. Additionally, TCP, UDP, sockets, and standard Berkeley network services can all be scaled in or out of the networking stack as necessary.

These configuration options may be easily selected by means of the Tornado II project facility´s graphical interface.

1.8.3 Other Operating Systems

Contact *Kontron Modular Computers* for information on other operating systems.

1.8.4 Kontron Support

Kontron is one of the few CompactPCI and VME vendors providing inhouse support for most of the industry-proven real-time operating systems that are currently available. Due to its close relationship with the software manufacturers, *Kontron* is able to produce and support BSPs and drivers for the latest operating system revisions thereby taking advantage of the changes in technology.

Finally, customers possessing a maintenance agreement with *Kontron* can be guaranteed hotline software support and are supplied with regular software updates. A dedicated website is also provided for online updates and release downloads.

1.9 Environmental Considerations

1.9.1 Absolute Maximum Electrical Ratings

Absolute Maximum Ratings indicate limits beyond which damage to the board may occur. Do not operate the CP303 at or beyond these maximum values.

Table 1-3: Voltage Limits

Supply Voltage	Maximum Permitted Value
3.3 V	+4.5 V
5 V	+5.5 V
+12 V	+14 V
-12 V	-14 V

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1.9.2 DC Operating Characteristics

The following table sets out the voltage parameters within which the board is functional. The CP303 cannot be guaranteed to function if the board is not operated within the prescribed limits.

Table 1-4: Voltage Range

Supply Voltage	Limit
3.3 V	3.20 V min. to 3.47 V max.
5 V	4.85 V min. to 5.25 V max.
+12 V	11.4 V min. to 12.6 V max.
-12 V	-11.4 V min. to -12.6 V max.

Note ...

If the main power input is switched off, the supply voltages will not go to 0V instantly. It will take a couple of seconds until the capacitors are discharged. If the voltage rises again before it has gone below a certain level, the circuits may enter a latch-up state where even a hard RESET will not help any more. The system must be switched off for at least 3 seconds before it may be switched on again. If problems still occur, turn off the main power for 30 seconds before turning it on again.

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1.9.3 Power Consumption

The CP303 board is based on the Intel® Pentium® III Processor-M™ microprocessor. Intel® has developed mobile processors to meet the specific needs of mobile PC's. As such, they operate at lower voltages than their desktop counterparts, are significantly smaller in size, consume less power and dissipate less heat. The design is optimized for low power consumption applications.

The goal of this description is to provide a method to calculate the power consumption for the CP303 base board and for additional configurations. The processor dissipates the majority of the thermal power.

The power consumption tables below list the voltage and current specifications for the CP303 board and the CP303 accessories. The values were measured using an 8-slot passive CompactPCI backplane with two power supplies, one for the CPU and the other for the hard disk. During measurement the power consumption of the backplane was ignored. The operating systems in use were DOS 6.22 without power management and Windows 2000 with power management. All measurements were conducted at a temperature of 25°C. The measured values varied, because power consumption was dependent on processor activity.

Table 1-5: Power Consumption Table Windows 2000/NT IDLE MODE

Power	800 MHz 256 MB Memory	933 MHz 256 MB Memory	1066 MHz 256 MB Memory	1200 MHz 256 MB Memory
Core Voltage	1.15 V	1.15 V	1.4 V	1.4 V
5 V	3.2 W	5.7 W	3.6 W	7.2 W
3.3 V	6.6 W	6.6 W	6.6 W	6.6 W
Total	9.8 W	12.3 W	10.2 W	13.8 W

Note ...

The above values were measured with no application started and without keyboard.

Table 1-6: Power Consumption DOS (without keyboard)

Power	800 MHz 256 MB Memory	933 MHz 256 MB Memory	1066 MHz 256 MB Memory	1200 MHz 256 MB Memory
Core Voltage	1.15 V	1.15 V	1.4 V	1.4 V
5V	6.9 W	5.9 W	10.7 W	15.5 W
3.3V	6.9 W	7.1 W	7.4 W	7.2 W
Total	13.8 W	13 W	18.1 W	22.7 W

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Table 1-7: Power Consumption Windows 2000/NT 100% CPU Usage

Power	800 MHz 256 MB Memory	933 MHz 256 MB Memory	1066 MHz 256 MB Memory	1200 MHz 256 MB Memory
Core Voltage	1.15 V	1.15 V	1.4 V	1.4 V
5 V	9.3 W	9.0 W	15.7 W	23.0 W
3.3 V	6.6 W	6.6 W	6.6 W	6.6 W
Total	15.9 W	15.6 W	22.3 W	29.6 W

Note ...

The above values are with Windows/NT running with 100% CPU usage, the INTEL HiPower tool started and without keyboard.

Analysis indicates that real applications does not reach the maximum possible power consumption of the HiPower tool, the maximum power consumption is 20 - 30% lower than the measured value.

Table 1-8: Power Consumption for CP303 Accessories

Module	Power 5V	Power 3.3V
Keyboard	100 mW	--
SODIMM module	--	500 mW - 1.5 W
CompactFlash	--	100 mW - 300 mW

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1.9.4 Temperature Range

The CP303 is one of the first CompactPCI boards capable of operating over the extended temperature range from -40°C up to +85°C. All onboard components are specially selected for the higher temperature range. For the higher temperatures the desktop processors are not suitable, because the power consumption is higher and the allowable junction temperature is lower. The only suitable processors are those within the Intel® Pentium® III Processor-M™ processor family. These processors are produced with the new 0.13-micron process and have lower power consumption and support higher junction temperatures (100°C).

1.9.4.1 Temperature Range and Air Flow

These values have been measured with typical applications under DOS and Windows 2000. In worst case situations the values and the temperature range must be reduced accordingly. For all situations the maximum junction temperature of the Intel® Pentium® III Processor-M™ processor must be below 100°C. This temperature value can be measured with the onboard remote temperature sensor. In instances of overtemperature the hardware monitor will reduce the processor clock to reduce power consumption.

Warning!

The temperature ranges detailed above assume that any appended hard disk is capable of operating at these temperatures. The user must ensure that any appended hard disk can function at the operating temperatures expected.

Table 1-9: Typical Temperature Range and Required Air Flow

Heat Sink Version	Range	800 MHz	933 MHz	1066 MHz	1200 MHz
4HP	0°C to 60°C	0 m/s	0.5 m/s	0.8 m/s	1 m/s
	-25°C to 75°C	0.2 m/s	0.8 m/s	1.2 m/s	--
	-40°C to 85°C	1 m/s	--	--	--

0 m/s air flow means standard convection cooling with the board in an upright position. An airflow of 1 - 1.2 m/s is a typical value for a standard *Kontron* ASM 4 rack (3U CompactPCI rack with 1U cooling fans). For other racks or housings the available airflow will differ. The maximum ambient temperature must be recalculated and/or measured for such environments. For the calculation of the maximum ambient temperature the processor junction temperature must never exceed 100°C. The maximum heat sink temperature depends on the physical characteristics of the heat sink and thermal connection to the processor. To ensure that the heat sink temperature does not exceed its limits an airflow may be needed for a given ambient temperature. Heat sink temperature is measured at the top of the heat sink base, closest to the processor.

Warning!

It is the responsibility of the end user to ensure that the processor junction temperate never exceeds 100°C in order to protect the board against overheating. Permanent overheating can damage the board.

If the temperature on the processor junction is greater than 100°C the maximum ambient temperature must be reduced or an external airflow must be provided by means of an additional fan.

Note ...

The BIOS supports a temperature control function, If the temperature is too high, the sensors automatically reduce the CPU clock frequency, depending on the mode chosen in the BIOS setup.

1.9.5 Storage Temperatures

- Storage temperature without hard disk –55°C to +85°C
- Storage temperature with hard disk –40°C to +65°C
- Humidity 93% RH at 40 °C, non-condensing

1.10 Applied Standards

The *Kontron Modular Computers'* CompactPCI systems comply with the requirements of the following standards:

Table 1-10: Applied Standards

COMPLIANCE	TYPE	STANDARD	Test Level (Ruggedized Version)
CE	Emission	EN55022 EN61000-6-3	--
	Immission	EN55024 EN61000-6-2	--
	Electrical Safety	EN60950	--
Mechanical	Mechanical Dimensions	IEEE 1101.10	--
Environmental Aspects	Vibration (Sinusoidal)	IEC68-2-6	2g/12-300Hz/10 acceleration / frequency range / test cycles
	Random Vibration (Broadband)	IEC68-2-64 (3U boards)	20-500Hz,0.1g²/500-2000Hz, 0.01g²/7g rms/3/30min frequency range1 / frequency range2 / acceleration / cycle / duration
	Permanent Shock	IEC68-2-29	15g/11ms/3000/1s peak acceleration / shock duration half sine / number of shocks / recovery time
	Single Shock	IEC68-2-27	30g/9ms/18/5s peak acceleration / shock duration / number of shocks / recovery time in sec.
	Climatic Humidity	IEC60068-2-78	93% RH at 40°C, non-condensing

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1.11 Related Publications

The following publications contain information relating to this product.

Table 1-11: Related Publications

PRODUCT	PUBLICATION
CompactPCI Systems and Boards	CompactPCI Specification 2.0, Rev. 3.0
	Hot Swap Specification PICMG 2.1
	Kontron Modular Computers' CompactPCI System Manual, ID 19954
CompactFlash Cards	CF+ and CompactFlash Specification Revision 1.4

1.12 Trademarks

- CompactPCI is a trademark of the PCI industrial Computers Manufacturers Group
- Ethernet is a registered trademark of Xerox Corporation
- IEEE is a registered trademark of the Institute of Electrical and Electronics Engineers Inc.
- VxWorks is a registered trademark of Wind River Systems Inc.
- OHCI-Lynx and TI are trademarks of Texas Instruments
- FireWire is a trademark of Apple Computer Inc.
- Intel is a trademark of Intel Corporation
- Processor-M™ is a trademark of Intel Corporation
- Microsoft is a trademark of the Microsoft Corporation
- Other trademarks are the property of their respective owners

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Chapter 2

Functional Description

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2. Functional Description

2.1 CPU, Memory and Chipset

2.1.1 CPU

The CP303 supports the Intel® Pentium® III Processor-M™ processor family up to 1200 MHz. The Intel® Pentium® III Processor-M™ microprocessors offer exceptional performance coupled with low power consumption. This processor is based on the same core as existing Intel® mobile processors. Key performance include Internet Streaming SIMD instructions and processor system bus speed of 133 MHz. These features are offered in a 479 Micro-FCBGA package.

The processor includes an integrated on-die 512KB 8-way set associative level-two (L2) cache. The L2 cache implements the Advanced Transfer Cache Architecture with a 256-bit wide bus. The processor also includes a 16 KB level one (L1) instruction cache and 16 KB L1 data cache. These cache arrays run at the full speed of the processor core. Memory is cacheable for 64 GB of addressable memory space, allowing significant headroom for desktop systems.

The processor speed is automatically selected and the onboard voltage regulator is automatically programmed by the processor's VID pins to provide the required voltage.

The CP303 is available with a variety of Intel® processors as set out in the following table.

Table 2-1: Supported Intel Processors on the CP303

Processor	Speed	L2 Cache	Core Voltage	Processor Side Bus
Pentium® III Mobile	800 MHz	512 kB	1.15 core voltage*	133 MHz
Pentium® III Mobile	933 MHz	512 kB	1.15 core voltage*	133 MHz
Pentium® III Mobile	1066 MHz	512 kB	1.4 core voltage	133 MHz
Pentium® III Mobile	1200 MHz	512 kB	1.4 core voltage	133 MHz
Celeron® ultra-low power	650 MHz	256 kB	1.15 core voltage	100 MHz
Plus future Intel® Pentium® III Processor-M™ microprocessors with 133 MHz processor side bus				

Note ...

Only the low core voltage versions are able to run in the extended temperature range because of the lower power dissipation.

2.1.2 Memory

The CP303 has two locations for installing memory; up to 256 MB may be soldered and a further 256 MB may be added by means of the onboard SODIMM socket. The board supports a maximum of 512 MB. All installed memory will be automatically detected, so there is no need to set any jumpers. All PC/133 compliant SDRAMs on 144-pin SODIMMs are supported by the CP303 board.

Table 2-2: Memory Options Utilizing SODIMM Sockets

Onboard	SODIMM	Total
128 MB	--	128 MB
128 MB	128 MB	256 MB
128 MB	256 MB	384 MB
256 MB *	--	256 MB
256 MB *	128 MB	384 MB
256 MB *	256 MB	512 MB

All memory components and SODIMMs used with this board must comply with the following PC SDRAM specifications:

- PC SDRAM Specification PC133
- PC Serial Presence Detect Specification

Note ...

The memory options marked with a * are the standard product configuration.

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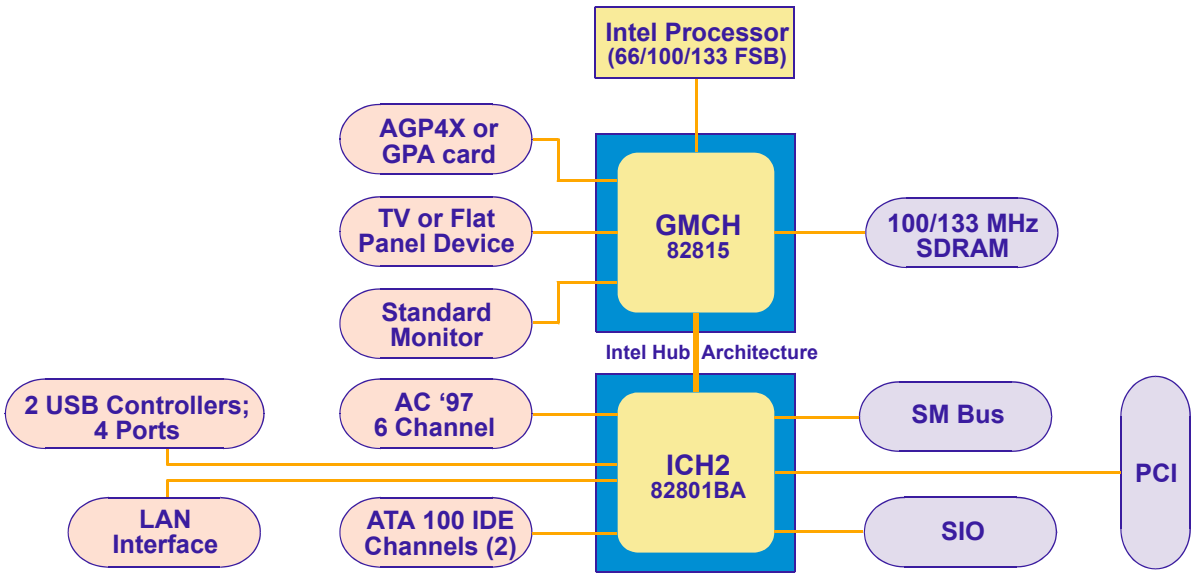
2.1.3 815-B0 Chipset Overview

The Intel® 815-B0 chipset consists of the following devices:

- 82815-B0 Graphics and Memory Controller Hub (GMCH) with Accelerated Hub Architecture (AHA) bus
- 82802 I/O Controller Hub 2 (ICH2) with AHA bus
- 82802 Firmware Hub (FWH)

The GMCH provides the processor interface for the Processor-M™ microprocessor, the memory bus, the AGP 4x bus in the case of an external graphics controller, and includes a high performance graphics accelerator. The ICH2 is a centralized controller for the boards' I/O peripherals, such as the PCI, USB, EIDE, LAN and AUDIO ports. The Firmware Hub FWH provides the non-volatile storage of the BIOS.

Figure 2-1: 815-B0 Chipset Functional Block Diagram



2.1.4 Graphics and Memory Controller Hub (815-B0)

The 815-B0 Graphics Memory Controller Hub (GMCH) is a highly integrated hub that provides the CPU interface (optimized for the Intel® Processor-M™), the SDRAM system memory interface, a hub link interface to the ICH2 and an AGP interface for an external VGA controller or internal graphics.

2.1.4.1 Graphics and Memory Controller Hub Feature Set

Host Interface

The 815-B0 is optimized for the Intel® Pentium® III Processor-M™ microprocessors. The chipset supports Processor Side Bus (PSB) frequency of 133 MHz using 1.25V AGTL signaling. Single ended AGTL termination is supported for single processor configurations. It supports 32 bit host addressing for decoding up to 4 GB memory address space.

System Memory Interface

The 815-B0 integrates a system memory SDRAM controller with a 64 bit wide interface without ECC. The chipset supports PC133 Single Data Rate (SDR) SDRAM for system memory.

AGP Interface

The 815-B0 supports 1.5 V AGP 4x devices with a max. data transfer of 1066 MB/s and sideband addressing. If the internal graphic controller is enabled the AGP port cannot be used. If an AGP card is installed in the system, the 815-B0 internal graphics will be disabled and the AGP controller will be enabled. The AGP is used in conjunction with the 8HP CP303-VGA1 board.

815-B0 Graphics Controller

The 815-B0 includes a highly integrated graphics accelerator and H/W Motion Compensation engines for software MPEG2 decoding delivering high performance 3D, 2D video capabilities. The internal graphics controller provides interfaces to a standard progressive scan monitor, TV-Out device, and TMDS transmitter. These interfaces are only active when running in internal graphics mode.

2.1.5 I/O Controller Hub ICH2

The ICH2 is a highly integrated multifunctional I/O Controller Hub that provides the interface to the PCI Bus and integrates many of the functions needed in today's PC platforms e.g. Ultra DMA 100/66/33 controller, USB host controller that supports USB 1.1, LPC interface, FWH Flash BIOS interface controller, LAN interface and an AC'97 digital controller. The ICH2 communicates with the host controller over a dedicated hub interface.

2.1.5.1 I/O Controller Hub Feature set

- PCI 2.2 interface with eight IRQ inputs
- Bus Master EIDE controller UltraDMA 100/66/33
- Two USB controller with up to four USB 1.1 ports
- Hub interface to 815-B0
- FWH interface
- LPC interface
- AC 97 2.1 interface
- Integrated LAN controller 82559 style
- RTC controller

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2.1.6 Interrupts

Two enhanced 8259-style interrupt controllers provide a total of fifteen interrupt inputs with features which include level and edge-triggered inputs, fixed and rotating priorities and individual input masking. Interrupt sources include: Counter/timers, serial I/O, RTC, keyboard/ mouse, printer, floppy disk, EIDE interfaces and four interrupt sources on the CompactPCI backplane.

2.2 Peripherals

The following standard peripherals are available on the CP303 board:

2.2.1 Timer

- Real-Time Clock

  The ICH2 contains a MC146818A-compatible real-time clock with 256 bytes of battery-backed RAM.

  The real-time clock performs time-keeping functions and includes 256 bytes of general purpose battery-backed CMOS RAM. Features include an alarm function, programmable periodic interrupt and a 100-year calendar. All battery-backed CMOS RAM data remains stored in an additional EEPROM. This prevents data loss.

- Counter/Timer

  Three 8254-style counter/timers are included on the CP303 as defined for the PC/ AT.

2.2.2 Watchdog Timer

A watchdog timer is provided, which forces either an IRQ5, NMI, or Reset condition (configurable in the watchdog register). The watchdog time can be programmed in 12 steps ranging from 125 msec up to 256 seconds. If the watchdog timer is enabled, it cannot be stopped.

2.2.3 Battery

The CP303 is provided with a 3.0V “coin cell” lithium battery for the RTC.

To replace the battery please proceed as follows:

- Turn off power
- Remove the battery
- Place the new battery in the socket.
- Make sure that you insert the battery the right way round. The plus pole must be on the top!

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer. Suitable batteries include the VARTA CR2025 and
PANASONIC BR2020

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Note ...

Care must be taken to ensure that the battery is correctly replaced.

The battery should be replaced only with an identical or equivalent type recommended by the manufacturer.

Dispose of used batteries according to the manufacturer's instructions.

The typical life expectancy of a 170 mAh battery (VARTA CR2025) is 5 - 6 years with an average on-time of 8 hours per working day at an operating temperature of 30°C. However, this typical value varies considerably because the life expectancy is dependent on the operating temperature and the standby time (shutdown time) of the system in which it operates.
To ensure that the lifetime of the battery has not been exceeded it is recommended to exchange the battery after 4 - 5 years.

2.2.4 Reset

The CP303 is automatically reset by a precision voltage monitoring circuit that detects a drop in voltage below the acceptable operating limit of 4.725 V for the 5 V line and below 3.0 V for the 3.3 V line, or in the event of a power failure of the DC/DC converter. Other reset sources include the watchdog timer and the local push-button switch. The CP303 responds to any of these sources by initializing local peripherals.

A reset will be generated by the following conditions:

- +5 V supply falls below 4.75 V.
- +3.3 V supply falls below 3.0 V.
- +1.8 V supply falls below 1.5 V
- Power failure of the DC/DC converter for the processor
- Pushbutton "RESET" pressed (only on 8HP)
- Watchdog overflow
- CompactPCI backplane PRST input

2.2.5 SMBus Devices

The CP303 provides a System Management Bus (SMBus) for access to several system monitoring and configuration functions. The SMBus consists of a two-wire I2C bus interface. The following table describes the function and address of every onboard SMBus device.

Table 2-3: SMBus Device Addresses

Device	SMB Address
Temperature sensor MAX1617	0011000Xb
Hardware Monitor LM81	0101100Xb
EEPROM	1010XXXXb

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2.2.6 Thermal Management / System Monitoring

The LM81 can be used to monitor several critical hardware parameters of the system, including power supply voltages, fan speeds and temperatures; all of which are very important for the proper operation and stability of a high-end computer system. The LM81 provides an I2C™ serial bus interface.

The voltages of the onboard power supply +12 V, -12 V, +5 V, +3.3 V, +1.5 V and the battery voltage are supervised. Two fan tachometer outputs can be measured using the LM81's FAN1 and FAN2 inputs.

The integrated MAX1617 temperature sensors monitor the CPU temperature and the ambient temperature around the CPU to make sure that the system is operating at a safe temperature level. If the temperature is too high, the sensors automatically reduces the CPU clock frequency, depending on the mode chosen in the BIOS set. Thermal management operations are controlled by the ICH2 hub and settings are available in the BIOS.

2.2.7 Serial EEPROM

A serial EEPROM is provided, organized into 4 blocks with 256 bytes per block (24LC08). This EEPROM is connected to the I2C™ bus provided by the ICH2.

Table 2-4: EEPROM Address Map

Address	Function
1010000xb	Reserved
1010001xb	Reserved
1010010xb	Reserved
1010011xb	Reserved
1010100xb	VxWorks parameter
1010101xb	Free for user purposes
1010110xb	Free for user purposes
1010111xb	CMOS backup and Board serial number

Warning!

It is strongly recommended that users access only the two free EEPROM banks.

2.2.8 FLASH Memory

There are three flash devices available as described below, one for the BIOS, one onboard flash and one CompactFlash socket.

2.2.8.1 BIOS FLASH (Firmware Hub)

For simple BIOS update a standard onboard 512 kB Firmware Hub device in a 40-pin TSSOP package is used. The Firmware Hub (FWH) interface consists of a 5-signal communication interface used to control the operation of the device in a system environment. The buffers for this interface were designed to be PCI compliant. The FWH interface is equipped to operate at 33 MHz, synchronous with the PCI bus.

The FWH stores both the system BIOS and video BIOS.

It can be updated as new versions of the BIOS become available. You may easily upgrade your BIOS using the AWARD *awdflash* utility.

2.2.8.2 User FLASH

For small flash extensions an additional 512 kB Firmware hub flash memory is available. Due to the new chipset generation with the Low Pin Count interface the flash block is not mapped in the first 1 MB memory block as on the BX based CPU boards, it is mapped in the extended memory area, e.g. 0xFFF00000-0xFFF7FFFF.

2.2.8.3 Dual BIOS

Dual BIOS means that there are two chips for the BIOS on the CP303 board (BIOS Flash and the User Flash). One chip is intended to be a backup in case the other gets corrupted. These chips are soldered to the board.

If the primary BIOS is corrupted due to physical damage or a faulty flash upgrade, it must be set the solder jumper J2 and the system switch over to the secondary chip and boots with default settings.

Note ...

The Dual BIOS feature cannot be used if the second Flash chip is used for VxWorks

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2.2.8.4 CompactFlash Socket

To enable flexible flash extension a CompactFlash (CF) type II socket, CON9, is available.

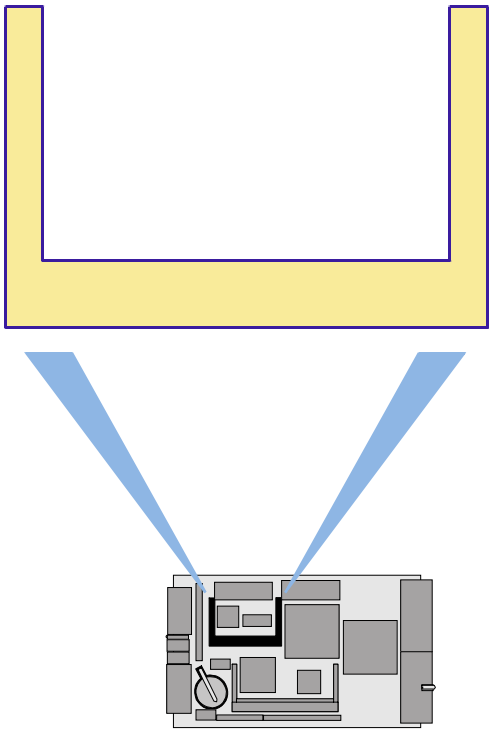
CF is a very small removable mass storage device. It provides true IDE functionality compatible with the 16 bit ATA/ATAPI-4 interface. CF cards are also available for data storage using the Microdrive hard disk from IBM with up to 1 GB capacity.

The board supports both CF types (type I and type II). CompactFlash is available in both CF type I and CF type II cards. The IBM Microdrive is a CF type II card..

Note ...

The CP303 does not support DMA-capable CompactFlash devices.

Figure 2-2: CompactFlash Socket Connector CON9



Note ...

If the AGP 4x extension connector is equipped, the onboard CompactFlash socket cannot be used.

The following table indicates the pinout of the CompactFlash Connector CON9.

Table 2-5: CompactFlash Connector CON9 Pinout

Pin Number	Signal	Function	In/Out
1	GND	Ground signal	--
2	D03	Data 3	In/Out
3	D04	Data 4	In/Out
4	D05	Data 5	In/Out
5	D06	Data 6	In/Out
6	D07	Data 7	In/Out
7	IDE_CS0	Chip select 0	Out
8	GND (A10)	--	--
9	GND (ATASEL)	--	--
10	GND (A09)	--	--
11	GND (A08)	--	--
12	GND (A07)	--	--
13	3.3 V	3.3 V power	--
14	GND (A06)	--	--
15	GND (A05)	--	--
16	GND (A04)	--	--
17	GND (A03)	--	--
18	A02	Address 2	Out
19	A01	Address 1	Out
20	A00	Address 0	Out
21	D00	Data 0	In/Out
22	D01	Data 1	In/Out
23	D02	Data 2	In/Out
24	NC (IOCS16)	--	--
25	NC (CD2)	--	--
26	NC (CD1)	--	--
27	D11	Data 11	In/Out
28	D12	Data 12	In/Out
29	D13	Data 13	In/Out
30	D14	Data 14	In/Out
31	D15	Data 15	In/Out
32	IDE_CS1	Chip select 1	Out
33	NC (VS1)	--	--
34	DIOR	I/O read	Out
35	DIOW	I/O write	Out
36	3.3 V (WE)	3.3 V power	--
37	INTRQ	Interrupt	In
38	3.3 V	3.3 V power	--
39	CSEL (GND pullup)	Master/Slave	Out
40	NC (VS2)	--	--
41	Reset	Reset	Out
42	IORDY	I/O ready	In
43	INPACK	Acknowledge	Out
44	3.3 V (REG)	3.3 V power	--
45	NC (ACTIVE)	--	--
46	NC (PDIAG)	--	--
47	D08	Data 08	In/Out
48	D09	Data 09	In/Out
49	D10	Data 10	In/Out
50	GND	--	--

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2.2.9 PCI-to-PCI Bridge

The Intel® 21154 bridge is a 64-bit 33 MHz PCI-to-PCI bridge device. It supports up to seven CompactPCI loads through a passive backplane.

The 21154 is a second generation PCI-to-PCI bridge and is fully compliant with the PCI Local Bus Specification Rev. 2.1. The 64-bit interface interoperates transparently with either 64-bit or 32-bit devices.

The PCI-to-PCI bridge allows the primary and secondary PCI bus to operate concurrently. A master and target on the same PCI bus can communicate while the other PCI bus is busy.

2.3 Board Interfaces

2.3.1 General Purpose LED Output

The CP303 provides two software programmable GP LED. After the reset the default configuration for the two front LEDs is the Overtemperature and Watchdog status. The LEDs can be configured via two onboard registers. For more information please see Chapter 4.

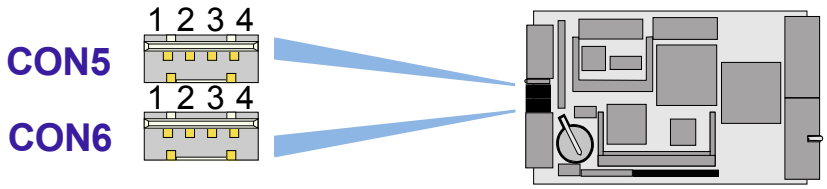
The LED control logic remains in the state until the next system reset.

2.3.2 USB Interfaces

There are two independent USB ports on the CP303 board each with a maximum transfer rate of 12 Mbit provided for connecting USB devices. One USB peripheral may be connected to each port. To connect more than two USB devices an external hub is required.

The USB power supply is protected by a self-resettable 500 mA fuse.

Figure 2-3: USB Connectors CON5 and CON6



Two USB interfaces with a maximum transfer rate of 2x12 Mbit are provided. Two USB peripherals may be connected to this port.

2.3.2.1 USB Connectors CON5 and CON6 Pinout

The CP303 has two USB interfaces implemented on a 4-pin connector with the following pinout:

Table 2-6: USB Connectors CON5 and CON6 Pinout

Pin Number	Signal	Function	In/Out
1	VCC	VCC signal	--
2	UV0-	Differential USB-	--
3	UV0+	Differential USB+	--
4	GND	GND signal	--

Note ...

The USB power supply to each USB connector is protected with a fuse (500 mA) and all the signal lines are EMI-filtered.

2.3.3 Graphics Controller

The 815-B0 includes a highly integrated graphics accelerator delivering high performance 3D, 2D video capabilities. The internal graphics controller provides interfaces to a standard progressive scan monitor. This interface is only active when running in internal graphics mode.

Integrated 2D/3D Graphics:

- 3-D hyperpipelined architecture
- Full 2-D hardware acceleration
- Intel® i815e D.V.M. Technology graphics core
- Integrated 230 Mhz DAC
- Resolution up to 1280 x 1024 with 16 M colors
- Integrated H/W Motion Compensation engines for software MPEG2 decode

2.3.3.1 Video Memory Usage

The 815-B0 chipset supports the new Dynamic Video Memory Technology (D.V.M.T.). This new technology ensures the most efficient use of all available memory for maximum 3D graphics performance. D.V.M.T. dynamically responds to application requirements allocating display and texturing memory resources as required.

The operating system requires up to 1 MB of system memory to support legacy VGA. System properties will display up to 1MB less than physical system memory available to the operating system.

The graphics driver for the Intel® 815-B0 configuration will request up to 6 MB of memory from the OS to implement a maximum 1024*768 screen resolution, 2 MB for a command buffer and 4 MB is required for Z-Buffering. When the 3D application is closed, the OS will reallocate system memory back for generic use.

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2.3.3.2 Video Resolution

The GMCH supports a wide range of resolutions, color depths, and refresh rates via a programmable dot clock that has a maximum frequency of 230 MHz.

Table 2-7: Partial List of Display Modes Supported

Resolution	Bits per Pixel (frequency in Hz)		
	8-bit indexed	16-bit	24-bit
320x200	70	70	70
320x240	70	70	70
352x480	70	70	70
352x576	70	70	70
400x300	70	70	70
512x384	70	70	70
640x400	70	70	70
640x480	60,70,72,75,85	60,70,72,75,85	60,70,72,75,85
720x480	75,85	75,85	75,85
720x576	60,75,85	60,75,85	60,75,85
800x600	60,70,72,75,85	60,70,72,75,85	60,70,72,75,85
1024x768	60,70,72,75,85	60,70,72,75,85	60,70,72,75,85
1152x864	60,70,72,75,85	60,70,72,75,85	60,70,72,75,85
1280x720	60,75,85	60,75,85	60,75,85
1280x960	60,75,85	60,75,85	60,75,85
1280x1024	60,70,72,75,85	60,70,72,75,85	60,70,75,85
1600x900	60,75,85	60,75,85	--
1600x1200	60,70,72,75	--	--

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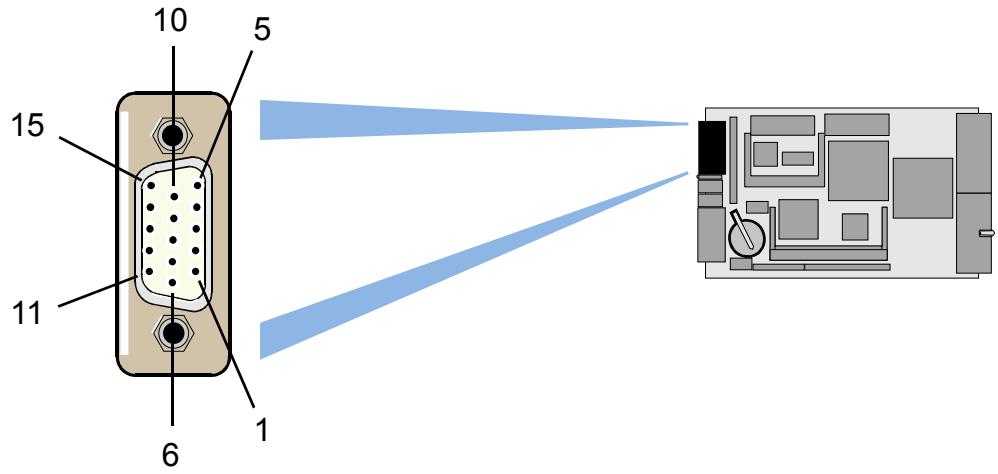
2.3.3.3 CRT Interface and Connector CON4

Figure 2-4: D-SUB CRT Connector CON4



The 15-pin female connector CON4 is used to connect a CRT monitor to the CP303 board.

Table 2-8: CRT Connector CON4 Pinout

Pin Number	Signal	Function	In/Out
1	Red	Red video signal output	Out
2	Green	Green video signal output	Out
3	Blue	Blue video signal output	Out
13	Hsync	Horizontal sync.	TTL out
14	Vsync	Vertical sync.	TTL out
12	Sdata	I2C™ data	In/Out
15	Sclk	I2C™ clock	Out
9	VCC	Power +5V 200 mA, no fuse protection	Out
5,6,7,8,10	GND	Signal ground	--
4,11	Free	--	--

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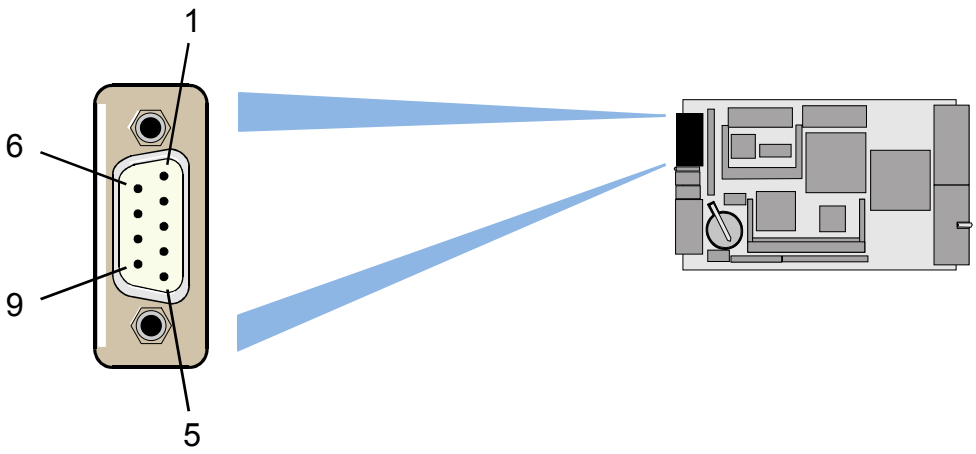
2.3.4 Universal Serial Ports (UART)

2.3.4.1 Serial Port Interface COM1

Figure 2-5: PC-Compatible D-SUB Serial Connector CON3 (COM1)



A PC-compatible RS232 serial port is available with 5V charge-pump technology eliminating the need for a +12V and -12V supply. The COM port, which is fully compatible with the 16550 controller, includes a complete set of handshaking and modem control signals, maskable interrupt generation and data transfer of up to 460.8 kB/s.

The Serial Port COM1 can be enabled/disabled under SW control. Selection can be made inside the BIOS or via the rear I/O configuration register. The standard software configuration is front I/O.

Note ...

The CP303 is delivered configured either with the COM or VGA interface and cannot subsequently be reconfigured.

2.3.4.2 Serial Port Connector CON3 (COM1) Pinout

Table 2-9: Serial Port Connector CON3 (COM1) Pinout

Pin Number	Signal	Function	In/Out
1	DCD	DCD Data carrier detect	In
2	RXD	RXD Receive data	In
3	TXD	TXD Transmit data	Out
4	DTR	DTR Data terminal ready	Out
5	GND	GND Signal ground	--
6	DSR	DSR Data send request	In
7	RTS	RTS Request to send	Out
8	CTS	CTS Clear to send	In
9	RIN	RI Ring indicator	In

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2.3.4.3 Serial Port Interface COM2

The COM2 port can be used only on the rear I/O interface.

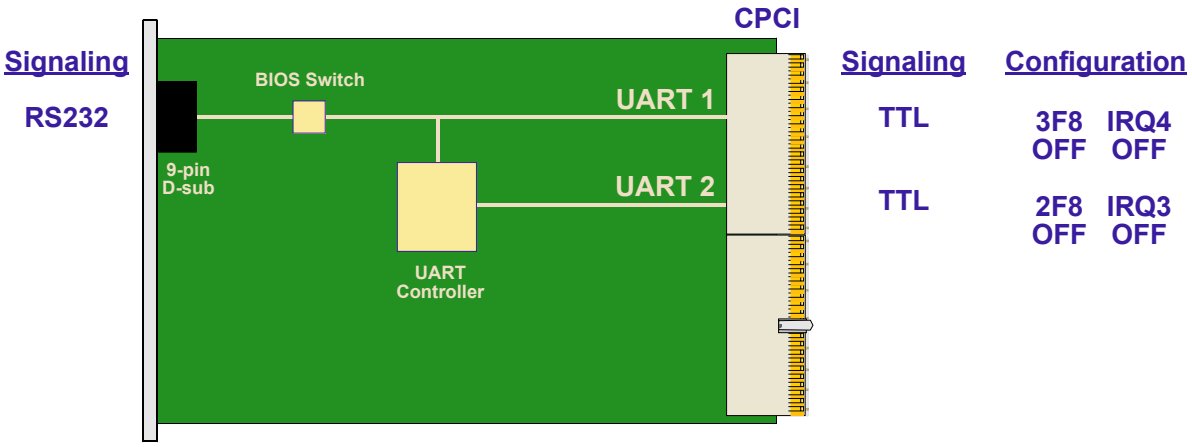
Table 2-10: COM Port Configuration Matrix

Board	Rear I/O Variant	UART1	UART2	UART3	UART4
4HP CRT board	No	--	--	--	--
4HP CRT board	Yes	Rear I/O COM1	Rear I/O COM2	--	--
4HP serial board	No	Front COM1 * note 1	--	--	--
8HP VGA board Multimedia	No	Front COM1 * note 1	--	--	--
8HP board with CP303-IDE 1	No	-- * note 3	-- *note 3	Front I/O COM1 or COM3 *note 2	Front I/O COM2 or COM4 *note 2
8HP board with CP303-IDE 1	Yes	Rear I/O COM1	Rear I/O COM2	Front I/O COM3	Front I/O COM4

- note 1, ensure that the line driver chips are disabled on the rear I/O board for UART1, if the channel is used via front I/O. Enabling of the UART1 front I/O lines is accomplished via the BIOS
- note 2, selection of UART3 / UART4 settings is made via the BIOS
- note 3, UART1 / UART2 are disabled via the BIOS settings

2.3.4.4 Serial Port Configuration

Figure 2-6: Serial Port Configuration Diagram



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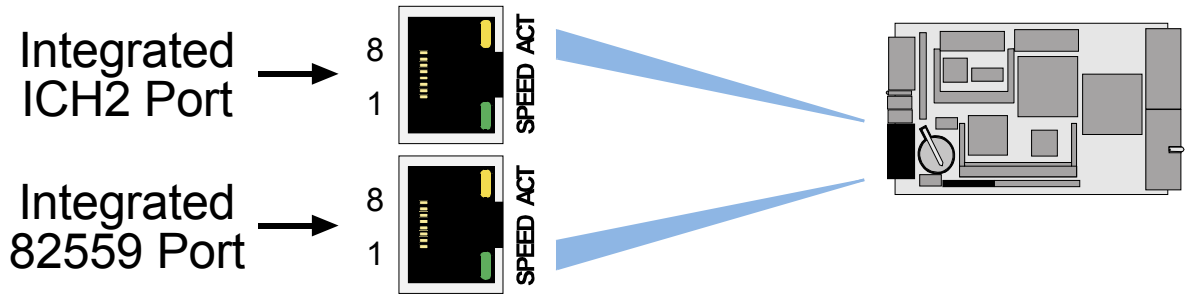
2.3.5 Fast Ethernet

The CP303 board includes two 10BASE-T/100BASE-TX ethernet ports by Intel®, ICH2 chipset, integrated LAN controller and an Intel® 82559 Fast Ethernet PCI Bus Controller. The controller contains two receive and transmit FIFO buffers that prevent data overruns or underruns while waiting for access to the PCI bus.

Two LEDs monitor network conditions. The Boot from LAN feature is supported, for details please refer to section 5.5, BIOS Features Setup, in chapter 5.

Figure 2-7: Dual Fast Ethernet Connector CON7



The Ethernet connectors are realized as RJ45 twisted-pair connectors. The interfaces provides automatic detection and switching between 10Base-T and 100Base-TX data transmission. The two Ethernet channels may be configured via the BIOS setting or the rear I/O Configuration Register for front I/O or rear I/O. The standard software configuration is front I/O.

2.3.5.1 RJ45 Connector CON7 Pinouts

The CON7 connector supplies the 10Base-TX/100Base-TX interfaces to the Ethernet controller.

Table 2-11: RJ45 Connector CON7 Pinout

Pin Number	Signal	Function	In/Out
1	TX+	Transmit +	Out
2	TX-	Transmit -	Out
3	RX+	Receive +	In
4	NC	--	--
5	NC	--	--
6	RX-	Receive -	In
7	NC	--	--
8	NC	--	--

2.3.6 Ethernet LED Status

Yellow: ACT: This LED monitors network connection and activity. The LED lights up when network packets are sent or received through the RJ45 port. When this LED is not lit it means that either the computer is not sending or receiving network data or that the cable connection is faulty.

Green: SPEED: This LED lights up to indicate a successful 100Base-TX connection. When not lit the connection is operating at 10Base-T.

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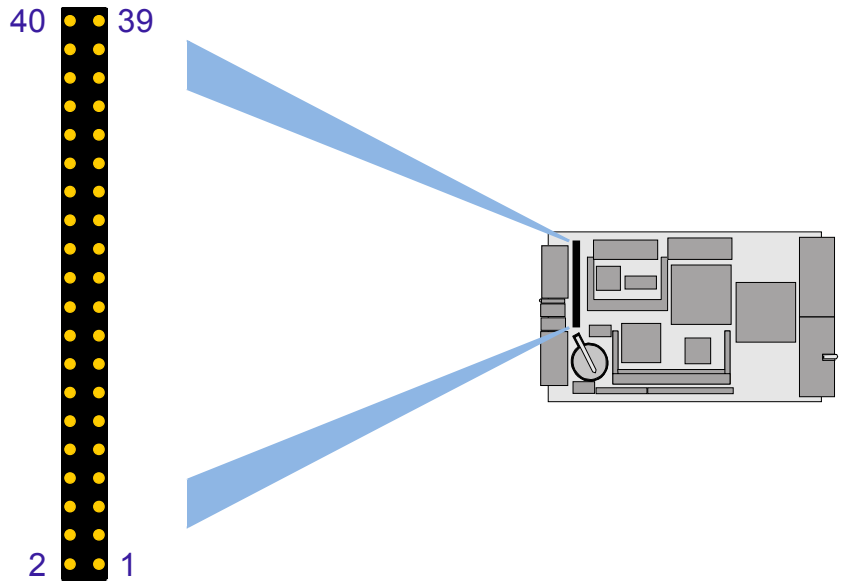
2.3.7 EIDE Interface

Figure 2-8: EIDE Interface Connector CON10



The IDE interface supports the following modes:

- Programmed I/O (PIO): CPU controls data transfer
- 8237-style DMA: DMA offloads the CPU, supporting transfer rates of up to 16 MB/sec
- Ultra DMA: DMA protocol on IDE bus supporting host and target throttling and transfer rates of up to 33 MB/sec
- ATA-66: DMA protocol on IDE bus supporting host and target throttling and transfer rates of up to 66 MB/sec. ATA-66 protocol is similar to Ultra DMA and is device driver compatible.
- ATA-100: DMA protocol on IDE bus allows host and target throttling. The ICH2 ATA-100 logic can achieve read transfer rates up to 100 MB/sec and write transfer rates up to 88 MB/sec.

There are two independent EIDE ports available. The primary port is connected to the CompactFlash socket. The secondary EIDE interface is a 40-pin, 2-row male connector AT standard interface for an EIDE hard disk.

The secondary EIDE interface provides support for two devices (one master and one slave). All hard disks can be used in cylinder head sector (CHS) mode with the BIOS also supporting the logical block addressing (LBA) mode.

Note ...

The secondary EIDE interface supports a maximum of two devices connected in the master-slave mode. To configure the first as a master disk and the second as a slave disk, please refer to the hard disk manufacturer's documentation.

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Note ...

ATA-66 and ATA-100 are faster timings and require a specialized cable which has additional grounding wires to reduce reflections, noise, and inductive coupling. This cable will also support all legacy IDE drives.

The blue end of the ATA-100 cable must connect to the motherboard, the gray connector to the UltraDMA /100 slave device and the black connector to the UltraDMA/100 master device.

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2.3.7.1 CON10 (Secondary EIDE Interface) Pinout

The following table sets out the pinout of the CON10 connector, giving the corresponding signal names. The maximum length of cable that may be used is 35 cm.

Table 2-12: CON10 (Secondary EIDE) Pinout

Pin Number	Signal	Function	In/Out
1	IDERESET	Reset HD	Out
2	GND	Ground signal	--
3	HD7	HD data 7	In/Out
4	HD8	HD data 8	In/Out
5	HD6	HD data 6	In/Out
6	HD9	HD data 9	In/Out
7	HD5	HD data 5	In/Out
8	HD10	HD data 10	In/Out
9	HD4	HD data 4	In/Out
10	HD11	HD data 11	In/Out
11	HD3	HD data 3	In/Out
12	HD12	HD data 12	In/Out
13	HD2	HD data 2	In/Out
14	HD13	HD data 13	In/Out
15	HD1	HD data 1	In/Out
16	HD14	HD data 14	In/Out
17	HD0	HD data 0	In/Out
18	HD15	HD data 15	In/Out
19	GND	Ground signal	--
20	N/C	--	--
21	IDEDRQ	DMA request	In
22	GND	Ground signal	--
23	IOW	I/O write	Out
24	GND	Ground signal	--
25	IOR	I/O read	Out
26	GND	Ground signal	--
27	IOCHRDY	I/O channel ready	In
28	GND	Ground signal	--
29	IDEDACKA	DMA Ack	Out
30	GND	Ground signal	--
31	IDEIRQ	Interrupt request	In
32	N/C	--	--
33	A1	Address 1	Out
34	ATA66	Detect ATA66	In
35	A0	Address 0	Out
36	A2	Address 2	Out
37	HCS0	HD select 0	Out
38	HCS1	HD select 1	Out
39	LED	LED driving	In
40	GND	Ground signal	--

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2.3.8 CompactPCI Bus Interface

The complete CompactPCI connector configuration comprises two connectors named J1 and J2

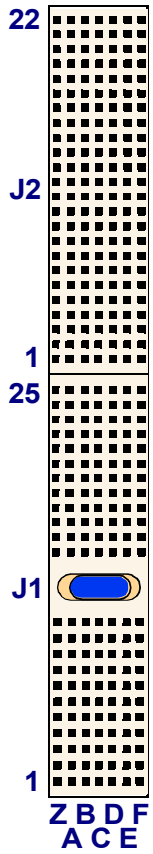
Their function is as follows:

- J1/J2: 64-bit CompactPCI interface with PCI bus signals, arbitration, clock and power
- J2 has optional rear I/O interface functionality.

The board is capable of driving up to seven CompactPCI slots, with individual arbitration and clock signals. In addition to standard CompactPCI system functionality, the CP303 also supports hot swap capability which means that hot swappable boards can be removed from or installed in the system whilst it is running.

The CP303 is designed for a CompactPCI bus architecture. The CompactPCI standard is electrically identical to the PCI local bus. However, these systems are enhanced to operate in rugged industrial environments and to support multiple slots.

Figure 2-9: CPCI Connectors J1/J2



2.3.8.1 CompactPCI Connector Keying

CompactPCI connectors support guide lugs to ensure a correct polarized mating. A proper mating is further assured by the use of color coded keys for 3.3V and 5V operation.

Color coded keys prevent inadvertent installation of a 5V peripheral board into a 3.3V slot. The CP303 board is a 5V version. Backplane connectors are always keyed according to the signaling (VIO) level. Coding key colors are defined as follows:

Table 2-13: Coding Key Colors

Signaling Voltage	Key Color
3.3V	Cadmium Yellow
5V	Brilliant Blue
Universal board (5V and 3.3V)	None

The default setting is indicated by italics.

2.3.8.2 CompactPCI Connectors CON1 and CON2 Pinouts

The CP303 is provided with two 2 mm x 2 mm pitch female CompactPCI bus connectors, J1 and J2.

Table 2-14: CompactPCI Bus Connector J1 (CON1) Pinout

Pin	Row A	Row B	Row C	Row D	Row E	Row F
25	5V	REQ64#	ENUM#	3.3V	5V	GND
24	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND
23	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
22	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
21	3.3V	AD[9]	AD[8]	M66EN#	C/BE[0]#	GND
20	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	3.3V	IPMB SCL	IPMB SDA	GND	PERR#	GND
16	DEVSEL	GND	V(I/O)	STOP#	LOCK#	GND
15	3.3V	FRAME#	IRDY#	GND	TRDY#	GND
12-14	Key Area					
11	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	C/BE[3]#	IDSEL (OPEN)	AD[23]	GND	AD[22]	GND
8	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	REQ0#	GND	3.3V	CLK0	AD[31]	GND
5	BRSVP1A5	BRSVP1B5	RST#	GND	GNT0	GND
4	IPMB PWR	GND	V(I/O)	INTP	INTS	GND
3	INTA#	INTB#	INTC#	5V	INTD#	GND
2	TCK	5V	TMS	TDO	TDI	GND
1	5V	-12V	TRST#	+12V	5V	GND

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Table 2-15: 64-bit CompactPCI Bus Connector J2 (CON2) Pinout

Pin	Row Z	Row A	Row B	Row C	Row D	Row E	Row F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	CLK6	GND	RSV	RSV	RSV	GND
20	GND	CLK5	GND	RSV	GND	RSV	GND
19	GND	GND	GND	RSV	RSV	RSV	GND
18	GND	RSV	RSV	RSV	GND	RSV	GND
17	GND	RSV	GND	PRST#	REQ6#	GNT6#	GND
16	GND	RSV	RSV	DEG#	GND	RSV	GND
15	GND	RSV	GND	FAL#	REQ5#	GNT5#	GND
14	GND	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND
13	GND	AD[38]	GND	V(I/O)	AD[37]	AD[36]	GND
12	GND	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND
11	GND	AD[45]	GND	V(I/O)	AD[44]	AD[43]	GND
10	GND	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND
9	GND	AD[52]	GND	V(I/O)	AD[51]	AD[50]	GND
8	GND	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND
7	GND	AD[59]	GND	V(I/O)	AD[58]	AD[57]	GND
6	GND	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND
5	GND	C/BE[5]#	GND	V(I/O)	C/BE[4]#	PAR64	GND
4	GND	V(I/O)	RSV	C/BE[7]#	GND	C/BE[6]#	GND
3	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	GND	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND

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2.3.9 Optional Rear I/O Interface on CompactPCI Connector J2

The CP303 board provides optional rear I/O connectivity for special compact systems. Some standard PC interfaces are implemented and assigned to the front panel and to the rear connector J2.

When the rear I/O module is used, the signals of some of the main board/front panel connectors are routed to the module interface. Thus the rear I/O module makes it much easier to remove the CPU in the rack as there is practically no cabling on the CPU board.

For this configuration two versions are available. One with 64-bit/33 MHz CompactPCI and reduced rear I/O functionality and one with 32-bit/33 MHz and some rear I/O peripherals.

For the system rear I/O feature a special backplane is necessary. The CP303 with rear I/O is compatible with all standard CompactPCI passive backplanes with rear I/O support on the system slot.

The CP303 rear I/O provides the following interfaces (all signals are available on J2 only when the board is ordered for rear I/O functionality):

The two versions of the board available come with the following features:

Version 1 (standard version)

- 32-bit CompactPCI and rear I/O
- 32-bit/33 MHz CompactPCI interface
- Two USB ports
- Two Ethernet ports without LED
- Two COM ports (TTL level)
- CRT VGA port
- One fan control input
- One general purpose output
- Input for external backup battery

Version 2

- 64-bit CompactPCI and rear I/O
- 64-bit/33 MHz CompactPCI interface
- Two USB ports
- Two Ethernet ports without LED

Note ...

The pinout for one ethernet, USB, COM and VGA port is identical to the CP302 pinout

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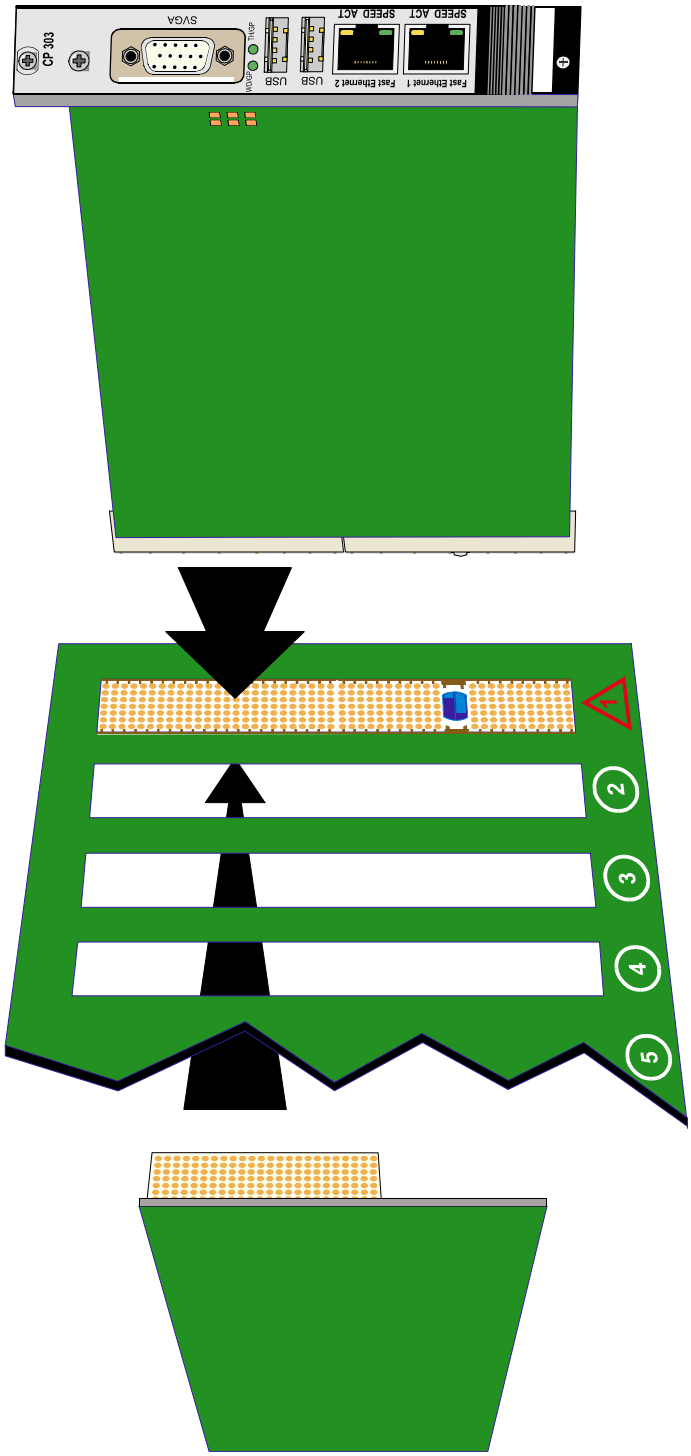
2.3.9.1 Rear I/O Configuration Illustration

Figure 2-10: CP303 Rear I/O Configuration



2.3.9.2 Optional Rear I/O Interface on CompactPCI Connector CON2

The CP303 conducts a wide range of I/O signals through the rear I/O connector J2.

Note ...

If the rear I/O feature is selected the CompactPCI interface is only 32-bit. For the 3U rear I/O a special backplane is necessary.

Warning!

To support the rear I/O feature a special backplane is necessary. Do not plug a rear I/O configured board in a non-system slot rear I/O backplane. This will damage the board. **This is of critical importance to the VGA interface; the blue signal of the VGA controller is connected to the CompactPCI connector J2 at pin C13. On the non-rear I/O version this pin is connected to the VI/O pin (default 5V) and on the rear I/O version this pin carries the VGA blue signal. If the rear I/O version is plugged into a non-system slot rear I/O backplane, the VGA controller will be damaged. (The blue signal is directly connected to the 5 V line).**

Table 2-16: Rear I/O CompactPCI Bus Connector J2 (CON2) Pinout

Pin	Z	A	B	C	D	E	F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	CLK6	GND	TDN1	RDN1	RDP1	GND
20	GND	CLK5	GND	TDP1	GND	VCC	GND
19	GND	GND	GND	RES	RES	+3.3V	GND
18	GND	RDN2	UV0-	UV3+	RTC Bat	+3.3V	GND
17	GND	RDP2	ROUT (GND)	PRST	REQ6	GNT6	GND
16	GND	TDN2	UV0+	DEG	GND	UV3-	GND
15	GND	TDP2	GOUT (GND)	FAL	REQ5	GNT5	GND
14	GND	2RIN	2DSR	2RTS	VSYNC (GND)	2CTS	GND
13	GND	2RXD	FANSENSE (GND)	BOUT (VIO)	2DTR	2DCD	GND
12	GND	1DSR	1RTS	1CTS	HSYNC (GND)	2TXD	GND
11	GND	1DTR	BOUT (GND)	--	1DCD	1RIN	GND
10	GND	--	--	1TXD	GND	1RXD	GND
9	GND	--	--	--	--	--	GND
8	GND	--	--	--	GND	--	GND
7	GND	--	--	--	--	--	GND
6	GND	--	--	--	GND	--	GND
5	GND	--	GND	--	--	GPLED	GND
4	GND	VIO	VCC	--	GND	--	GND
3	GND	CLK4	GND	GNT3	REQ4	GNT4	GND
2	GND	CLK2	CLK3	SSYSEN	GNT2	REQ3	GND
1	GND	CLK1	GND	REQ1	GNT1	REQ2	GND

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Legend for table on preceding page

Ethernet1

TDP1/TDN1	Transmit Differential Pair.
RDP1/RDN1	Receive Differential Pair.

Ethernet2

TDP2/TDN2	Transmit Differential Pair.
RDP2/RDN2	Receive Differential Pair.

USB ports

USB1+/-	USB data differential data signals
USB3+/-	USB data differential data signals

Serial Port 1

S1*	Serial port signals; TTL level

Serial Port 2

S2*	Serial port signals; TTL level

CONTROL Signals

FANSENSE	Schmitt Trigger fan tachometer inputs; TTL level

VGA CRT signals

ROUT	Red signal
GOUT	Green signal
BOUT*	Blue signal
HSYNC	Horizontal Sync.
VSYNC	Vertical Sync.

* Note that this signal (BOUT) appears twice in the rear I/O CompactPCI bus connector J2 pinout in order to provide compatibility with the CP302. Pin number B11 refers to the CP303 and C13 refers to the CP302. The default configuration is CP303 (B11).

Reserved Signals

RES	Reserved (leave open)

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2.3.9.3 Rear I/O Configuration

Rear I/O interfaces are only available on rear I/O versions of the board.

In order to implement the system rear I/O feature, a system slot rear I/O backplane is necessary. This backplane must comply with the CompactPCI Specification PICMG 2.0 R3.0, October 1999.

Warning!

If the board is ordered for 64-bit CompactPCI the rear I/O feature is **not supported**. The rear I/O jumpers and resistors must not be configured for rear I/O. The setting of the rear I/O jumpers and resistors **may result in damage to your board or system**.

To support the rear I/O feature a special backplane is necessary. Do not plug a rear I/O configured board in a non-system slot rear I/O backplane. This will damage the board. This is of critical importance to the VGA interface; the blue signal of the VGA controller is connected to the CompactPCI connector J2 at pin C13. On the non-rear I/O version this pin is connected to the VI/O pin (default 5V) and on the rear I/O version this pin carries the VGA blue signal. If the rear I/O version is plugged into a non-system slot rear I/O backplane, the VGA controller will be damaged. (The blue signal is directly connected to the 5 V line).

Ethernet Interface

Ethernet signals are available on the front RJ45 connector and on the rear I/O interface.

The combination of both front and rear I/O is not supported. Both Fast Ethernet channels are decoupled, but enabled separately. It is not possible to operate both the rear and front I/O at the same time. Switching over from front to rear I/O or vice versa is effected under BIOS control without the need to plug/unplug Ethernet cables.

VGA Interface

The VGA signals are available on J2 when the board is ordered for rear I/O configuration. In this configuration both interfaces are active. The 75 ohm termination resistor for the red, green and blue video signals are equipped on the CP303.

Note ...

Both VGA ports are electrically identical and not separated. Do not connect devices at both connectors (front I/O and rear I/O) at the same time. Doing so will result in poor signal quality.

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Warning!

To support the rear I/O feature a special backplane is necessary. Do not plug a rear I/O configured board in a non-system slot rear I/O backplane. This will damage the board. **This is of critical importance to the VGA interface; the blue signal of the VGA controller is connected to the CompactPCI connector J2 at pin C13. On the non-rear I/O version this pin is connected to the VI/O pin (default 5V) and on the rear I/O version this pin carries the VGA blue signal. If the rear I/O version is plugged into a non-system slot rear I/O backplane, the VGA controller will be damaged. (The blue signal is directly connected to the 5 V line)**

Serial Interface COM1 and COM2

The COM1 port can be used on either the front I/O or the rear I/O. If rear I/O configuration is enabled the driver for the COM1 port can be disabled via the BIOS setting or the rear I/O configuration register. The COM2 port can be used only on the rear I/O interface.

USB Interface

There are four independent USB interfaces available, two ports are routed to the 4-pin front I/O connector. The other two ports are only available on the rear I/O connector.

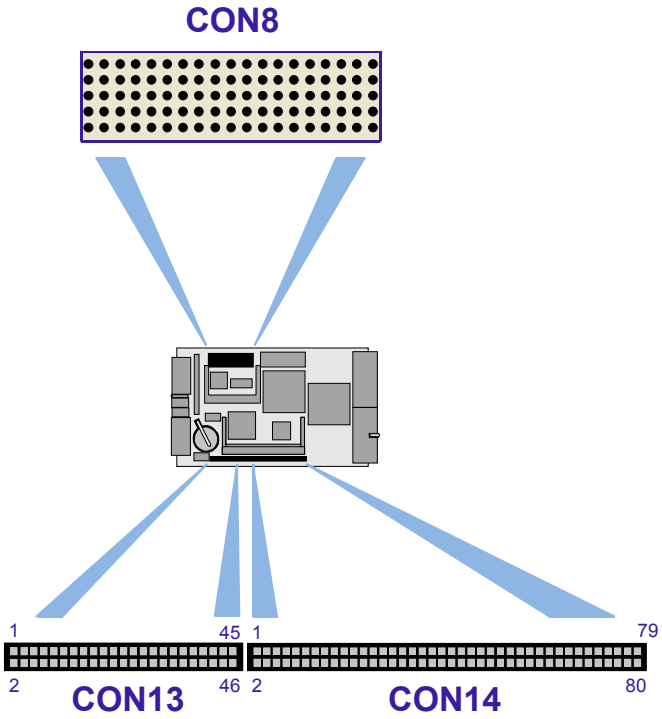
Note ...

All four USB ports may be used at the same time.

2.3.10 Extension Connectors CON8, CON13 and CON14

The I/O extension connectors provide cost-effective, flexible configuration options.

Figure 2-11: Extension Connectors CON8, CON13 and CON14



2.3.10.1 AGP Extension Connector CON8

For a flexible VGA controller configuration an onboard AGP 4x extension connector (CON8) is available. This interface contains all necessary signals for the AGP 4x bus to connect one AGP device. The AGP interface supports all three AGP standards AGP 1x, AGP 2x and AGP 4x. The default configuration is AGP 4x with 1.5V signaling voltage.

Table 2-17: AGP Data Transfer Rate

Bus Type	Clock Frequency	Effective Clock Frequency	Signaling voltage	Data Transfer rate
PCI 1 x 33 MHz	33 MHz	33 MHz	3.3 V	133 MB/sec
AGP1 x 66 MHz	66 MHz	66 MHz	3.3 V	266 MB/sec
AGP 2 x 66 MHz	66 MHz	133 MHz (*2)	3.3 V	512 MB/sec
AGP 4 x 66 MHz	66 MHz	266 MHz (*4)	1.5 V	1024 MB/sec

Note ...

If the AGP 4x extension connector is equipped, the onboard CompactFlash socket cannot be used.

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2.3.10.2 I/O Extension Connector CON13

On the Intel® 815 chipset platform, the Super I/O (SIO) component has migrated to the Low Pin Count (LPC) interface. On the 4HP version there is no Super I/O device implemented. To provide a flexible configuration of further low speed PC devices e.g. Super I/O, IPMI or CAN controller, the LPC port is connected to the I/O extension connector. The I/O extension interface contains all the necessary signals to connect up to three LPC devices.

In addition to the LPC interface the digital AC'97 link is connected to the I/O extension connector (CON13). The ICH2 integrated digital link allows several external codecs configurations on 8HP, e.g. audio with an audio codec, a modem with a modem codec, or an integrated audio/modem codec.

2.3.10.3 PCI Extension Connector CON14

For a flexible configuration an onboard PCI extension connector is available. This interface contains all the necessary signals to enable the 32-bit PCI bus to connect three PCI master devices. To support the three PCI master devices there are three sets of the following signals available: CLOCK, REQ and GNT.

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Chapter 3

Installation

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3. Installation

3.1 Board Installation

Caution!

If your board type is not specifically qualified as hot swap capable, please switch off the CompactPCI system before installing the board in a free CompactPCI slot. Failure to do so could endanger your life/health and may damage your board or system.

Note ...

Certain CompactPCI boards require bus master and/or rear I/O capability. If you are in doubt whether such features are required for the board you intend to install, please check your specific board and/or system documentation to make sure that your system is provided with an appropriate free slot in which to insert the board.

ESD Equipment!

Your CompactPCI board contains electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:

Discharge your clothing before touching the assembly. Tools must be discharged before use.

Do not touch components, connector-pins or traces.

If working at an anti-static workbench with professional discharging equipment, please do not omit to use it.

Chapters 2 and 5 of this manual describe the hardware and software setup of the CP303 controller board, its CPU and the following related devices:

- serial port
- floppy disk interface
- EIDE device interface
- VGA
- USB
- Fast Ethernet

3.1.1 Placement of the CP303

The Kontron CompactPCI system configuration is characterized by the fact that its system slot (slot “1”) is on the right end of the backplane, thus allowing for physical CPU growth (heat-sink, cooling fan etc.) associated with higher performance processors.

Note ...

After having inserted your controller board, please make sure it has been fitted into the system slot.

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3.1.2 EIDE Interface

The CP303 board is provided with one EIDE interface.

The EIDE interface allows installation of up to two devices (one master-slave pair). If installed, the devices are automatically recognized by the BIOS at system “power on”.

3.1.2.1 Hard Disk Installation

To install a hard disk, it is necessary to perform the following operations in the given order:

1. Install the hardware;
2. Initialize the software necessary to run the chosen operating system.

Warning!

The incorrect connection of power or data cables may damage your hard disk unit and/or CP303 board.

Note ...

ATA-66 and ATA-100 are faster timings and require a specialized cable which has additional grounding wires to reduce reflections, noise, and inductive coupling. This cable will also support all legacy IDE drives.

The blue end of the ATA-100 cable must connect to the motherboard the gray connector to the UltraDMA/100 slave device and the black connector to the UltraDMA/100 master device.

Some symptoms of incorrectly installed HDDs are:

- Hard disk drives are not auto-detected: may be a Master / Slave problem or a bad IDE cable. Contact your vendor.
- Hard Disk Drive Fail message at bootup: may be a bad cable or lack of power going to the drive.
- No video on bootup: usually means the cable is on backwards.
- Hard drive lights are constantly on: usually means bad IDE cable or defective drives / motherboard. Try another HDD.
- Hard drives do not power up: check power cables and cabling. May also be a bad power supply or IDE drive.

3.1.3 CompactFlash Interface

The CompactFlash socket supports all available CompactFlash ATA cards type I and type II with 3.3V.

Warning!

The CP303 does not support removal and reinsertion of the CompactFlash storage card while the host computer’s power is on. Connecting the CompactFlash cards while the power is on, which is known as ”hot plugging”, may damage your system.

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3.1.4 USB Connectors

The CP303 supports all USB plug and play computer peripherals (e.g. keyboard, mouse, printer etc.).

Note ...

All USB devices can be attached or detached while the host or other peripherals are powered up.

3.1.5 Rear I/O Installation

Warning!

To support the rear I/O feature a special backplane is necessary. Do not plug a rear I/O configured board in a non-system slot rear I/O backplane. This will damage the board. **This is of critical importance to the VGA interface; the blue signal of the VGA controller is connected to the CompactPCI connector J2 at pin C13. On the non-rear I/O version this pin is connected to the VI/O pin (default 5V) and on the rear I/O version this pin carries the VGA blue signal. If the rear I/O version is plugged into a non-system slot rear I/O backplane, the VGA controller will be damaged. (The blue signal is directly connected to the 5 V line)**

3.1.6 LVDS Connectors

The CP303 supports LVDS via the LVDS A and LVDS B connectors on the front panel. The LVDS flat panel display must be connected to the CP303 prior to applying power to the board.

Warning!

Do not disconnect or connect the LVDS panel with system power applied.

Connecting or disconnecting of the LVDS panel with power applied to the system will result in damage to the CP303 board.

3.2 Software Installation

The installation of the Ethernet and all other onboard peripheral drivers is described in detail in the relevant Driver Kit files.

Installation of an operating system is a function of the OS software and is not addressed in this manual. Refer to appropriate OS software documentation for installation.

Note ...

Users working with pre-configured operating system installation images for Plug and Play compliant operating systems, for example Windows® 95/98/ME, Windows® 2000, Windows® XP, Windows® XP Embedded, must take into consideration that the stepping and revision ID of the chipset and/or other onboard PCI devices may change. Thus, a re-configuration of the operating system installation image deployed for a previous chipset stepping or revision ID is in most cases required. The corresponding operating system will detect new devices according to the Plug and Play configuration rules.

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Chapter 4

Configuration

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4. Configuration

4.1 Jumper Description

4.1.1 Dual BIOS Configuration

Dual BIOS means that there are two chips for the BIOS on the CP303 board (BIOS Flash and the User Flash). One chip is intended to provide a backup in the event that the other gets corrupted. These chips are soldered to the board.

If the primary BIOS is corrupted due to physical damage or a faulty flash upgrade, the solder jumper J2 should be set and the system switched over to the secondary chip and booted with default settings.

Table 4-1: Dual BIOS Configuration

J2	Description
Open	*Normal boot from the onboard BIOS*
Closed	Boot from the second BIOS chip

The default setting is indicated by italics

Note ...

The Dual BIOS feature cannot be used if the second Flash chip is used for VxWorks

4.1.2 Clearing BIOS CMOS Setup

If the system does not boot (due to, for example, the wrong BIOS configuration, or wrong password setting) the CMOS setting may be cleared using Jumper J4.

Procedure for clearing CMOS setting:

The system is booted with the jumper in the new, closed position, then powered down again. The jumper is reset back to the normal position, then the system is rebooted again

Table 4-2: Clearing BIOS CMOS Setup

J4	Description
Open	*Normal boot using the CMOS settings*
Closed	Clear the CMOS settings and use the default values

The default setting is indicated by italics

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4.1.3 Shorting Chassis GND (Shield) to Logic GND

The front panel and front panel connectors are isolated to the logic ground.

To enable the connection between the chassis GND and logic GND the capacitors must be exchanged with zero ohm resistors.

Table 4-3: Shorting Chassis GND (Shield) to Logic GND

CAPACITOR	SETTING	DESCRIPTION
C77, C179, C287	*Closed 470pF 2KV capacitors*	*Connectors are isolated to logic GND with three 470pF 2KV capacitors*
	Closed zero ohm resistors	Connectors are connected to logic GND and chassis GND

The default setting is indicated by italics.

4.1.4 PCI VI/O setting

The CP303 provides for either a 5V or 3.3V PCI signaling environment.

The BVI/O jumpers are used to power the buffers for the onboard chips and the PCI extension. The BVI/O does not provide power to the CompactPCI interface. The CompactPCI VI/O must be configured via the backplane.

Table 4-4: PCI VI/O Setting

R72	R76	DESCRIPTION
Open	*Closed*	*Board is configured for 5V VI/O*
Closed	Open	Board is configured for 3.3V VI/O

The default setting is indicated by italics.

4.1.5 Reserved Jumpers

The following jumpers are reserved for future configurations:

J3 and J5

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4.2 Interrupts

The CP303 board uses the standard AT IRQ routing (8259 controller).

This interrupt routing is the default, but can be modified via the BIOS.

Table 4-5: Interrupt Setting

IRQ	Priority	Standard Function
IRQ0	1	System Timer
IRQ1	2	Keyboard Controller
IRQ2	--	Input of the second IRQ controller (IRQ8-IRQ15)
IRQ3	11	Free reserved for COM2
IRQ4	12	Free reserved for COM1
IRQ5	13	Watchdog
IRQ6	14	Floppy Disk Controller
IRQ7	15	Free reserved for COM3 or COM4
IRQ8	3	System Real Time Clock
IRQ9	4	PCI or ACPI
IRQ10	5	PCI
IRQ11	6	PCI
IRQ12	7	PCI or PS/2 mouse
IRQ13	8	Coprocessor error
IRQ14	9	Primary hard disk
IRQ15	10	Secondary hard disk
NMI		Watchdog

Warning!

IRQ5 should normally have only **one** source enabled, otherwise improper system operation may result.

If more than one source is required to be enabled, contact Kontron's Technical Support before implementing the IRQs.

For events that are not time critical, such as ENUM, DERATE, etc., polling should be considered instead of using an IRQ.

Note ...

Selecting USB keyboard support in the BIOS will initiate an emulation of a PS/2 keyboard. This emulation uses a cyclic SMI interrupt whereby the latency of the interrupt handler may by up to 250 µsec. The BIOS and the CPU speed are the primary influences concerning the increased latency. The latency is not consistent with regards to occurrence or duration.

Since the SMI is the highest IRQ, other IRQ routines may experience erratic latency. Should this interfere with the application requirements, turn off this option in the BIOS or disable the SMIs in the start-up boot code.

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4.3 Onboard PCI Interrupt Routing

The ICH2 provides up to 8 PCI interrupt inputs. The table below describes the connection of these IRQ signals:

For more information please see the INTEL ICH2 data sheet.

Table 4-6: PCI Interrupt Routing

ICH2 IRQ Input	PCI Device	Function Internal ICH2
PIRQA	PCI to PCI Bridge IRQA	Free
PIRQB	PCI to PCI Bridge IRQB	AC97 + MODEM + SMBUS
PIRQC	PCI to PCI Bridge IRQC	Free
PIRQD	PCI to PCI Bridge IRQD	USB 1 controller
PIRQE	Free	ICH 2 LAN controller IRQA
PIRQF	Free	Free
PIRQG	External 82559 IRQA	Free
PIRQH	Free	USB 2 controller

4.4 Memory Map

The CP303 board uses the standard AT ISA memory map.

4.4.1 Memory Map for the 1st Megabyte

The following table sets out the memory map for the first megabyte:

Table 4-7: Memory Map for the 1st Megabyte

Memory Range	Size	Function
0xE0000 – 0xFFFFF	128 k	BIOS implemented in FWH Reset vector 0xFFFF0
0xD0000 – 0xDFFFF	64 k	Free
0xCC000 – 0xCFFFF	16 k	Free
0xC0000 – 0xCBFFF	48 k	BIOS of the VGA card.
0xA0000 – 0xBFFFF	128 k	Normally used as video RAM as follows: CGA video : 0xB8000-0xBFFFF Monochrome video : 0xB0000-0xB7FFF EGA/VGA video : 0xA0000-0xAFFFF
0x000000 – 0x9FFFF	640 k	DOS reserved memory space

Note ...

The 512 kB FLASH extension is mapped in the extended memory area e.g. 0xFFF00000–0xFFF7FFFF. The Flash address range can be configured by the ICH2 chip.

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4.4.2 I/O Address Map

The following table sets out the memory map for the I/O memory:

Table 4-8: I/O Address Map

Address	Device
000,00F	DMA controller #1
020,021	Interrupt controller #1
022,02F	Reserved
040,043	Timer
060,063	Keyboard interface
070,071	RTC port
080,08F	DMA page register
0A0,0A	Interrupt controller #2
0C0,0DF	DMA controller #2
0E0,0EF	Reserved
0F0,0FF	Math coprocessor
170,17F	Hard disk secondary
1F0,1FF	Hard disk primary
278,27F	Parallel port LPT2
280	Watchdog trigger
282	Watchdog timer
284	Watchdog, CPCI IRQ routing
286	I/O status
287	I/O configuration
288	Board version
289	Hardware index
28B	Logic index
28D	LED control
2E8,2EF	Serial port COM4
2F8,2FF	Serial port COM2
378,37F	Parallel printer port LPT1
3BC,3BF	Parallel printer port LPT3
3E8,3EF	Serial port COM3
3F0,3F7	Floppy Disk + Super-I/O #1 Com.
3F8,3FF	Serial port COM1

Note ...

The yellow (shaded on a printout) table cells indicate CP303-specific registers.

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4.5 Special Registers Description

The following registers are special registers which the CP303 uses to watch the onboard hardware special features and the CompactPCI control signals.

Normally, only the system BIOS uses these registers, but they are documented here for application use as required.

Note ...

Take care when modifying the contents of these registers as the system BIOS may be relying on the state of the bits under its control.

4.5.1 Watchdog

The CP303 has one watchdog timer. This timer is provided with a programmable timeout ranging from 125 msec to 256 sec. Failure to strobe the watchdog timer within a set time period results in a system reset, NMI or an interrupt. This can be configured via the register 0x284.

To enable the watchdog bit ”4” of the register 0x282 must be set. If the watchdog is enabled via bit ”4” this bit cannot later be cleared.

With a write access to the register 0x280 the watchdog is retriggered. Once the watchdog is enabled, it must be continuously strobed within the terminal count period to avoid resetting the system hardware.

The watchdog can be configured in several modes, one of which is the dual stage configuration. If the NMI and the reset configuration bit are set (0x284 = 0x84) the watchdog has two stages. The first stage timeout generates an NMI interrupt. If the NMI handler does not reconfigure the watchdog, the watchdog switches to the second stage and generates a master reset after the configured timeout elapses.

4.5.2 Watchdog Trigger

A write access triggers the watchdog.

The I/O location for the watchdog trigger is 0x280.

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4.5.3 Watchdog Timer

Table 4-9: Watchdog Timer

REGISTER NAME		WATCHDOG TIMER						ACCESS	
ADDRESS		0x282						R	W
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		Res.	Res.	Res.	WDEN	WDT3	WDT2	WDT1	WDT0
DEFAULT		0	0	0	0	0	0	0	0

BIT	NAME	VAL	DESCRIPTION
0 1 2 3	WDT[3:0]		Timeout Period: Bits: 3 2 1 0 Setting: 0 0 0 0 = 0 = 000.125 sec 0 0 0 1 = 1 = 000.250 sec 0 0 1 0 = 2 = 000.500 sec 0 0 1 1 = 3 = 001 sec 0 1 0 0 = 4 = 002 sec 0 1 0 1 = 5 = 004 sec 0 1 1 0 = 6 = 008 sec 0 1 1 1 = 7 = 016 sec 1 0 0 0 = 8 = 032 sec 1 0 0 1 = 9 = 064 sec 1 0 1 0 = 10 = 128 sec 1 0 1 1 = 11 = 256 sec 1 1 0 0 = 12 = res. 1 1 0 1 = 13 = res. 1 1 1 0 = 14 = res. 1 1 1 1 = 15 = res.
4	WDEN	0	Watchdog timer disabled
		1	Watchdog timer enabled ***Note ...*** Once the watchdog timer is enabled it cannot be disabled except by resetting the system.
5		0	Reserved
6		0	Reserved
7		0	Reserved

4.5.4 Watchdog, CompactPCI Interrupt Configuration Register

The interrupt configuration register holds a series of bits defining the interrupt routing for the watchdog, the power control derate signal and the CompactPCI enumeration signal. If the watchdog timer fails, it can generate three independent hardware events: reset, NMI and IRQ5 interrupt.

The enumeration signal is generated by a hot swap compatible board after insertion and prior to removal. The system uses this interrupt signal to force software to configure the new board. The derate signal indicates that the power supply is beginning to derate its power output.

Note...

To enable the dual stage watchdog the NMI and the reset bit must be set. At the first stage the watchdog generates an NMI and at the second stage the system will be reset.

Table 4-10: Watchdog, CompactPCI Interrupt Configuration Register

REGISTER NAME		Interrupt Configuration Register						ACCESS	
ADDRESS		0x284						R	W
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		WNMI	CFNMI	CFIRQ	CEIRQ	CDIRQ	WRST	WIRQ	Res.
DEFAULT		0	0	0	0	0	0	0	0
BIT	NAME	VAL	DESCRIPTION						
0		0	Reserved						
1	WIRQ	0	Disable Watchdog IRQ5 routing						
		1	Enable Watchdog IRQ5 routing						
2	WRST	0	Disable Watchdog hardware reset						
		1	Enable Watchdog hardware reset						
3	CDIRQ	0	Disable CPCI derate signal to IRQ5 routing						
		1	Enable CPCI derate signal to IRQ5 routing						
4	CEIRQ	0	Disable CPCI enum signal to IRQ5 routing						
		1	Enable CPCI enum signal to IRQ5 routing						
5	CFIRQ	0	Disable CPCI fail signal to IRQ5 routing						
		1	Enable CPCI fail signal to IRQ5 routing						
6	CFNMI	0	Disable CPCI fail signal to NMI routing						
		1	Enable CPCI fail signal to NMI routing						
7	WNMI	0	Disable Watchdog NMI routing						
		1	Enable Watchdog NMI routing						

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4.5.5 I/O Status

This register describes the local and CompactPCI control signals. The watchdog status bit indicates the status of the watchdog timer. If the timer is not retriggered within the previously set time period, the bit is set to ”0” and the watchdog LED lights. The fail signal is an output of the power supply and indicates a power supply failure. For the description of the derate and enumeration signals please see the interrupt routing register.

Table 4-11: I/O Status Register

REGISTER NAME		I/O Status Register						ACCESS	
ADDRESS		0x286						R	
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		WST	Res.	Res.	Res.	CSLOT	CENUM	CFAIL	CDER
DEFAULT		1	0	0	0	0	0	0	0
BIT	NAME	VAL	DESCRIPTION						
0	CDER	0	Indicates power derating (CPCI DEG signal)						
		1	Power normal						
1	CFAIL	0	Indicates a power supply failure (CPCI FAIL signal)						
		1	Power normal						
2	CENUM	0	Indicates the insertion or removal of a hot swap system board (CPCI ENUM)						
		1	No hot swap event						
3	CSLOT	0	Indicates that the board is installed in a system slot						
		1	Indicates that the board is installed in a peripheral slot						
4		0	Reserved						
5		0	Reserved						
6		0	Reserved						
7	WST	0	Indicates that a Watchdog timeout has occurred						
		1	Indicates that no Watchdog timeout has occurred						

4.5.6 I/O Configuration Register

The I/O configuration register holds a series of bits defining the onboard configuration for the two COM ports and the general purpose LEDs.

Table 4-12: I/O Configuration Register

REGISTER NAME		I/O Configuration Register						ACCESS	
ADDRESS		0x287						R	W
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		Res.	DBIOS	ELED2	ELED1	ESIOR	ESIOE	ECOM2	ECOM1
DEFAULT		0	0	0	0	0	0	0	0
BIT	NAME	VAL	DESCRIPTION						
0	ECOM1	0	Disable COM1 interface on 4 HP version						
		1	Enable COM1 interface on 4 HP version						
1	ECOM2	0	Disable COM2 interface on 4 HP version						
		1	Enable COM2 interface on 4 HP version						
2	ESIOE	0	Enable Super I/O on extension module						
		1	Disable Super I/O on extension module						
3	ESIOR	0	Disable keyboard controller emulation						
		1	Enable keyboard controller emulation						
4	ELED1	0	Enable LED1 for watchdog						
		1	Enable LED1 for GP						
5	ELED2	0	Enable LED2 for over temperature						
		1	Enable LED2 for GP						
6	DBIOS	0	Default boot from 1st FWH						
		1	Boot from 2nd FWH						
7		0	Reserved						

4.5.7 Board Version

This register describes the hardware and the board version. The content of this register is unique for each Kontron CompactPCI board.

Table 4-13: Board ID Register

REGISTER NAME	Board Version						ACCESS	
ADDRESS	0x288						R	
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	BID7	BID6	BID5	BID4	BID3	BID2	BID1	BID0
DEFAULT	0	1	0	1	0	0	0	0

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4.5.8 Hardware Index

The hardware index will signal to the software when differences in the hardware require different handling by the software. It starts with the value 0 and will be incremented with each change in hardware as development continues.

Table 4-14: Hardware Index Register

REGISTER NAME	Hardware Index						ACCESS	
ADDRESS	0x289						R	
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	HWI7	HWI6	HWI5	HWI4	HWI3	HWI2	HWI1	HWI0
DEFAULT	0	0	0	0	0	0	0	0

4.5.9 Logic Version

The logic version register may be used to identify the logic status of the board by software. It starts with the value 0 and will be incremented with each logic update.

Table 4-15: Logic Version Register

REGISTER NAME	Logic Version						ACCESS	
ADDRESS	0x28B						R	
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	LR7	LR6	LR5	LR4	LR3	LR2	LR1	LR0
DEFAULT	0	0	0	0	0	0	0	0

4.5.10 LED Control

With the LED Control register the LED on the front panel can be switched on and off.

Table 4-16: LED Control Register

REGISTER NAME		LED Control Register						ACCESS	
ADDRESS		0x28D						R	W
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		res.	res.	res.	res.	res.	res.	LED1	LED0
DEFAULT		0	0	0	0	0	0	0	0
BIT	NAME	VAL	DESCRIPTION						
0	LED0	0	LED off						
		1	LED on						
1	LED1	0	LED off						
		1	LED on						
2		0	Reserved						
3		0	Reserved						
4		0	Reserved						
5		0	Reserved						
6		0	Reserved						
7		0	Reserved						

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4.6 Onboard Chipset I/O Configuration

The ICH2 provides several general purpose I/O pins. The table below describes the connection of these I/O pins:

For more information please see the Intel® ICH2 data sheet.

Table 4-17: On-board Chipset I/O Configuration

Number	Type	After Reset	Description
GPIO0	R	Input	Free
GPIO6	R	Input	Cable detection for primary EIDE port
GPIO7	R	Input	Cable detection for secondary EIDE port
GPI8	R	Input	Rear I/O status 1 = rear I/O module plugged in 0 = no rear I/O module plugged in
GPI12	R	Input	SMI input from hardware Monitor LM81
GPI13	R	Input	Extension module selector 1 = no extension module plugged 0 = extension module plugged
GPO18	W	Output blinks	GPIO[18] blinks, by default, immediately after reset. Connected to logic
GPO19	W	Output High	Ethernet 1 interface 1 = front I/O interface 0 = rear I/O interface
GPO20	W	Output High	Ethernet 2 interface 1 = front I/O interface 0 = rear I/O interface
GPO21	W	Output High	COM1 R232 buffer for front I/O connector 1 = disable RS232 buffer 0 = enable RS232 buffer
GPO22	W	Output High	Free
GPO23	W	Output Low	Free
GPIO24	RW	Input High	Solder Jumper for BIOS setting 1 = normal 0 = clear CMOS RAM
GPIO25	RW	Input High	Reserved
GPIO27	RW	Input High	Ethernet 2 Link Status 1 = no link 0 = link
GPIO28	RW	Input High	Ethernet 1 Link Status 1 = no link 0 = link

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Chapter 5

CMOS

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5. CMOS

This chapter describes the Award BIOS Setup program, BIOS, version 6.00PG. The Setup program lets you modify basic system configuration settings.

5.1 Proprietary Notice

5.2 Introduction to Setup

This manual describes the Award BIOS Setup program. The Setup program lets you modify basic system configuration settings. The settings are then stored in a dedicated battery-backed memory, called CMOS RAM, that retains the information when the power is turned off.

A special feature of *Kontron's* CompactPCI boards is that all Setup information is additionally saved in a non-volatile serial EEPROM. This feature provides the user with enhanced data security in comparison with a standard PC board, because setup data will not be lost should the battery fail.

The Award BIOS in your computer is a customized version of an industry-standard BIOS for IBM PC AT–compatible personal computers. It supports the Intel®x86 and compatible processors. The BIOS provides critical low-level support for the system central processing, memory, and I/O subsystems.

The Award BIOS has been customized by adding important, but nonstandard, features such as virus and password protection, power management, and detailed fine-tuning of the chipset controlling the system.

The rest of this manual is intended to guide you through the process of configuring your system using Setup.

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Starting Setup

The Award BIOS is immediately activated when you first turn on the computer. The BIOS reads system configuration information in CMOS RAM and begins the process of checking out the system and configuring it through the Power-on Self Test (POST).

When these preliminaries are finished, the BIOS seeks an operating system on one of the data storage devices (hard drive, floppy drive, etc.). The BIOS launches the operating system and hands control of system operations to it.

During POST, you can start the Setup program in one of two ways:

- By pressing <Del> immediately after switching the system on, or
- By pressing the <Del> key or by simultaneously pressing <CTRL>, <ALT>, and <ESC> keys when the following message appears briefly at the bottom of the screen during POST:

Press DEL to enter SETUP

If the message disappears before you respond and you still wish to enter Setup, restart the system to try again by turning it OFF then ON or pressing the RESET button on the system case. You may also restart by simultaneously pressing <CTRL>, <ALT>, and <Delete> keys. If you do not press the keys at the correct time and the system does not boot, an error message appears and you are again asked to

Press F1 to continue, DEL to enter SETUP

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Setup Keys

Use the keystrokes listed in the left column of the table below to make your selections or exit the current menu. The table below describes the functions of the keystrokes:

The following table describes how to navigate in Setup using the keyboard.

Table 5-1: Keyboard Commands

Key	Description
Up Arrow	Move to previous item
Down Arrow	Move to next item
Left Arrow	Move to the item to the left
Right Arrow	Move to the item to the right
Esc Key	Exit this menu. Main Menu: Quit without saving changes into CMOS RAM
PgUp Key	Increase the numeric value or make changes
PgDn Key	Decrease the numeric value or make changes
+ Key	Increase the numeric value or make changes
- Key	Decrease the numeric value or make changes
F1 Key	Brings up the General Help window that describes the legend keys
F5 Key	Select the Previous Value for the field
F6 Key	Load the Fail-Save Defaults for this page
F7 Key	Load the Optimized Defaults for this page
F10 Key	Save to CMOS and EXIT
Enter	Execute Command or Select sub menu

To display a sub-menu, use the arrow keys to move the cursor to the sub-menu you want. Then press <Enter>.

A pointer (>) indicates those entries which have sub-menus. Within the sub-menus, the variable fields may be changed directly if the desired values are known. Alternatively, a pop-up box may be opened by selecting the item using the arrow keys and then pressing return. The box offers a range of values from which a selection may be made.

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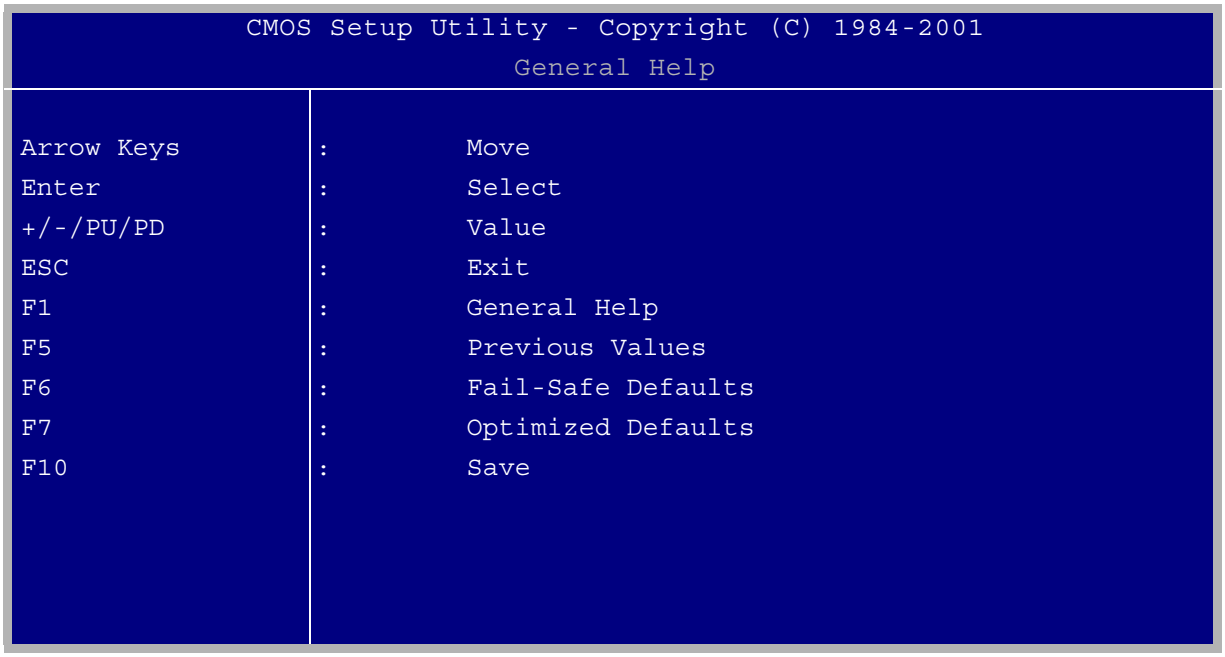
Getting Help

The General Help Window

Press F1 and the General Help window pops up which describes the legend keys and their alternatives. To exit the Help Window press <Esc>.

Figure 5-1: General Help Window — Screen Display



The Field Help Window

The Item Help window on the right side of each menu displays the help text for the currently selected field. It updates as you move the cursor to each field.

In Case of Problems

You can restart by either using the ON/OFF switch, the RESET button or by pressing <CTRL>, <ALT> and <Delete> at the same time. The best advice is change only those settings that you thoroughly understand. In particular, do not change settings in the Chipset screen without good reason. The Chipset defaults have been carefully chosen by Kontron Modular Computers for optimum performance and reliability. Even a seemingly small change to the Chipset setup may result in the system becoming unstable.

Setup Variations

Not all systems have the same Setup. While the basic look and function of the Setup program remains the same for all systems, the appearance of your Setup screens may differ from the screens shown here. Each system design and chipset combination require customized configurations. In addition, the final appearance of the Setup program depends on your system designer. Your system designer may decide that certain items should not be available for user configuration and remove them from the Setup program.

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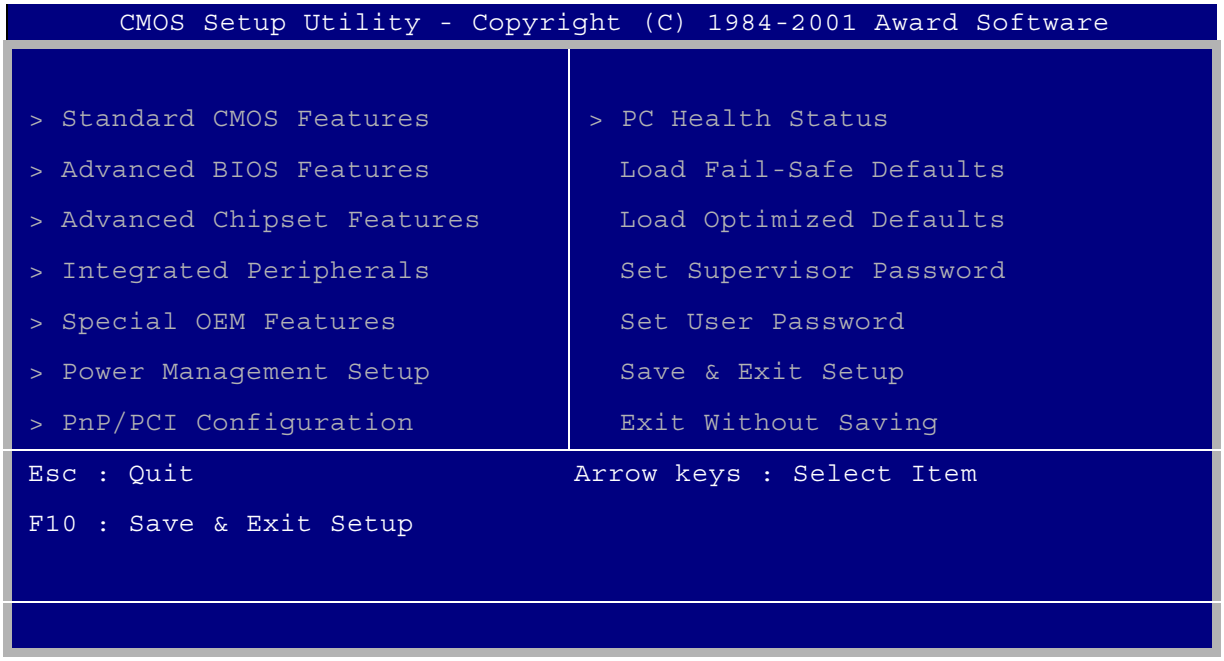
5.3 Main Setup Menu

When you enter the Award BIOS CMOS Setup Utility, a Main Menu, similar to the one shown below, appears on the screen. The Main Menu allows you to select from several Setup functions and two exit choices. Use the arrow keys to select items and press ↵ to accept and enter the sub-menu.

Figure 5-2: CMOS Setup Utility Main Menu — Screen Display



A brief description of each highlighted selection appears at the bottom of the screen.

Following is a brief summary of each Setup category.

Standard CMOS Setup

Options in the original PC AT-compatible BIOS.

Advanced BIOS Features

Award enhanced BIOS options.

Advanced Chipset Features

Options specific to your system chipset.

Integrated Peripherals

I/O subsystems, which are dependant on the integrated peripherals controller in your system.

Special OEM Features

Kontron features specific to Award BIOS.

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Power Management Setup

Advanced Power Management (APM) options.

PnP/PCI Configuration

Plug and Play standard and PCI Local Bus configuration options.

PC Health Status

Information about the temperature and the voltage of the CPU.

Load Fail-Safe Defaults

BIOS defaults are factory settings for the most stable, minimal-performance system operations.

Load Optimized Defaults

Setup defaults are factory settings for optimal-performance system operations.

Set Supervisor/User Password

Change, set, or disable a password. In BIOS versions that allow separate user and supervisor passwords, only the supervisor password permits access to Setup. The user password generally allows only power-on access.

Save & Exit Setup

Save settings in non-volatile CMOS RAM and exit Setup.

Exit Without Save

Abandon all changes and exit Setup.

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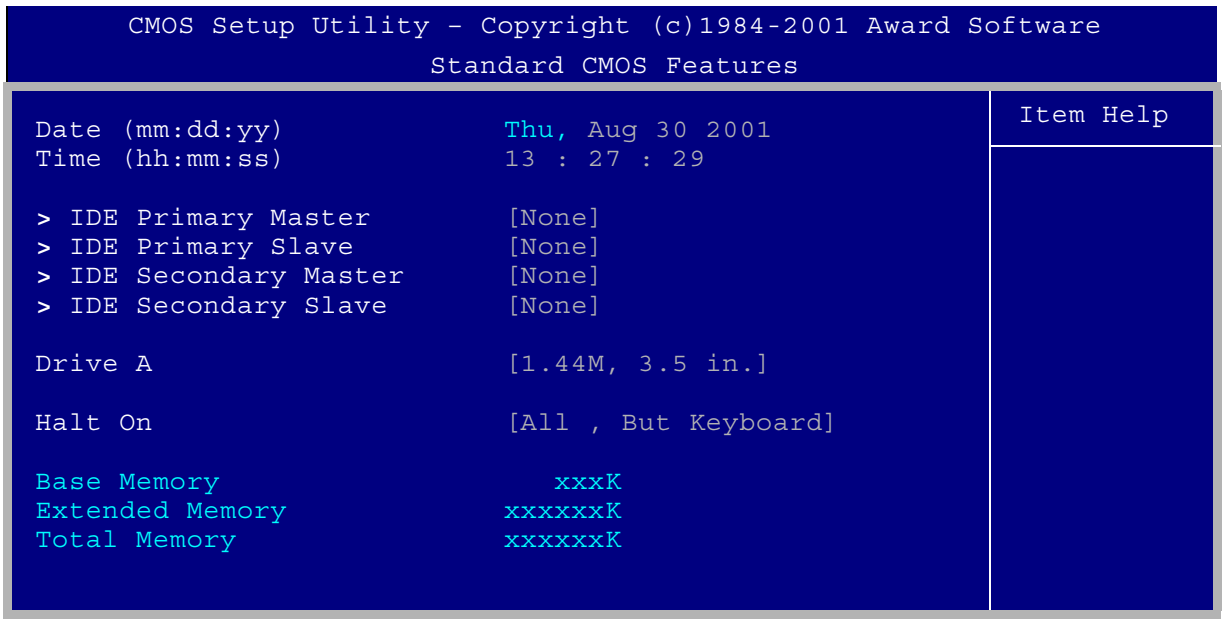
5.4 Standard CMOS Features

In the Standard CMOS menu you may set the system time and date, drive parameters, and select the type of errors that stop the BIOS POST.

Figure 5-3: Standard CMOS Setup Menu — Screen Display



Date

Press the →or ←key to move to the desired field (month, date, year). Press the “PgUp” or “PgDn” key to change the setting, or type the desired value into the field. With these settings you set the system date. The weekday is set from the system.

Time

The time format is based on the 24-hour military-time clock. For example, 1 p.m. is 13:00:00. Press the →or ←key to move to the desired field. Press the PgUp or PgDn key to change the setting, or type the desired value into the field. Using these settings you set the system time.

Hard Disks

The BIOS supports up to four EIDE drives. This section does not show information relating to other EIDE devices, such as a CD-ROM drive, or about other hard drive types, such as SCSI drives.

Note ...

We recommend that you select the AUTO type for all drives.

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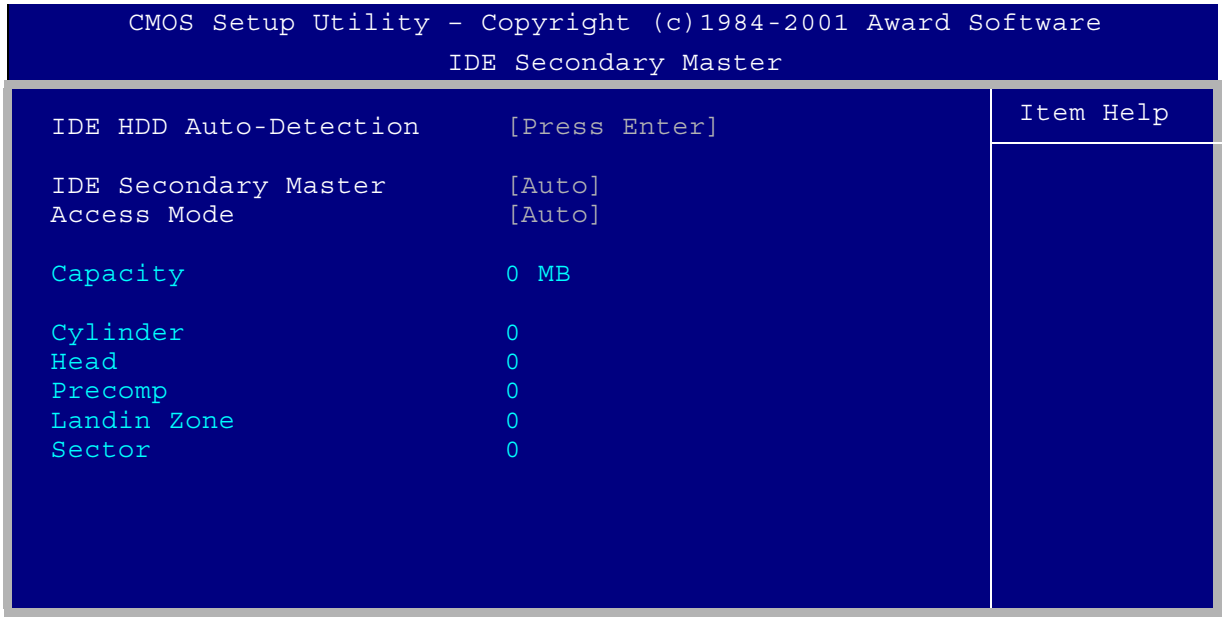
The BIOS has the capability to automatically detect the specifications and optimal operating mode of almost all EIDE hard drives. When AUTO is selected in the hard drive field, the BIOS detects its specifications during POST, every time the system boots.

If you do not want to select drive type AUTO, choose the IDE Drive you will change, press Enter and the Master/Slave menu pops up.

Figure 5-4: IDE Secondary Master — Screen Display



IDE HDD Auto Detection

The BIOS auto-detects the HDDs size, head and other characteristics on this channel.

IDE Primary Slave/Master

Select drive type for hard drive detection.

Access Mode

Select the Access Mode for the hard drive and enter values into each drive parameter field.

The following table provides a brief explanation of drive specifications:

Table 5-2: Description of Drive Specifications

Spec.		Description
Type		The BIOS contains a table of pre-defined drive types. Each defined drive type has a specified number of cylinders, number of heads, write pre-compensation factor, landing zone, and number of sectors. Drives whose specifications do not accommodate any pre-defined type are classified as type USER.
Size		Disk drive capacity (approximate). Note that this size is usually slightly greater than the size of a formatted disk given by a disk-checking program.
Cyls.		Number of cylinders
Head		Number of heads
Precomp.		Write pre-compensation cylinder
Landz		Landing zone
Sector		Number of sectors
Mode	Auto	Auto: The BIOS automatically determines the optimal mode.
	CHS	The maximum number of cylinders, heads, and sectors supported are 65535, 255, and 255 respectively.
	Large	For drives that do not support LBA and have more than 1024 cylinders.
	LBA	During drive accesses, the EIDE controller transforms the data address described by sector, head, and cylinder number into a physical block address, significantly improving data transfer rates. For drives with greater than 1024 cylinders.

Drive A

Selects the correct specifications for the diskette drive installed in the computer.

Table 5-3: Diskette Drives

Drive Type	Description
None	No diskette drive installed
720k, 3.5 in	3-1/2 inch double-sided drive; 720 kilobyte capacity
1.44M, 3.5 in	3-1/2 inch double-sided drive; 1.44 megabyte capacity
2.88M, 3.5 in	3-1/2 inch double-sided drive; 2.88 megabyte capacity

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Halt On

During the power-on self-test (POST), the computer stops if the BIOS detects a hardware error. You can program the BIOS to ignore certain errors during POST and continue the boot-up process. The possible selections are listed in the following table.

Table 5-4: POST Specific Commands

Command	POST Action
No errors	POST does not stop for any errors.
All errors	If the BIOS detects any non-fatal error, POST stops and prompts you to take corrective action.
All, but keyboard	POST does not stop for a keyboard error, but stops for all other errors.
All, but diskette	POST does not stop for diskette drive errors, but stops for all other errors.
All, but disk/Key	POST does not stop for a keyboard or disk error, but stops for all other errors.

5.5 Advanced BIOS Features

This screen contains industry-standard options additional to the core PC AT BIOS. This section describes all fields presented by Award Software in this screen. The example screen below may vary somewhat from the one in your Setup program; your system board designer may omit or modify some fields

Figure 5-5: Advanced BIOS Features - Screen Display

```
CMOS Setup Utility - Copyright (c)1984-2001 Award Software
                    Advanced BIOS Features

Virus Warning               [Disabled]          Item Help
CPU Internal Cache          [Enabled]
External Cache              [Enabled]
CPU L2 Cache ECC Checking   [Enabled]
Processor Number Feature    [Enabled]
Quick Power On Self Test    [Enabled]
First Boot Device           [Floppy]
Second Boot Device          [HDD-0]
Third Boot Device           [LS120]
Boot Other Device           [Enabled]
Boot Up Floppy Seek         [Enabled]
IDE HDD Block Mode          [Enabled]
Security Option             [Setup]
Award Preboot Agent         [Disabled]
Agent Port Address          [3F8h]
Agent after boot            [Disabled]
Agent Baud Rate             [19200]
Report No FDD For WIN 95    [No]
Small Logo(EPA) Show        [Disabled]
```

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Virus Warning

Virus Warning is a primary IDE hard disk boot sector protection. When this function is enabled it prevents the writing of data to the Master Boot Record.

CPU Internal Cache / External Cache

Cache memory is additional memory that is much faster than conventional DRAM (system memory). CPUs from 486-type on up contain internal cache memory, and most, but not all, modern PCs have additional (external) cache memory. When the CPU requests data, the system transfers the requested data from the main DRAM into cache memory, for even faster access by the CPU.

The External Cache field may not appear if your system does not have external cache memory.

CPU L2 Cache ECC Checking

When you select *Enabled*, memory checking is enabled when the external cache contains ECC SRAMs.

Processor Number Feature

Selecting disable means that it is not possible to read the Serial Number of the processor.

Quick Power-on Self Test

Select Enabled to reduce the amount of time required to run the power-on self-test (POST). A quick POST skips certain steps. We recommend that you normally disable quick POST. Better to find a problem during POST than lose data during your work.

First - Second - Third Boot Device / Boot Other Device

The options First, Second and Third Boot Device and Boot Other Device gives you the possibility to create your own Boot Sequence.

This BIOS includes a feature for booting from LAN using the BOOTP / DHCP protocol.

Lan-Boot is based on Etherboot-5.04, a LAN-Boot implementation, which is covered by the GNU public licence. It has been adopted for use with *Kontron* CompactPCI Hardware. As required by the GNU public licence, the complete source code and further information are available via the internet (www.sourceforge.net).

Using this option requires an understanding of the BOOTP and/or DHCP mechanisms and knowledge in configuring a BOOTP or DHCP server. These topics are not described within this manual.

Boot Up Floppy Seek

When Enabled, the BIOS tests (seeks) floppy drives to determine whether they have 40 or 80 tracks. Only 360-KB floppy drives have 40 tracks; drives with 720 KB, 1.2 MB, and 1.44 MB capacity all have 80 tracks. Because very few modern PCs have 40-track floppy drives, we recommend that you set this field to Disabled to save time.

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IDE HDD Block Mode

Select Enabled only if your hard drives support block mode.

Security Option

If you have set a password, select whether the password is required every time the system boots, or only when you enter Setup.

Award Preboot Agent

The Award Preboot Agent is a BIOS extension which redirects console input/output to a serial port with the following capabilities:-

- Supports Windows Hyper Terminal VT100
- Supports direct RS-232C serial (null modem) connection
- Receives keystrokes from the Hyper Terminal
- Enables video snooping at OS load for full run-time video output to HyperTerminal
- Recognizes a subset of VT100/320 escape sequences and control codes
- Supports DOS diagnostic and flash utilities

To be able to use the Award Preboot Agent, the Windows Hyper Terminal (VT100) is required.

Table 5-5: Keyboard Shortcuts for Award Preboot Agent Commands

Keyboard Shortcut	Operation
CTRL + P or F5 key	Previous values
CTRL + F or F6 key	Fail save defaults
CTRL + O or F7 key	Optimized defaults
CTRL + M	Return
CTRL + J	UP
CTRL + K	DOWN
CTRL + G or F1 key	General Help / Award Flash
TAB	Enter setup
ESC + C	Restart

Agent Port Address

Select the UART address to be used by Agent software.

The recommended address is 3F8h (equivalent to COM1) or 2F8h (equivalent to COM2 under DOS).

If no connection is established, check that you have already configured the UART in the INTEGRATED PERIPHERALS setup page. If your system is equipped with rear I/O please ensure also that the front or rear configuration in SPECIAL OEM FEATURES SETUP is correct and that the appropriate port is connected.

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Agent after Boot

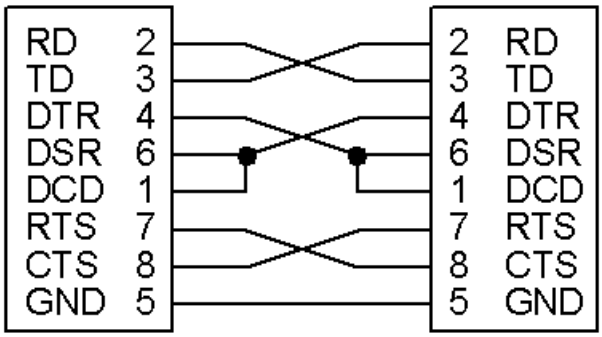
In the "standard" Agent product, Agent software continues to function after the operating system loads. However, some non-DOS operating systems are not compatible with the Agent BIOS extension, so the Agent software should be disabled when the OS loads. Selecting Disabled turns off the Agent software just as the BIOS transfers control to the operating system. Default is Disabled.

Award Baud Rate

Selects the speed at which the UART is to operate. Default is 19,200.

Null-Modem Cable Pinout

Figure 5-6: Null-Modem Cable Connection



A null-modem cable is a serial cable designed to connect two PCs. Each end has a 9-pin, female RS-232C connector. If you are creating your own 9-pin cable, connect the two ends through the cable as shown here.

Further Information

For further information please refer to the manual for the Award Preboot Agent™ 2.0

Report No FDD for WIN 95

Select *Yes* to release IRQ6 when the system contains no floppy drive, for compatibility with Windows 95 logo certification. In the **Integrated Peripherals** screen, select *Disabled* for the **Onboard FDC Controller** field.

Small Logo (EPA) Show

Disable this item and the EPA symbol is not shown on the screen during booting.

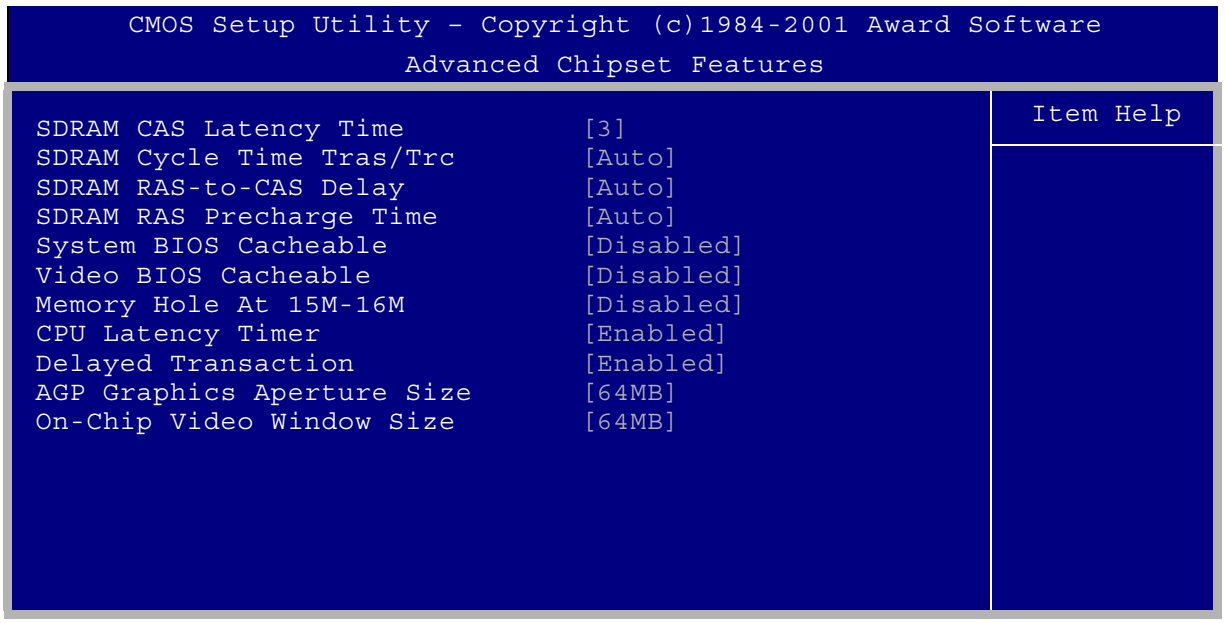
5.6 Advanced Chipset Features

This section describes features of the ICH2 PCI set and describes all the fields presented on this screen display. Please note that your system board designer may omit or modify some of the fields described in the following.

Advanced Options

The parameters in this screen are for system designers, service personnel, and technically competent users only. Do not reset these values unless you understand the consequences of your changes.

Figure 5-7: Chipset Features Setup - Screen Display



SDRAM CAS Latency Time

When synchronous DRAM is installed, you can control the number of CLKs between the SDRAMs sample of a read command and the time when the controller samples read data from the SDRAMs. Do not reset this field from the default value specified by the system designer.

SDRAM Cycle Time Trans/Trc

In this Item you can select the Cycle Time which a memory line is open (Trans), also you can select the Bank Cycle Time (Trc).

SDRAM RAS To CAS Delay

Select the RAS to CAS delay time. See Refresh Cycle Time for information about the Auto Configuration of this value.

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SDRAM RAS Precharge Time

The precharge time is the number of cycles it takes for the RAS to accumulate its charge before DRAM refresh. If insufficient time is allowed, refresh may be incomplete and the DRAM may fail to retain data.

System BIOS Cacheable

Selecting *Enabled* allows caching of the system BIOS ROM at 0xF0000 to 0xFFFFF, resulting in better system performance. However, if any program writes to this memory area, a memory access error may result.

Video BIOS Cacheable

Selecting *Enabled* allows caching of the video BIOS ROM at 0xC0000 to 0xC7FFF, resulting in better video performance. However, if any program writes to this memory area, a memory access error may result.

Memory Hole at 15M-16M

You can reserve this area of system memory for ISA adaptor ROM. When this area is reserved, it cannot be cached. The user information for peripherals that need to use this area of system memory usually discusses their memory requirements.

CPU Latency Timer

CPU Latency Timer Disabled: deferrable processor cycle will be deferred immediately after receiving another ADS#

CPU Latency Timer Enabled = deferrable processor cycle will only be deferred after it has been held in a “Snoop Stall” for 31 clocks and another ADS# has arrived (default).

Delayed Transaction

The chipset has an embedded 32-bit posted write buffer to support delay transactions cycles. Select *Enabled* to support compliance with PCI specification version 2.1.

AGP Graphics Aperture Size

Select the size of the Accelerated Graphics Port (AGP) aperture. The aperture is a portion of the PCI memory address range dedicated for graphics memory address space. Host cycles that hit the aperture range are forwarded to the AGP without any translation.

See http://www.agpforum.org for AGP information.

On-Chip Video Window Size

Programs On-Chip VGA memory cache window in the configured size (Default 64 MB).

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5.7 Integrated Peripherals

Note ...

This section describes all the fields presented by Award Software in this screen display. Please note that your system board designer may omit or modify some fields.

Figure 5-8: Integrated Peripherals — Screen Display

```
        CMOS Setup Utility - Copyright (c)1984-2001 Award Software
                          Integrated Peripherals

                                                                  Item Help
   On-Chip Primary   PCI IDE    [Enabled]
   On-Chip Secondary PCI IDE    [Enabled]
   IDE Primary Master PIO       [Auto]
   IDE Primary Slave  PIO       [Auto]
   IDE Secondary Master PIO     [Auto]
   IDE Secondary Slave  PIO     [Auto]
   IDE Primary Master UDMA      [Auto]
   IDE Primary Slave  UDMA      [Auto]
   IDE Secondary Master UDMA    [Auto]
   IDE Secondary Slave  UDMA    [Auto]
   USB Controller               [Enabled]
   USB Keyboard Support         [Enabled]
   Init Display First           [PCI Slot]
   Watchdog Timer               [Disabled]
X  WDT Active for Booting       Disabled
X  WDT Active Time              256 sec
   CPCI-Enum Signal             [Disabled]
   CPCI-Derate Signal           [Disabled]
   CPCI-Fail Signal             [Disabled]
   AC97 Audio                   [Auto]
   4HP Onboard Serial Port 1    [Disabled]
   4HP Onboard Serial Port 2    [Disabled]
X  8HP Serial Port 1            [Disabled]
X  8HP Serial Port 1            IRQ4
X  8HP Serial Port 2            [Disabled]
X  8HP Serial Port 2            IRQ3
   POWER ON Function            [BUTTON ONLY]
   Onboard FDC Controller       [Enabled]
   Onboard Parallel Port        [Disabled
X  Parallel Port Mode           [PRINTER]
X  ECP Mode Use DMA             3
```

On-Chip PCI IDE (Primary/Secondary)

The Intel® 815 chipset contains a PCI EIDE interface with support for two EIDE channels. Select *Enabled* to activate the primary and/or secondary EIDE interface. Select *Disabled* to deactivate this interface if you instal a primary and/or secondary add-in EIDE interface.

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IDE PIO Modes (Primary/Secondary Master/Slave)

The four EIDE PIO (Programmed Input/Output) fields let you set a PIO mode (0-4) for each of up to four EIDE devices that the internal PCI EIDE interface supports. Modes 0 through 4 provide successively increased performance. In *Auto* mode, the system automatically determines the best mode for each device.

IDE Primary/Secondary Master/Slave UDMA

UDMA (Ultra DMA) is a DMA data transfer protocol that utilizes ATA commands and the ATA bus to allow DMA commands to transfer data at a maximum burst rate of 33 MB/s. When you select *Auto* in the four EIDE UDMA fields (for each of up to four EIDE devices that the internal PCI EIDE interface supports), the system automatically determines the optimal data transfer rate for each EIDE device.

USB Controller

Select Enabled to activate the USB controller. The system needs and takes the IRQ 11.

USB Keyboard Support

Select Enabled if your system contains a Universal Serial Bus (USB) controller and you have a USB keyboard.

Init Display First

Initialize the PCI slot video display before initializing any other display device on the system. Thus, the PCI Slot display becomes the primary display. You also can select the AGP.

Watchdog Timer

When enabled, the Watchdog Timer may be used to select the watchdog routing to NMI, NMI + Reset, IRQ5 or Reset.

WDT Active for Booting

Select *Enable* if the watchdog timer requires to be started before the operating system is booted from the BIOS.

WDT Active Time

Select the time after which the action selected occurs, if the watchdog timer is not retriggered.

CPCI-Enum Signal

The enumeration signal is generated by a hot swap compatible board after insertion and prior to removal. The system uses this interrupt signal to force software to configure the new board.

If this signal is to used inside an application, it may be routed to the IRQ5 interrupt here.

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CPCI-Derate signal

The derate signal indicates that the power supply is beginning to derate its power output.

If this signal is to used inside an application, it may be routed to the IRQ5 interrupt here.

CPCI-Fail Signal

Fail signal from the power supply. If this signal is to used inside an application, it may be routed to the IRQ5 interrupt here.

AC97 Audio

Select Auto if you want use the onboard AC97 Audio-Controller.

4HP Onboard Serial Port 1/2

Here you may disable or enable the two serial ports on the CP303 Motherboard. Note that the connector for serial port 2 is only available on rear IO. The connector for serial port 1 is available on the front panel on the version without the VGA connector, otherwise this port is only available on rear IO.

If you require serial ports with front panel connectors, this facility is available via the optional CP303-IDE1 Super I/O extension board.

8 HP Serial Port 1/2

These are only available where Super I/O exists (via CP303-IDE1 module).

Selects a logical COM port address and the corresponding interrupts for the two serial ports.

POWER ON Function

Choose how to start the system. Button Only (Standard) or Any Key. The function Any Key is only possible under a PS/2 Keyboard.

Onboard FDC Controller

Select *Enabled* if your system has a floppy disk controller (FDC) installed on the system board and you wish to use it. If you install an add-on FDC or the system has no floppy drive, select *Disabled* in this field.

Onboard Parallel Port

Select a logical LPT port address and corresponding interrupt for the physical parallel port.

Parallel Port Mode

Select an operating mode for the onboard parallel port. Select *Normal* unless you are certain that both your hardware and software support one of the other available modes.

ECP Mode Use DMA

Select a DMA channel for the parallel port for use during ECP mode.

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5.8 Special OEM Features

Note ...

This section describes all the fields presented by Award Software in this screen display. Your system board designer may omit or modify some fields.

Figure 5-9: Special OEM Features — Screen Display

```
       CMOS Setup Utility - Copyright (c)1984-2001 Award Software
                          Special OEM Features

 Bootrom Os-Loader              [Disabled]          | Item Help
                                                    |
 Reset PCI-to-PCI-Bridges       [Disabled]          |
X Reset from System Master      [Enabled]           |
                                                    |
 System Slot                    Yes                 |
 RIO Board installed            No                  |
 Onboard Ethernet1              [Auto]              |
 Onboard Ethernet2              [Auto]              |
 4HP Onboard Serial Port 1      [Front]             |
 4HP Onboard Serial Port 2      Rear                |
 Board Version                  CP-303              |
 Board Index                    00                  |
 Logic Index                    00                  |
 EKS Number                     -------------       |
 EKS Index                      -------------       |
 Serial Number                  -------------       |
```

Bootrom OS-Loader

Loading for VxWorks or other OS Bootimages.

Reset PCI-to-PCI-Bridges

The BIOS may reset the PCI-to-PCI bridges in the system using a software reset mechanism. Especially when the board is used in conjunction with hot swap compatible boards elsewhere in the system, it should be disabled. Default is disabled.

Reset from System Master

Only for peripheral master CPUs (for SMs this field is disabled).

Enabled (default): When the reset button on the system master front panel, which may be, for example, a CP604, is pressed the corresponding peripheral master CP604-PM board will also perform a hardware reset.

When Disabled: The reset signal generated by the system master is ignored by the peripheral master.

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System Slot

This is a display only field. Yes indicates that this CPU is the system controller configuring the backplane and handling all interrupts relating to the backplane. No indicates that this CPU is a slave CPU.

RIO Board Installed

This is a display only field, which shows, if a RIO board is installed in the system

Onboard Ethernet1/2, 4HP Onboard Serial Port 1

This item allows EtherNet1/2 and Serial Port1 to be configured, wether they should be connected physically to the front panel (Front) or to the Rear IO-Connector (BACK)

4HP Onboard Serial Port 2

This is a display only field, which shows, that the 4HP onboard serial port 2 is physically connected to the rear IO connector.

Board Version

This is a display only field, which reflects the value of an onboard register. This must always correspond with the CPU on which the BIOS is installed.

Board Index

This is a display only field, which reflects the value of an onboard register. It shows the index of the hardware.

Logic Index

This is a display only field, which reflects the value of an onboard register. It shows the index of the onboard logic. When the Board Index is 00 this item is not displayed.

EKS Number, EKS Index, Serial Number:

This is a display only field, which shows Kontron internal information about the board. EKS-Number and EKS-Index refer to the production number and version respectively.

The serial number is unique to each board produced by Kontron. It could be used also by the customer to identify specific boards.

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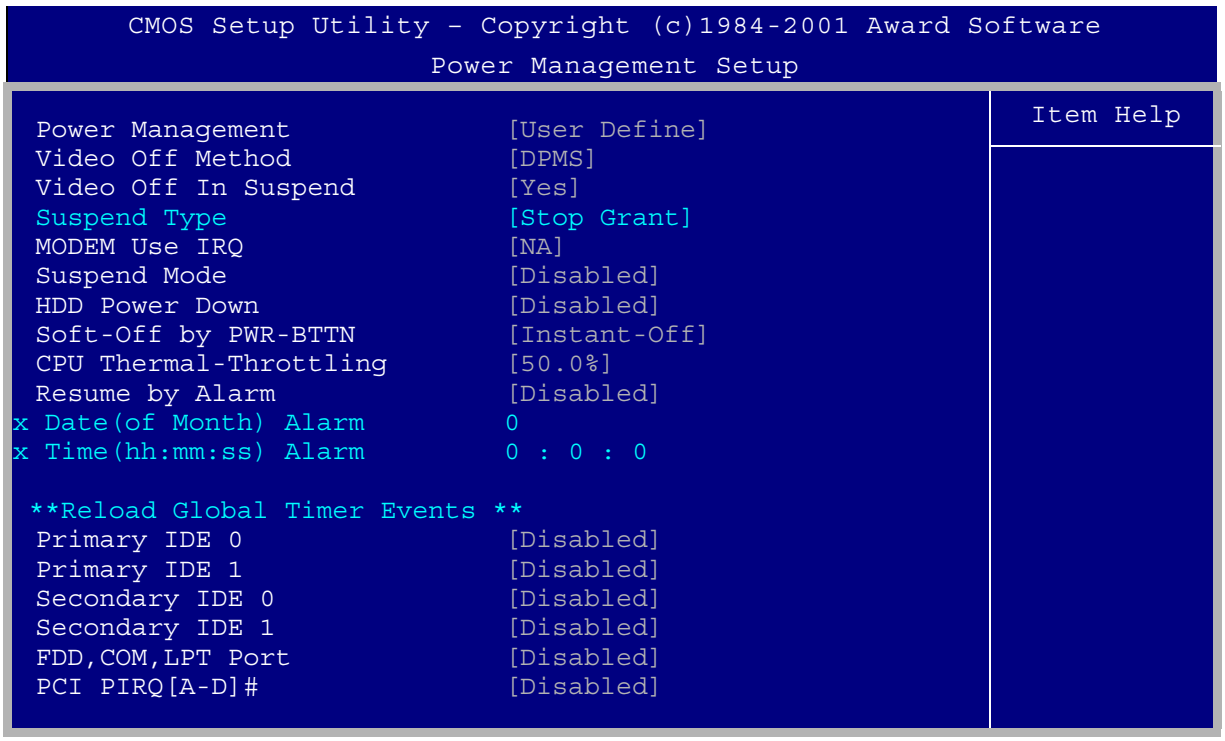
5.9 Power Management Setup

This section describes all fields presented on this screen display. Please note that your system board designer may omit or modify some of the fields described in the following.

Figure 5-10:Power Management Setup — Screen Display



Power Management

This option allows you to select the type (or degree) of power saving for Doze, Standby, and Suspend modes. See the section *PM Timers* for a brief description of each mode.

The following table describes each power management mode:

Table 5-6: Power Management Modes

Mode	Description
Maximum Saving	Maximum power savings. Inactivity period is 1 minute in each mode.
User Defined	Sets each mode individually. Select time-out periods in the *PM Timers* section, which follows.
Minimum Saving	Minimum power savings. Inactivity period is one hour in each mode (except the hard drive).

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Video-Off Method

Determines the manner in which the monitor is blanked.

Table 5-7: Video-Off Commands

Command	Description
Blank Screen	System only writes blanks to the video buffer.
V/H SYNC + Blank	System switches off vertical and horizontal synchronization ports and writes blanks to the video buffer.
DPMS Support	Select this option if your monitor supports the Display Power Management Signalling (DPMS) standard of the Video Electronics Standards Association (VESA). Use the software supplied for your video subsystem to select video power management values.

Video Off in Suspend

In this option you can choose either Yes or No and select the manner in which the monitor is switched off.

Suspend Type (display only)

Suspend Type is factory set to the function “Stop Grant” (CPU off during system inactivity).

Modem Use IRQ

Name the interrupt request (IRQ) line assigned to the modem (if any) on your system. Activity by the selected IRQ always awakens the system.

Suspend Mode

After the selected period of system inactivity (1 minute to 1 hour), all devices except the CPU shut down.

HDD Power Down

After the selected period of drive inactivity (1 to 15 minutes), the hard disk drive powers down while all other devices remain active.

Soft-Off by PWR-BTTN

When you select Instant Off or Delay 4 Sec., turning the system off with the on/off button places the system in a very low power usage state, either immediately or after 4 seconds, with only enough circuitry receiving power to detect power button activity or Resume by Ring activity.

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CPU Thermal-Throttling

When the system enters Suspend mode, the CPU clock runs only part of the time. You may select the percentage of the time that the clock runs.

Resume by Alarm

When Enabled, you can set the date and time at which the RTC (real-time clock) alarm awakens the system from suspend mode.

Date (of Month) Alarm

Select a date in the month when you want the alarm to go off. Select 0 (zero) if you prefer to set a weekly alarm

Time (hh:mm:ss) Alarm

Set the time at which you want the alarm to go off the days when it is activated.

Reload Global Timer Events

When Enabled, an event occurring on each of the devices listed below restarts the global timer for Standby mode:

- Primary EIDE 0,
- Primary EIDE 1,
- Secondary EIDE 0,
- Secondary EIDE 1,
- Floppy Disk,COM;LPT Port
- PCI PIRQ[A-D]#

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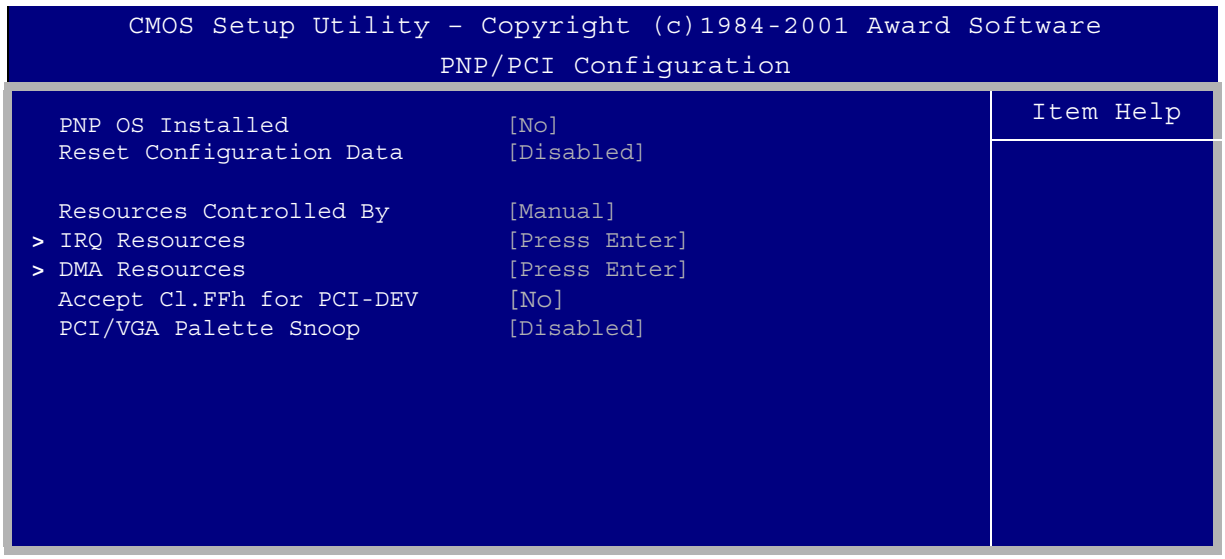
5.10 PNP/PCI Configuration

This section describes all the fields presented by this screen display. Please note that your system board designer may omit or modify some of the fields described in the following.

Figure 5-11:PNP/PCI Configuration — Screen Display



PNP OS Installed

Select “Yes” if the system operating environment is PlugandPlay aware (e.g. Win 95).

Reset Configuration Data

Normally this field is left *Disabled*. Select *Enabled* to reset Extended System Configuration Data (ESCD) when you exit Setup if you have installed a new add-on and the system re-configuration has caused such a serious conflict that the operating system cannot boot.

Resources Controlled by

The Award PlugandPlay BIOS can automatically configure all the boot and PlugandPlay-compatible devices. If you select *Auto*, all the interrupt request (IRQ) and DMA assignment fields disappear, as the BIOS automatically assigns them.

IRQ Resources

When resources are controlled manually, assign each system interrupt as one of the following types, depending on the type of device using the interrupt.

Legacy ISA	Devices compliant with the original PC AT bus specification, requiring a specific interrupt (such as IRQ4 for serial port 1).
PCI/ISA PnP	Devices compliant with the PlugandPlay standard, whether designed for PCI or ISA bus architecture.

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DMA Resources

When resources are controlled manually, assign each system interrupt as one of the following types, depending on the type of device using the interrupt.

Legacy ISA	Devices compliant with the original PC AT bus specification, requiring a specific DMA channel
PCI/ISA PnP	Devices compliant with the PlugandPlay standard, whether designed for PCI or ISA bus architecture.

Accept Class FFh for PCI-device

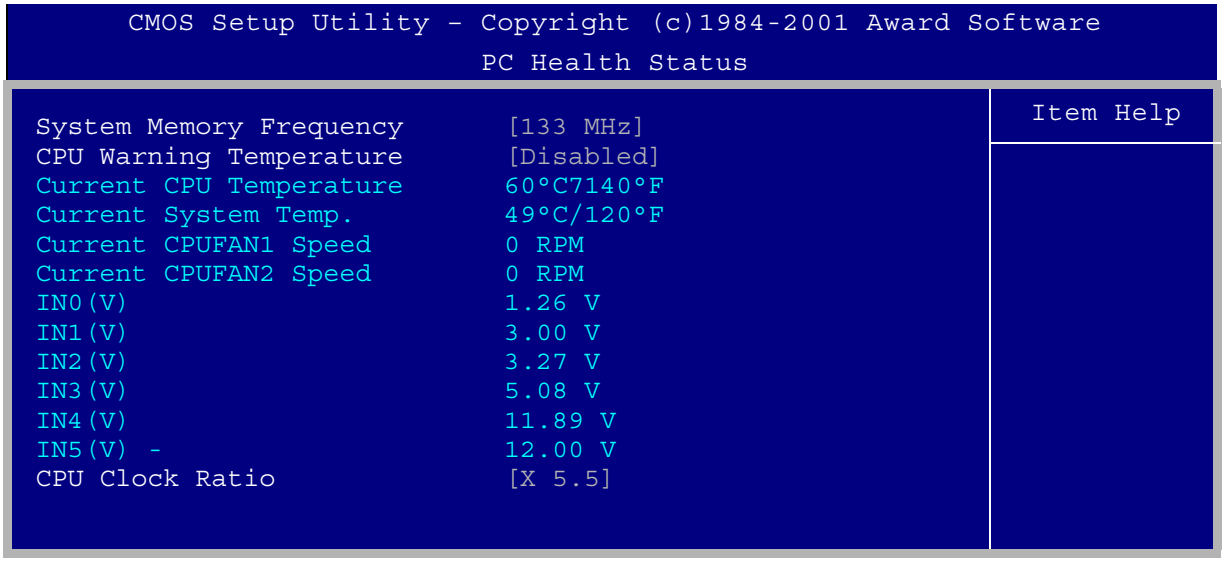
Some PCI boards use the class code 0FFh. Boards with class code FF are distributed by some vendors in the knowledge that there will be different handling of such devices. The PCI standard does not define configuration rules for class code FF. To make it transparent to the user that such a board has been identified in the system, the BIOS will display the text "Class-Code FF Device" highlighted and blinking in the PCI device list, which is displayed on system startup before booting. By setting this field to “No”, these non-standard boards will be ignored. By setting this field to “Yes”, these non-standard boards will also be configured by the BIOS and made operable.

PCI/VGA Palette Snoop

Your BIOS Setup may not contain this field. If the field is present, leave at Disabled.

5.11 PC Health Status

Figure 5-12: PC Health Status — Screen Display



System Memory Frequency

Select the bus frequency with which the CPU and the memory modules correspond. (front side bus).

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CPU Warning Temperature

Select the combination of lower and upper limits for the CPU temperature. If the CPU temperature extends beyond either limit, any warning mechanism programmed into your system will be activated.

CPU Clock Ratio

In this object you can select the proportion between the Internal (Core) and External (Bus) Frequency.

5.12 Password Setting

When you select this function, the following message appears at the center of the screen:

`Enter password:`

Type the password, up to eight characters in length, and press "↵". Typing a password clears any previously entered password from the CMOS memory.

After having pressed "↵" the message changes to:

`Confirm password:`

Type the password again and press "↵". To abort the process at any time, press "Esc".

In the "Security Option" item in the "BIOS Features Setup" screen, select `System` or `Setup`:

Note ...

To clear the password, simply press "↵" when asked to enter a password. Then the password function is disabled.

Table 5-8: Security Options

Option	Description
System	Enter a password each time the system boots and whenever you enter Setup.
Setup	Enter a password whenever you enter Setup.

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5.13 POST Messages

During the Power-on Self Test (POST), the BIOS displays a message whenever it detects a correctable error. Any error message is followed by this prompt:

```
Press "F1" to continue, "Ctrl-Alt-Esc" or "Del" to enter setup.
```

Following is a list of POST error messages for both the ISA and the EISA BIOS.

CMOS Battery Has Failed

The CMOS battery is no longer functional. It should be replaced.

CMOS Checksum Error

Checksum of CMOS is incorrect. This can indicate that the CMOS has become corrupted. This error may have been caused by a weak battery. Check the battery and replace it, if necessary.

Disk Boot Failure, Insert System Disk and Press Enter

No boot device was found. This could mean that either a boot drive was not detected or that the drive does not contain proper system boot files. Insert a system disk into
Drive A: and press <Enter>. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also be sure the disk is formatted as a boot device. Then reboot the system.

Diskette Drives or Types Mismatch Error - Run Setup

Type of floppy-disk drive installed in the system is different from the CMOS definition. Run "Setup" to reconfigure the drive type correctly.

Display Switch is Set Incorrectly

Display switch on the motherboard can be set to either monochrome or color. This error message indicates that the switch has a setting other than that indicated in Setup. Determine which setting is correct, and then either turn off the system and change the jumper, or enter Setup and change the video selection.

Display Type Has Changed Since Last Boot

Since the last powering-down of the system, the display adapter has been changed. You must configure the system for the new display type.

EISA Configuration Checksum Error - Please Run EISA Configuration Utility

The EISA non-volatile RAM checksum is incorrect or cannot correctly read the EISA slot. This can indicate either the EISA non-volatile memory has become corrupted or the slot has been configured incorrectly. Ensure also that the card is installed firmly in the slot.

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EISA Configuration Is Not Complete - Please Run EISA Configuration Utility

The slot configuration information stored in the EISA non-volatile memory is incomplete.

Note ...

When either of the above EISA error messages appears, the system boots in ISA mode so that you can run the EISA Configuration Utility.

Error Encountered Initializing Hard Drive

Hard drive cannot be initialized. Make sure that the adapter is installed correctly and that all cables are correctly and firmly attached. Ensure also that the correct hard drive type is selected in “Setup”.

Error Initializing Hard Disk Controller

Cannot initialize controller. Make sure that the cord is correctly and firmly installed in the bus. Ensure also that the correct hard drive type is selected in Setup. Also check to see if any jumper needs to be set correctly on the hard drive.

Floppy-Disk Controller Error or No Controller Present

Cannot find or initialize the floppy drive controller. Make sure that the controller is installed correctly and firmly. If there are no floppy drives installed, ensure that the floppy-disk drive selection in “Setup” is set to `NONE`.

Invalid EISA Configuration - Please Run EISA Configuration Utility

The non-volatile memory containing EISA configuration information was programmed incorrectly or has become corrupted. Re-run EISA configuration utility to correctly program the memory.

Note ...

When this error appears, the system boots in ISA mode so that you can run the EISA configuration utility.

Keyboard Error or No Keyboard Present

Cannot initialize the keyboard. Make sure that the keyboard is attached correctly and that no keys are being pressed during the boot process.

If you are deliberately configuring the system without a keyboard, set the “Error Halt” condition in “Setup” to `HALT ON ALL, BUT KEYBOARD`. This causes the BIOS to ignore the missing keyboard and continue the boot process.

Memory Address Error at ...

Indicates a memory address error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory chips.

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Memory Parity Error at ...

Indicates a memory parity error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory chips.

Memory Size Has Changed Since Last Boot

Memory has been added or removed since the last boot. In EISA mode use the configuration utility to reconfigure the memory configuration. In ISA mode enter “Setup” and enter the new memory size into the memory fields.

Memory Verify Error at ...

Indicates an error verifying a value already written to memory. Use the location along with your system's memory map to locate the bad chip.

Offending Address not Found

This message is used in conjunction with the “I/O Channel Check” and “RAM Parity Error” messages whenever the segment that has caused the problem cannot be isolated.

Offending Segment

This message is used in conjunction with the “I/O Channel Check” and “RAM Parity Error” messages whenever the segment that has caused the problem has been isolated.

Press a Key to Reboot

This message appears at the bottom of the screen when an error occurs that requires you to reboot. Press any key to reboot the system.

Press “F1” to Disable NMI, “F2” to Reboot

When the BIOS detects a non-maskable interrupt condition during boot, you can disable the NMI and continue to boot, or you can reboot the system with the NMI enabled.

RAM Parity Error - Checking for Segment ...

Indicates a parity error in the random access memory.

Should Be Empty But EISA Board Found - Please Run EISA Configuration Utility

A valid board ID was found in a slot that was configured as having no board ID.

Note ...

When this error appears, the system boots in ISA mode so that you can run the EISA configuration utility.

Should Have EISA Board but not Found - Please Run EISA Configuration Utility

The board installed is not responding to the ID request, or no board ID has been found in the indicated slot.

Note ...

When this error appears, the system boots in ISA mode so that you can run the EISA configuration utility.

Slot not Empty

Indicates that a slot designated as empty by the EISA Configuration Utility actually contains a board.

Note ...

When this error appears, the system boots in ISA mode so that you can run the EISA configuration utility.

System Halted, <CTRL-ALT-DEL> to Reboot ...

Indicates that the present boot attempt has been aborted and that the system must be rebooted. Press and hold down the “CTRL” and “ALT” keys and press “DEL”.

Wrong Board in Slot - Please Run EISA Configuration Utility

The board ID does not match the ID stored in the EISA non-volatile memory.

Note ...

When this error appears, the system boots in ISA mode so that you can run the EISA configuration utility.

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5.14 POST Codes

ISA and PCI POST codes are routed to port address 80H.

Table 5-9: Early POST Codes before System BIOS is Shadowed

POST Code	Action
Reset	RTC& KBC initialization
0CFh	Early CPU Detection
0C0h	Early Chipset initialization
0C1h	Memory presence test: detects memory modules and programs chipset accordingly
0C3h	Decompresses Bios
0C5h	Shadows Main Bios and jumps to POST

Table 5-10: Normal POST Codes after System BIOS is Shadowed

POST Code	Action
02h	- Jump to E000 segment - Commences execution of POST routines in E000 - Starting with POST 3h
03h	Early initialization of Super I/O
04h	Reserved
05h	Blank Video, reset video controller
06h	Reserved
07h	Initialize Keyboard Controller
08h	Keyboard Test
09h	Reserved
0Ah	Mouse Initialization
0Bh	Reserved
0Ch	Reserved
0Dh	Reserved
0Eh	Checksum ROM, verify Shadow
0Fh	Reserved

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Table 5-10: Normal POST Codes after System BIOS is Shadowed (Continued)

POST Code	Action
10h	Detect EEPROM
11h	Reserved
12h	Test and Reset CMOS
13h	Reserved
14h	Load Chipset Defaults
15h	Reserved
16h	Initialize onboard clock generator
17h	Reserved
18h	CPU ID and initialize L1/L2 Cache
19h	Reserved
1Ah	Reserved
1Bh	Initialize interrupt vector table
1Ch	Test CMOS and Check Battery Fail
1Dh	Early PM initialization
1Eh	Reserved
1Fh	Load Keyboard Matrix
20h	Reserved
21h	Init Heuristic Power Management (HPM)
22h	Reserved
23h	Early Prog chipset (PM) registers
24h	Init PNP
25h	Shadow system/video BIOS
26h	Init onboard clock generator and sensor
27h	Setup BIOS DATA AREA (BDA)
28h	Reserved
29h	Chipset programming and Cpu Speed detect
2Ah	Reserved

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Table 5-10: Normal POST Codes after System BIOS is Shadowed (Continued)

POST Code	Action
2Bh	Initialize Video
2Ch	Reserved
2Dh	Test Video Memory and display Logos
2Eh	Reserved
2Fh	Reserved
32h	Reserved
33h	Early Keyboard Reset
34h	Reserved
35h	Test DMA channel 0
36h	Reserved
37h	Test DMA channel 1
38h	Reserved
39h	Test DMA Page Registers
3Ah	Reserved
3Bh	Reserved
3Ch	Test 8254 chip
3Dh	Reserved
3Eh	Test 8259 Channel 1 mask bits
3Fh	Reserved
40h	Test 8259 channel 2 mask bits
41h	Reserved
42h	Reserved
43h	Test 8259 functionality
44h	Reserved
45h	Reinitialize Preboot agent serial port
46h	Reserved
47h	EISA test (if applicable)

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Table 5-10: Normal POST Codes after System BIOS is Shadowed (Continued)

POST Code	Action
48h	Reserved
49h	Size base and extended memory
4Eh	Initialize APIC and set MTRR
4Fh	Reserved
50h	USB Initialization
51h	Reserved
52h	Memory Test
53h	Reserved
54h	Reserved
55h	Display CPU type string
56h	Reserved
57h	Early PNP Init and Display PNP logo
58h	Reserved
59h	Initialize Trend Antivirus
5Ah	Reserved
5Bh	Auto Load Awdflash (optional)
5Ch	Reserved
5Dh	Initialize onboard IO
5Eh	Reserved
5Fh	Reserved
60h	Display Setup message and enable Setup functions
61h	Reserved
62h	Reserved
63h	Check for PS2 mouse and reset keyboard
64h	Reserved
65h	Install Mouse
66h	Reserved

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Table 5-10: Normal POST Codes after System BIOS is Shadowed (Continued)

POST Code	Action
67h	ACPI sub-system initialization
68h	Reserved
69h	Initialize Cache
6Ah	Reserved
6Bh	Enter Setup check and auto config prog.
6Ch	Reserved
6Dh	Initialize floppy controller
6Eh	Reserved
6Fh	Install FDDs
70h	Reserved
71h	Reserved
72h	Reserved
73h	Initialize IDE controller
74h	Reserved
75h	Detect IDE devices
76h	Reserved
77h	Initialize serial ports
78h	Reserved
79h	Reserved
7Ah	Initialize Parallel Ports
7Bh	Reserved
7Ch	HDD write protect (optional)
7Dh	Reserved
7Eh	Reserved
7Fh	Check and Display POST error messages
80h	Reserved
81h	Reserved

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Table 5-10: Normal POST Codes after System BIOS is Shadowed (Continued)

POST Code	Action
82h	Password Check
83h	Write CMOS back to RAM
84h	Display PNP devices detected
85h	USB Final Initialisation
86h	Reserved
87h	Reserved
88h	Reserved
89h	Setup ACPI tables
8Ah	Reserved
8Bh	Scan for Option ROMs
8Ch	Reserved
8Dh	Enable parity check
8Eh	Reserved
8Fh	Enable IRQ12 if mouse present
90h	Reserved
91h	Reserved
92h	Reserved
93h	Read and store boot partition info in RAM
94h	Final Init – for last minute details
95h	Set NUMLOCK status
96h	Set Low Stack and BOOT via INT 19h

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Appendix A

IDE1 Module

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A. IDE1 Module

A.1 Overview

The Kontron CP303-IDE1 module has been designed to make all PC legacy I/O ports accessible to the user and includes two COM ports, a PS/2 keyboard and mouse port, a parallel port, floppy and hard disk interfaces. This additional capability opens up the broadest range of expansion possibilities.

The connectors for the two COM ports, the PS/2 keyboard and mouse are situated at the front panel, while the floppy, hard disk and LPT1 connector can be attached on the onboard connectors. The module connects to the CP303 across an I/O extension connector.

The I/O extension connector provides the possibility to mount several Low Pin Count (LPC) devices to the CP303 for adding additional functionality which is not provided on the CP303 main board.

A.2 Technical Specifications

Table A-1: CP303-IDE1 Module Main Specifications

	CP303-IDE1	Specifications
Controller	Super I/O Controller	The LPC47M107 from SMSC is an LPC Plug and Play compatible I/O device that provides functions for serial interfacing, parallel interfacing and floppy disk interfacing.
External Interfaces	Keyboard and Mouse Interface	PS/2 type, 6-pin, shielded mini-DIN connector for the keyboard and mouse (via Y-cable)
	Floppy	One floppy disk interface (up to 2.88 MB) on 34-pin 2.54mm connector
	Serial Port	Up to two UARTs, 16C550 compatible COM1/2 RS-232/RS422/RS485 two 9-pin D-SUB connector
	Parallel port	IEEE 1284; SPP/EPP/ECP parallel mode 26-pin connector
Internal Interfaces	EIDE interface	One EIDE interface supporting Ultra ATA/100/66/33 for 2 hard disks or CD-ROM on 40-pin 2.54mm or 44-pin 2mm onboard connector
Indicators / Switches	LEDs	One LED (green) monitors hard disk activity
	Switches, Front Panel	Reset button, guarded
General	Power Consumption	3.3 V at 100 mW 5.0 V at 100 mW (without hard disk)
	Temperature Range	Operating temp.: 0°C to +60°C E1 (optional): -25°C to +75°C E2 (optional): -40°C to +85°C Storage temp.: -55°C to +85°C
	Humidity	Climatic humidity: 93% RH at 40 °C, non-condensing
	Dimensions	Dimensions: 100 mm x 160 mm
	Board Weight	CP303 8HP with heat sink: 146 grams (without hard disk)

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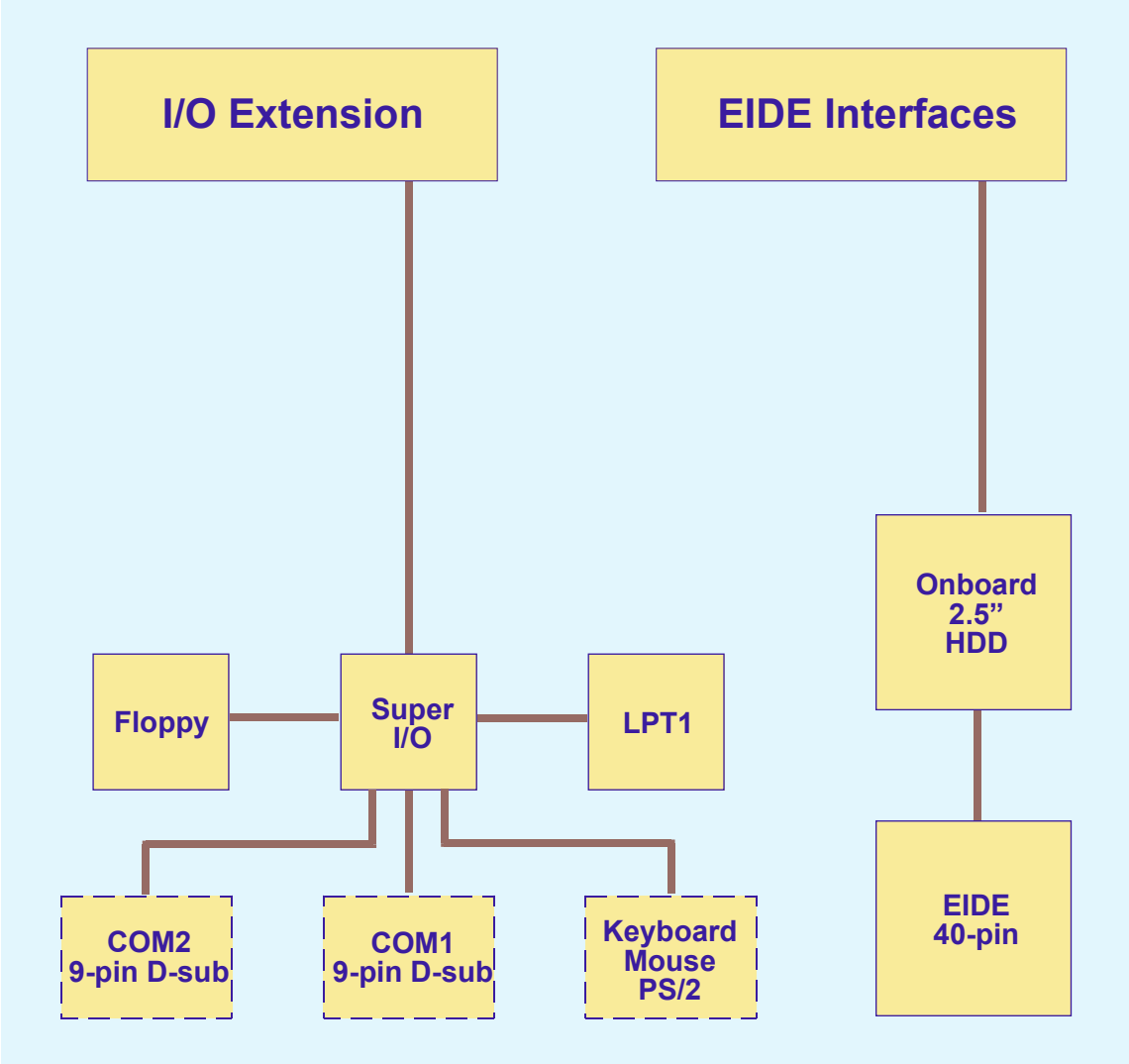
A.3 CP303-IDE1 Module Functional Block Diagram

Figure A-1: CP303-IDE1 Module Functional Block Diagram



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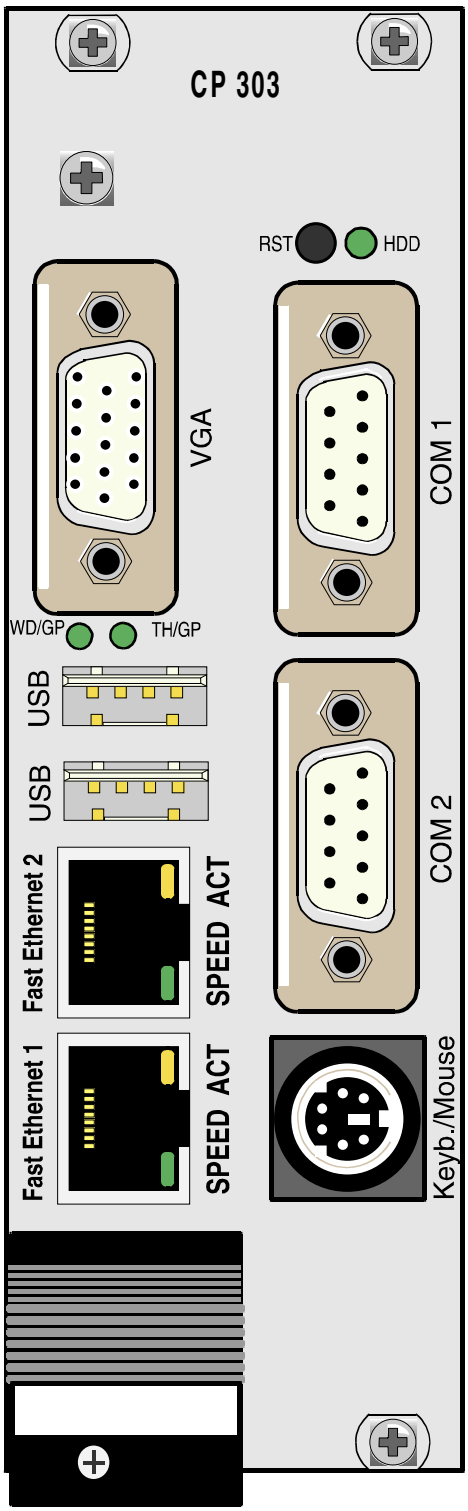
A.4 CP303-IDE1 Module Front Panel

Figure A-2: CP303-IDE1 Module Front Panel



LEGEND:

General Purpose LEDs

- WD/GP (green): Watchdog or General Purpose
- TH/GP (green): Overtemperature Status or General Purpose
- HDD (green): Monitors hard disk activity

Reset Button

- RST = reset button

Integral Ethernet LEDs

- ACT (yellow): Ethernet Link/Activity
- SPEED (green): Ethernet Speed

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A.5 CP303-IDE1 Module Layout

The transition module includes additional standard PC interfaces, two configurable COM ports and one ECP/EPP compatible Parallel Port.

A.5.1 CP303-IDE1 Module Layout

Figure A-3: CP303-IDE1 Module Layout (Front Side)

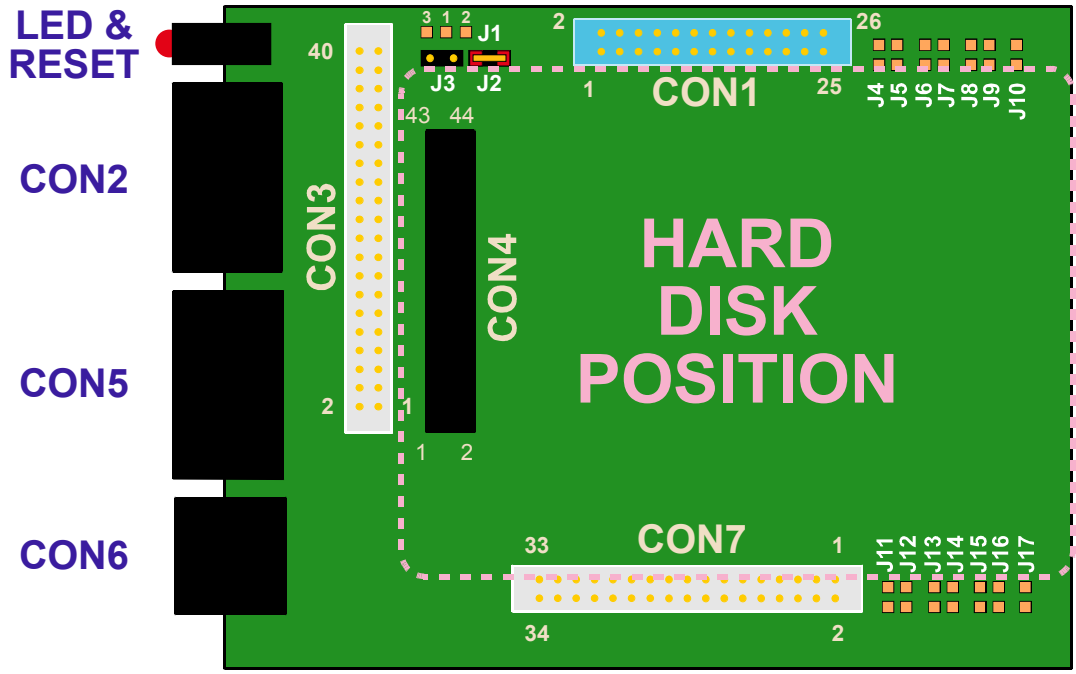
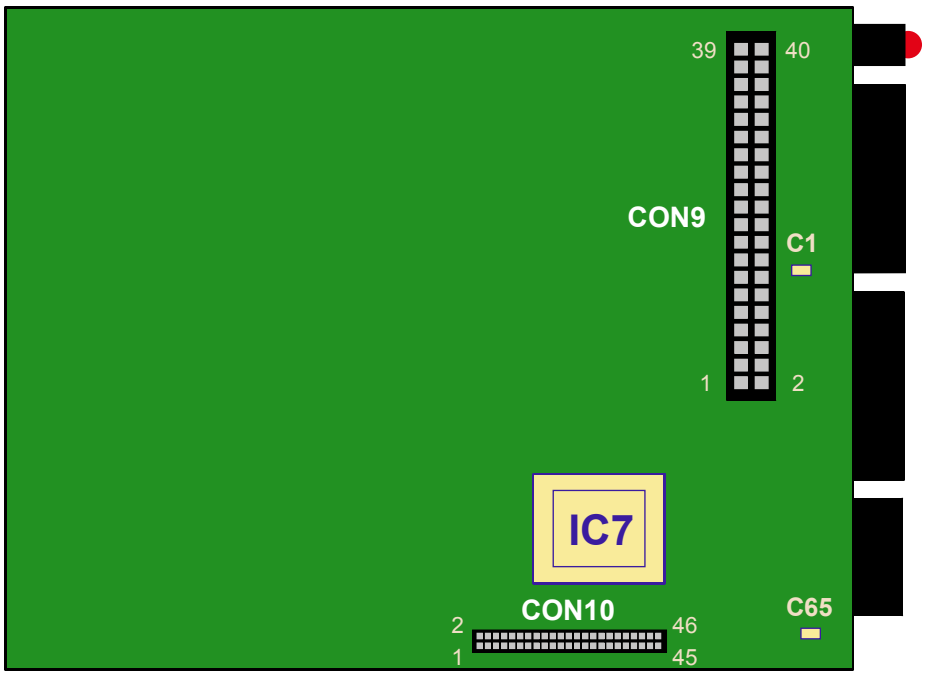


Figure A-4: CP303-IDE1 Module Layout (Reverse Side)



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A.6 Module Interfaces (Front Panel and Onboard)

A.6.1 Keyboard/Mouse Interface

The onboard keyboard controller is 8042 software compatible.

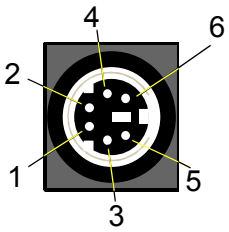
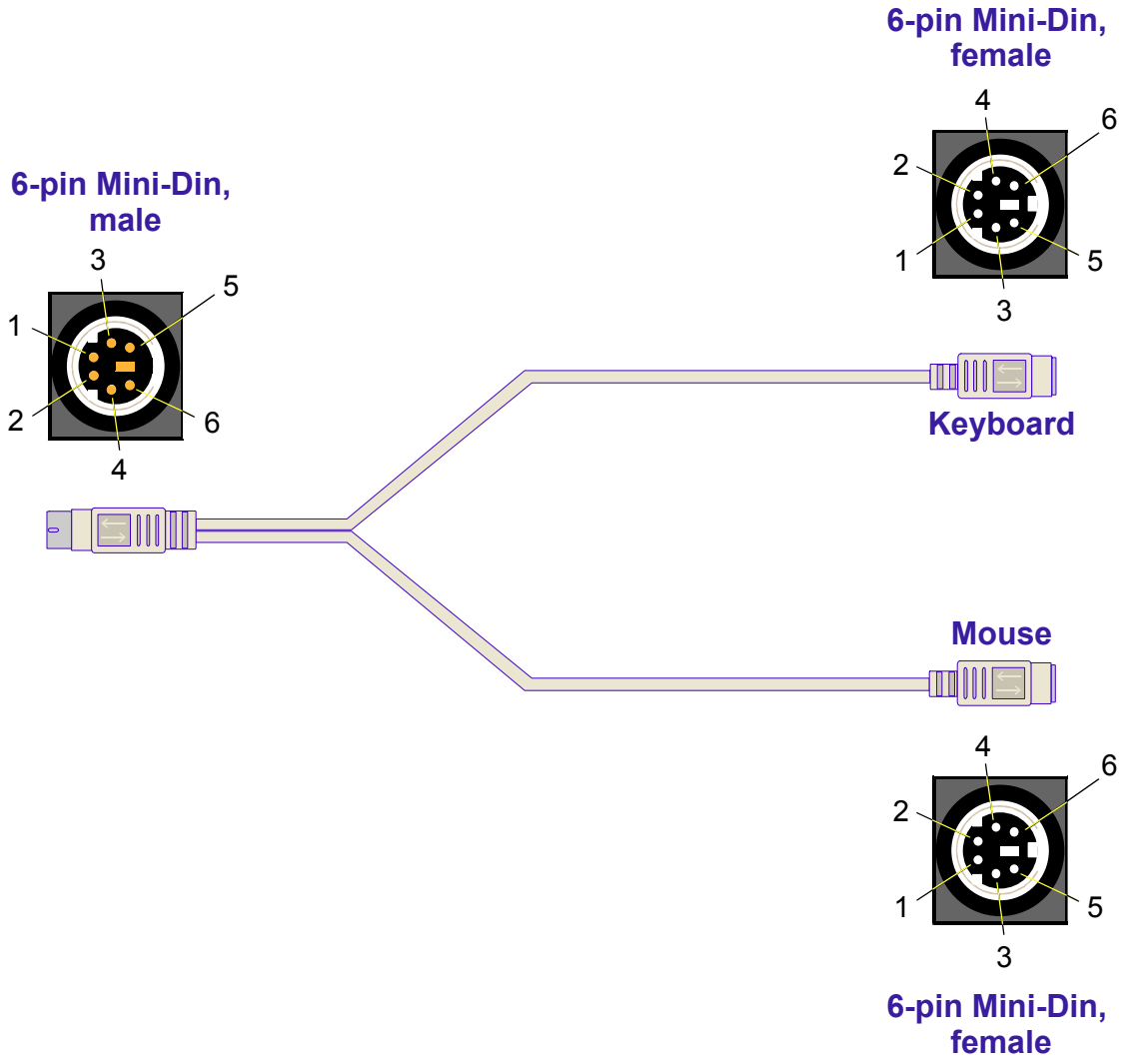


Figure A-5:Keyboard/Mouse Connector

The PC/AT standard keyboard/mouse connector is a PS/2-type 6-pin shielded Mini-DIN connector. The keyboard power supply unit is protected by a 500 mA fuse. All signal lines are EMI-filtered.

A special adapter to connect a mouse device and/or a keyboard to the PS/2 connector is available from *Kontron Modular Computers.*

Figure A-6: Adapter for Connecting Mouse/Keyboard via PS/2



A.6.1.1 Keyboard Connector CON6 Pinout

The CP303 has the AT keyboard connector implemented on a 6-pin Mini-Din connector.

Table A-2: Keyboard Connector CON6 Pinout

Pin Number	Signal	Function	In/Out
1	KDATA	Keyboard data	In/Out
2	MDATA	Mouse data	In/Out
3	GND	Ground signal	--
4	VCC	VCC signal	--
5	KCLK	Keyboard clock	Out
6	MCLK	Mouse clock	Out

Note ...

The keyboard power supply is protected with a fuse (500mA) and all the signal lines are EMI-filtered.

A.6.2 Universal Serial Ports (UART)

Two PC-compatible serial 9-pin DSUB ports are available with 5V charge-pump technology eliminating the need for a +12V and -12V supply. The two COM ports, which are fully compatible with the 16550 controller, include a complete set of handshaking and modem control signals, maskable interrupt generation and data transfer of up to 460.8 kB/s.

The two COM interfaces may be configured as RS232, RS422 or RS485 ports by setting the appropriate solder jumpers. The standard setting of the two COM ports envisages the RS232 configuration.

RS-422 configuration:

The RS-422 interface use two differential data lines RX and TX for communication (Full-Duplex)

RS-485 configuration:

The RS-485 interface use one differential data line. It differs from the RS-422 modes in that it provides the ability to transmit and receive over the same wire. The RTS signal is used to control the direction of the RS-485 buffer.

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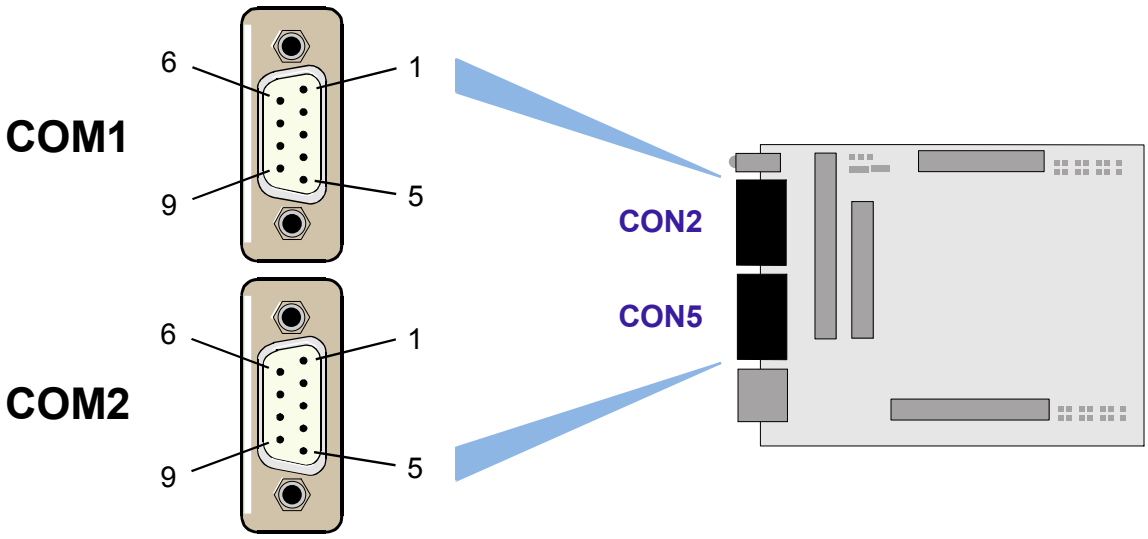
Figure A-7: PC-Compatible D-SUB Serial Interface Connectors CON2 and CON5



A.6.2.1 Serial Port Connectors CON2 and CON5 Pinouts

The pinout of the 9-pin D-SUB connectors depends on the configuration.

The COM1 interface is routed to the connector CON2 and the COM2 interface is routed to CON5.

Note ...

The RS422 connector is *Kontron*-specific and the serial control signals are not available.

Table A-3: Serial Port Connectors CON2 and CON5 Pinouts

Pin Number	RS232 (Standard PC)	RS422	RS485
1	DCD	+RXD	NC
2	RXD	NC	NC
3	TXD	+TXD	+TRXD
4	DTR	NC	NC
5	GND	GND	GND
6	DSR	-RXD	NC
7	RTS	NC	NC
8	CTS	-TXD	-TRXD
9	RIN	NC	NC

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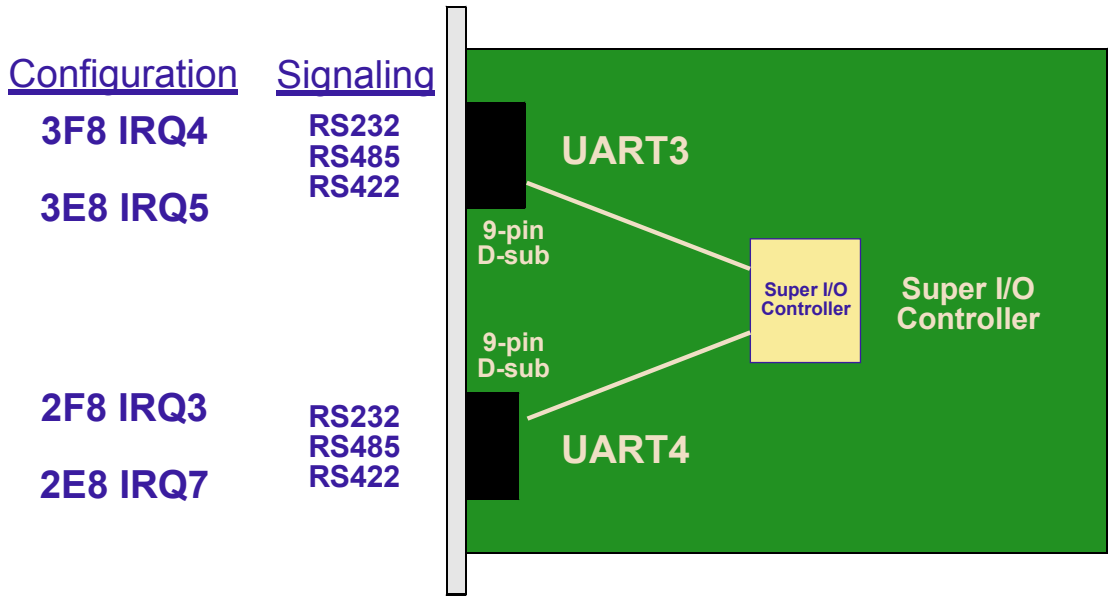
A.6.2.2 Serial Port Configuration

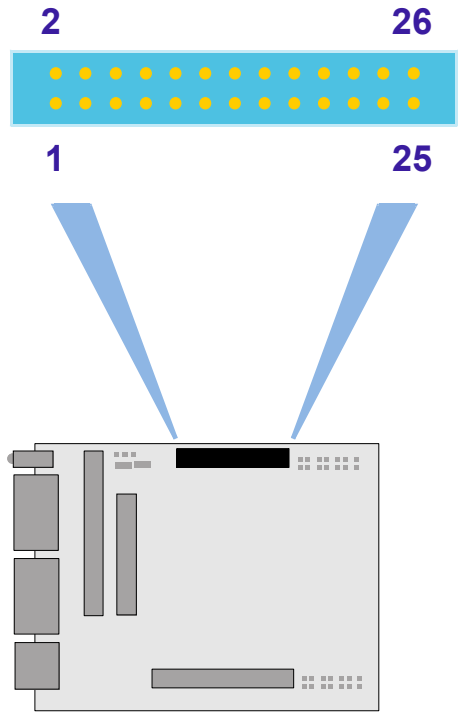
Figure A-8: Serial Port Configuration Diagram



A.6.3 Parallel Port Interface

The CP303-IDE1 module is provided with an IEEE1284, ECP/EPP-compatible parallel port/ printer interface. The parallel port is a 26-pin 2.54mm connector. To use a standard parallel port device a special adapter is necessary.

Figure A-9: PC-Compatible Parallel Interface Connector CON1



A.6.3.1 Parallel Port Connector CON1 Pinout

The CP303-IDE1 module is provided with a PC-compatible 26-pin MDR connector CON1.

Table A-4: 26-Pin MDR Connector Pinout

PIN	SIGNAL	FUNCTION	IN/OUT	PIN	SIGNAL	FUNCTION	IN/OUT
2	-AFD	Auto feed	Out	1	-STB	Strobe data	Out
4	-ERR	Printer error	In	3	PD0	LSB of printer data	Out
6	-INIT	Initialize printer	Out	5	PD1	Printer data 1	Out
8	-SLIN	Select printer	Out	7	PD2	Printer data 2	Out
10	GND	Signal ground	N/A	9	PD3	Printer data 3	Out
12	GND	Signal ground	N/A	11	PD4	Printer data 4	Out
14	GND	Signal ground	N/A	13	PD5	Printer data 5	Out
16	GND	Signal ground	N/A	15	PD6	Printer data 6	Out
18	GND	Signal ground	N/A	17	PD7	Printer data 7	Out
20	GND	Signal ground	N/A	19	-ACK	Character accepted	In
22	GND	Signal ground	N/A	21	BSY	Busy	In
24	GND	Signal ground	N/A	23	PE	Paper end	In
26	GND	Signal ground	N/C	25	SLCT	Ready to receive	In

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A.6.4 EIDE Interface (Secondary Port)

The EIDE interface on the CP303-IDE1 module comprises three connectors, CON3, CON4 and CON9. The CON9 connector, situated on the reverse of the board, is used to connect the CP303-IDE1 module to the baseboard, while the other two connectors, CON3 and CON4, are used to connect devices to the CP303-IDE1 module.

Figure A-10: Front Side EIDE Interface Connectors CON3 and CON4

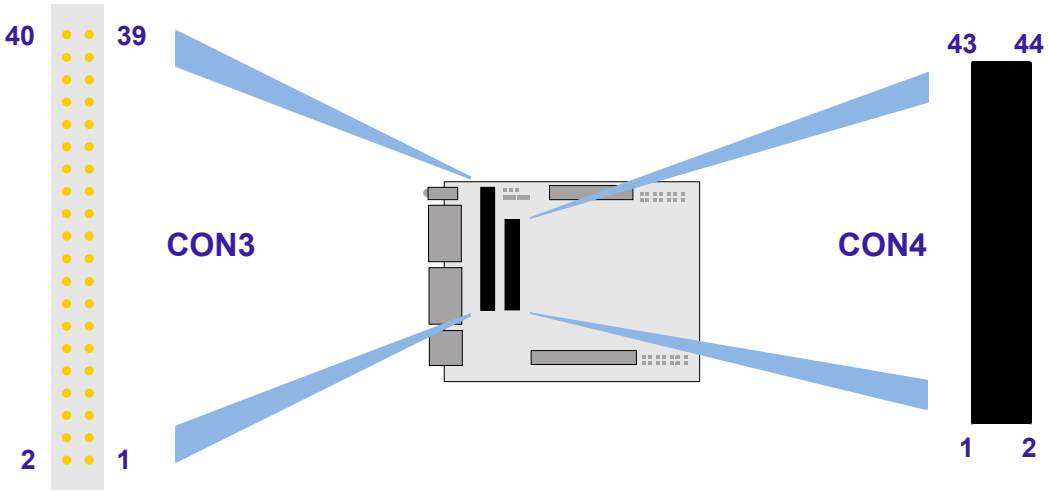
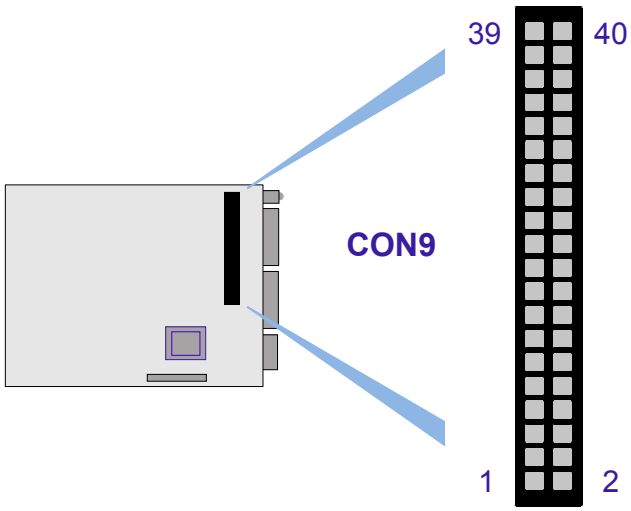


Figure A-11: Rear Side EIDE Interface Connector CON9



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CON4 is a 44-pin 2mm pinrow connector while CON3 is a standard 40-pin 2.54mm pinrow connector. Up to two devices (which must be master/slave pairs) may be attatched to the CP303-IDE1 board; either both devices on CON3 or on CON4 or one device on each connector. The maximum length of cable that may be used for CON4 is 25 cm.

Note ...

ATA-66 and ATA-100 are faster timings and require a specialized cable which has additional grounding wires to reduce reflections, noise, and inductive coupling. This cable will also support all legacy IDE drives.

The onboard 2.5" hard disk or Flash disk (CON4) must be configured as a MASTER device. Due to the ATA100 cable specification the board does not support a 2.5" slave device and a master device on CON3.

The blue end of the ATA-100 cable must connect to the motherboard, the gray connector to the UltraDMA /100 slave device and the black connector to the UltraDMA/100 master device.

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A.6.4.1 Onboard EIDE Connector CON4 Pinout

A 2.5” hard disk or Flash disk may be mounted directly onto the CP303-IDE1 module using the 44-pin connector CON4.

Table A-5: Pinout of the AT 44-pin Connector

Pin Number	Signal	Function	In/Out
1	IDERESET	Reset HD	Out
2	GND	Ground signal	--
3	HD7	HD data 7	In/Out
4	HD8	HD data 8	In/Out
5	HD6	HD data 6	In/Out
6	HD9	HD data 9	In/Out
7	HD5	HD data 5	In/Out
8	HD10	HD data 10	In/Out
9	HD4	HD data 4	In/Out
10	HD11	HD data 11	In/Out
11	HD3	HD data 3	In/Out
12	HD12	HD data 12	In/Out
13	HD2	HD data 2	In/Out
14	HD13	HD data 13	In/Out
15	HD1	HD data 1	In/Out
16	HD14	HD data 14	In/Out
17	HD0	HD data 0	In/Out
18	HD15	HD data 15	In/Out
19	GND	Ground signal	--
20	N/C	--	--
21	IDEDRQ	DMA request	In
22	GND	Ground signal	--
23	IOW	I/O write	Out
24	GND	Ground signal	--
25	IOR	I/O read	Out
26	GND	Ground signal	--
27	IOCHRDY	I/O channel ready	In
28	GND	Ground signal	--
29	IDEDACKA	DMA Ack	Out
30	GND	Ground signal	--
31	IDEIRQ	Interrupt request	In
32	N/C	--	--
33	A1	Address 1	Out
34	ATA66	Detect ATA66	In
35	A0	Address 0	Out
36	A2	Address 2	Out
37	HCS0	HD select 0	Out
38	HCS1	HD select 1	Out
39	LED	LED driving	In
40	GND	Ground signal	--
41	VCC	5V power	--
42	VCC	5V power	--
43	GND	Ground signal	--
44	N/C	--	--

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A.6.4.2 EIDE Connectors CON3 and CON9 Pinouts

A wide range of EIDE devices may be connected to the CP303-IDE1 module at CON3 using a ribbon cable.

The following table describes the pinouts of connectors CON3 and CON9, which are identical, with the corresponding signal names.

Table A-6: Pinouts of EIDE Connectors CON3 and CON9

Pin Number	Signal	Function	In/Out
1	IDERESET	Reset HD	Out
2	GND	Ground signal	--
3	HD7	HD data 7	In/Out
4	HD8	HD data 8	In/Out
5	HD6	HD data 6	In/Out
6	HD9	HD data 9	In/Out
7	HD5	HD data 5	In/Out
8	HD10	HD data 10	In/Out
9	HD4	HD data 4	In/Out
10	HD11	HD data 11	In/Out
11	HD3	HD data 3	In/Out
12	HD12	HD data 12	In/Out
13	HD2	HD data 2	In/Out
14	HD13	HD data 13	In/Out
15	HD1	HD data 1	In/Out
16	HD14	HD data 14	In/Out
17	HD0	HD data 0	In/Out
18	HD15	HD data 15	In/Out
19	GND	Ground signal	--
20	N/C	--	--
21	IDEDRQ	DMA request	In
22	GND	Ground signal	--
23	IOW	I/O write	Out
24	GND	Ground signal	--
25	IOR	I/O read	Out
26	GND	Ground signal	--
27	IOCHRDY	I/O channel ready	In
28	GND	Ground signal	--
29	IDEDACKA	DMA Ack	Out
30	GND	Ground signal	--
31	IDEIRQ	Interrupt request	In
32	N/C	--	--
33	A1	Address 1	Out
34	ATA66	Detect ATA66	In
35	A0	Address 0	Out
36	A2	Address 2	Out
37	HCS0	HD select 0	Out
38	HCS1	HD select 1	Out
39	LED	LED driving	In
40	GND	Ground signal	--

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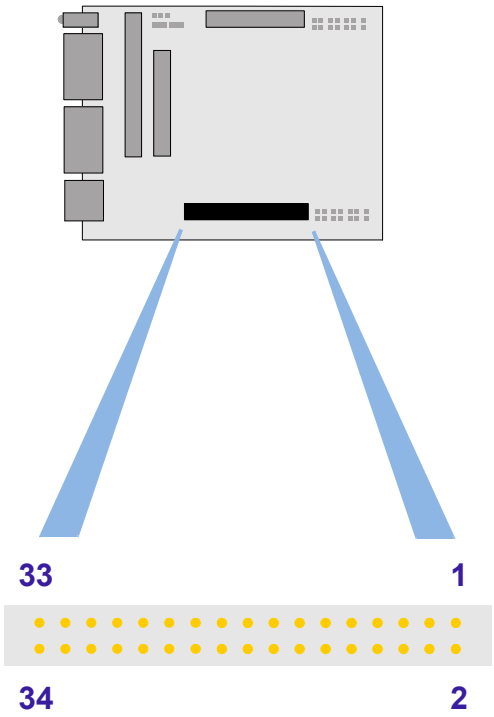
A.6.5 Floppy Drive Interface

The floppy drive interface CON7 of the CP303-IDE1 module is realized as a 34-pin, 2.54-mm pitch pin row connector.

Figure A-12: Floppy Drive Interface Connector CON7



Warning!

If the floppy drive connection cable is inverted (pin “1” in place of pin “34”) at “power on”, the floppy drive will work uninterruptedly, with consequent risk of damaging the floppy disk inserted.

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A.6.5.1 Floppy Drive Connector CON7 Pinout

Please note that all odd numbered pins are used as GND (ground signal)

Table A-7: Floppy Drive Connector CON7 Pinout

Pin Number	Signal	Function	In/out
2	RWC	Write precompensation	Out
4	N/C	--	--
6	N/C	--	--
8	INDEX	Index pulse	In
10	MOTEN1	Motor 1 enable	Out
12	DRVSEL2	Driver select 2	Out
14	DRVSEL1	Driver select 1	Out
16	MOTEN2	Motor 2 enable	Out
18	DIRECTION	Step direction	Out
20	STEP	Step pulse	Out
22	WRDATA	Write data	Out
24	WREN	Write enable	Out
26	TRACK0	Track 0 signal	In
28	WRPROT	Write protect	In
30	RDDATA	Read data	In
32	HEADSEL	Head select	Out
34	DSKCHG	Disk change	In
ODD NUMBERS.	GND	Ground signal	--

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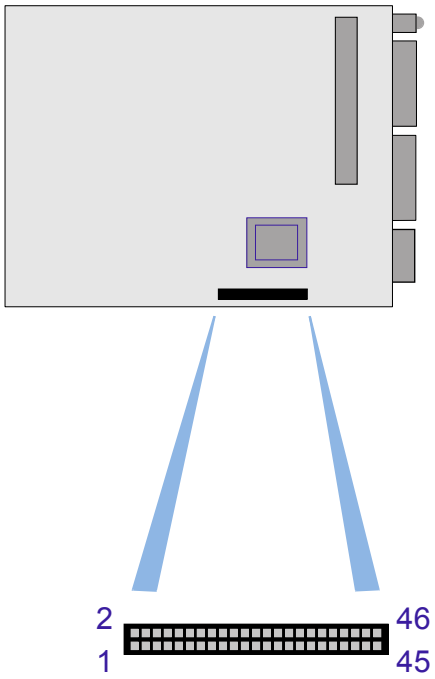
A.6.6 I/O Extension Interface Connector CON10

The I/O interface connector CON10 provides all the necessary signals for the CP303-IDE1 module.

Figure A-13: I/O Extension Interface Connector CON10



A.6.7 Speaker Connector J3

This 2-pin connector enables connection to an external speaker.

A.6.8 Reserved Jumpers

Jumpers J1 and J2 are non-system relevant.

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A.7 Jumper Description

A.7.1 Shorting Chassis GND (Shield) to Logic GND

The front panel and front panel connectors are isolated to the logic ground.

To enable the connection between the chassis GND and logic GND the capacitors must be exchanged with zero ohm resistors.

Table A-8: Shorting Chassis GND (Shield) to Logic GND

CAPACITOR	SETTING	DESCRIPTION
C1, C65	*Closed 470pF 2KV capacitors*	*Connectors are isolated to logic GND with three 470pF 2KV capacitors*
	Closed zero ohm resistors	Connectors are connected to logic GND and chassis GND

The default setting is indicated by italics.

A.7.2 Serial Port Setting

The serial interfaces CON2 (COM1) and CON5 (COM2) on the CP303-IDE1 module may be configured for either RS232, RS422 or RS485 by setting solder jumpers.

Table A-9: Jumper Setting to Configure COM1

Jumper	RS232 (default)	RS422	RS485	Disabled
J4	Open	Closed	Open	Open
J5	Open	Open	Closed	Open
J8	Open	Closed	Closed	Closed
J9	Open	Closed	Closed	Open
J10	Open	Closed	Open	Open

Table A-10:Jumper Setting to Configure COM2

Jumper	RS232 (default)	RS422	RS485	Disabled
J11	Open	Closed	Open	Open
J12	Open	Open	Closed	Open
J15	Open	Closed	Closed	Open
J16	Open	Closed	Closed	Closed
J17	Open	Closed	Open	Open

The default configuration is RS232.

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A.7.2.1 RS422 and RS485 COM1 Termination

When the CP303-IDE1 module is using the onboard RS485 interface and is the last on the RS422 or RS485 bus, then the RS422 or RS485 interface must provide termination resistance. The purpose of jumpers J6 and J7 are to enable this line termination resistor (120 R).

Table A-11: Jumper Settings for RS422 RXD Termination (COM1)

Termination	J6
ON	Closed
OFF	Open

Table A-12: Jumper Settings for RS422 TXD and RS485 Termination (COM1)

Termination	J7
ON	Closed
OFF	Open

A.7.2.2 RS422 and RS485 COM2 Termination

When the CP303-IDE1 module is using the onboard RS485 interface and is the last on the RS422 or RS485 bus, then the RS422 or RS485 interface must provide termination resistance. The purpose of jumpers J13 and J14 are to enable this line termination resistor (120 R).

Table A-13: Jumper Settings for RS422 RXD Termination (COM2)

Termination	J13
ON	Closed
OFF	Open

Table A-14: Jumper Settings for RS422 TXD and RS485 Termination (COM2)

Termination	J14
ON	Closed
OFF	Open

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Appendix B

VGA1 Module

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B. VGA1 Module

B.1 Overview

The CP303-VGA1 module has been designed to provide the CP303 user with comprehensive access to the multimedia world. The board includes a highly integrated VGA controller from SMI (the Cougar 3DR) with up to 32 MB DDR memory with two high performance graphic engines supporting dual independent graphic displays optimized for MPEG2 and MPEG4 video decoding. The video output configuration is very flexible, allowing a choice of CRT-VGA, DVI, two independent LVDS ports and one TV output.

An additional highlight are the two 1394a-2000 OHCI-compliant 400/100 Mbit/s FireWire™ ports, one for internal connection and one routed via the front panel. The module also includes a very flexible audio interface with several input and output configuration possibilities.

For standalone applications the module provides the mounting for a 2.5" HDD or Flash Disk.

B.2 Technical Specifications

Table B-1: CP303-VGA1 Module Main Specifications

	CP303-	Specifications
Controller	VGA Controller	SMI Cougar 3DR graphics controller with up to 32 MB DDR video memory, supporting dual independent video displays, CRT, DVI, two LVDS ports and a TV port. The controller supports resolutions of up to 1600 x 1200 x 16-bit colors at a 85 Hz refresh rate.
	Firewire Controller	TI TSB43AA22 Integrated 1394a-2000 OHCI PHY/Link Layer controller compliant with IEEE Std 1394-1995, IEEE Std 1394a-2000, and the 1394 Open Host Controller Interface Specification. It is capable of transferring at the 1394 bus up to 400M bits/s.
	Audio Codec	The AD1885 AC'97 Codec includes high-fidelity stereo analog/digital, digital/analog I/O interfaces enabling the connection of several audio sources to the board
External Interfaces	VGA-CRT	15-pin D-SUB connector (only available on the CRT version)
	VGA-DVI	29-pin DVI-I connector with analog and digital video signals (only available on the DVI version)
	VGA-LVDS	Two independent 18-bit LVDS ports on two 8-pin RJ45 connectors
	VGA-TV Out	S-video signal on 4-pin Mini-DIN connector
	FireWire Interface	6-pin FireWire connector, including power distribution
Internal Interfaces	EIDE interface	One EIDE interface supporting Ultra ATA/100/66/33 for 2 hard disks or CD-ROM on 40-pin 2.54 mm or 44-pin 2 mm onboard connector
	Audio Interface	26-pin Audio extension connector with all available analog audio input and output signals. Three ATAPI-style 3-pin audio connectors for CD-ROM, Line and Micro input
	FireWire Interface	6-pin FireWire connector, including power distribution
	Baseboard Interface	I/O extension connector, PCI extension connector, AGP4x extension connector

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Table B-1: CP303-VGA1 Module Main Specifications (Continued)

	CP303-	Specifications
General	Power Consumption	3.3 V at TBD 5.0 V at TBD (without hard disk)
	Temperature Range	Operating temp.: 0°C to +60°C E1 (optional): -25°C to +75°C E2 (optional): -40°C to +85°C Storage temp.: -55°C to +85°C
	Humidity	Climatic humidity: 93% RH at 40 °C, non-condensing
	Dimensions	Dimensions: 100 mm x 160 mm
	Board Weight	CP303 8HP with heat sink: 417 grams (without hard disk)
	Operating System Support	Operating systems supported: Windows 2000, Windows XP etc.

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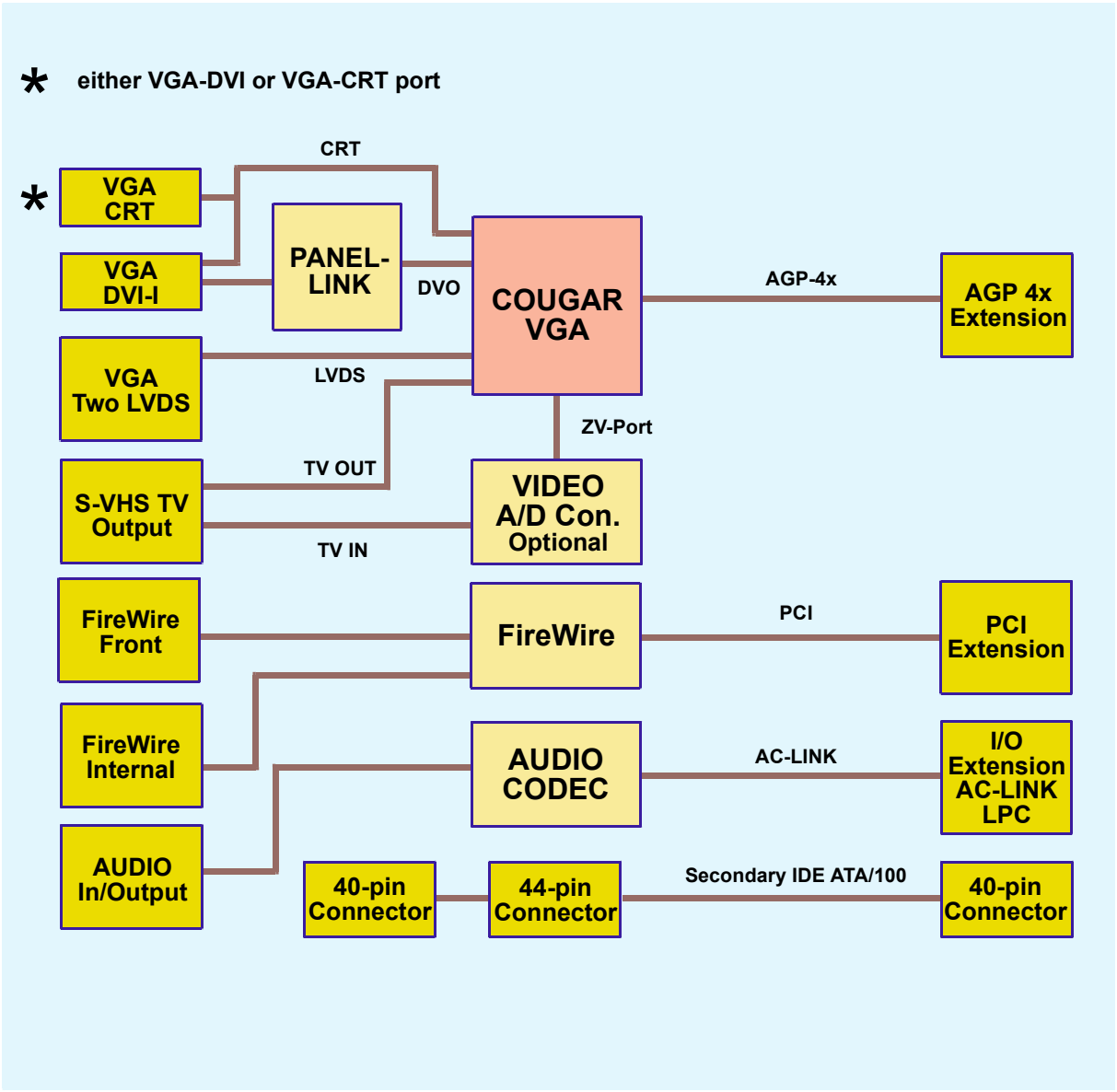
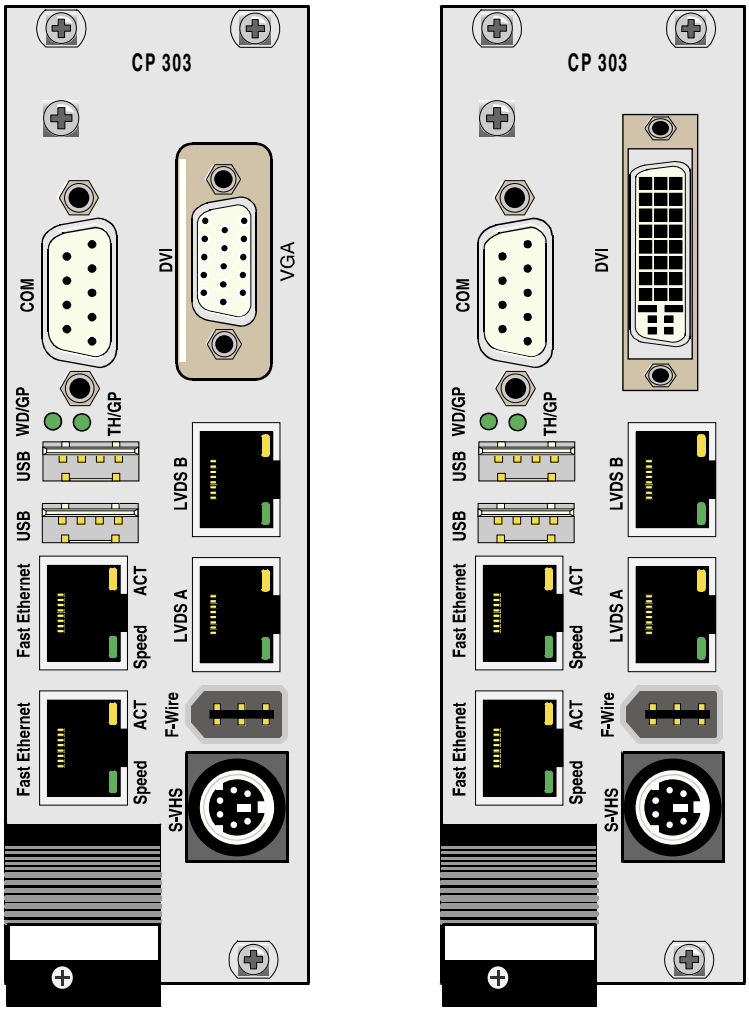
B.3 CP303-VGA1 Module Functional Block Diagram

Figure B-1: CP303-VGA1 Module Functional Block Diagram



B.4 CP303-VGA1 Module Version Front Panels

Figure B-2: CP303-VGA1 Module Version Front Panels



LEGEND:

General Purpose LEDs

- WD/GP (green): Watchdog or General Purpose
- TH/GP (green): Overtemperature Status or General Purpose

Integral Ethernet LEDs

- ACT (yellow): Ethernet Link/Activity
- SPEED (green): Ethernet Speed

Note ...

The LEDs within the LVDS connectors are not utilized on the CP303-VGA1.

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B.5 CP303-VGA1 Module Layout

B.5.1 CP303-VGA1 Module Layout

Figure B-3: CP303-VGA1 Module Layout (Front Side)

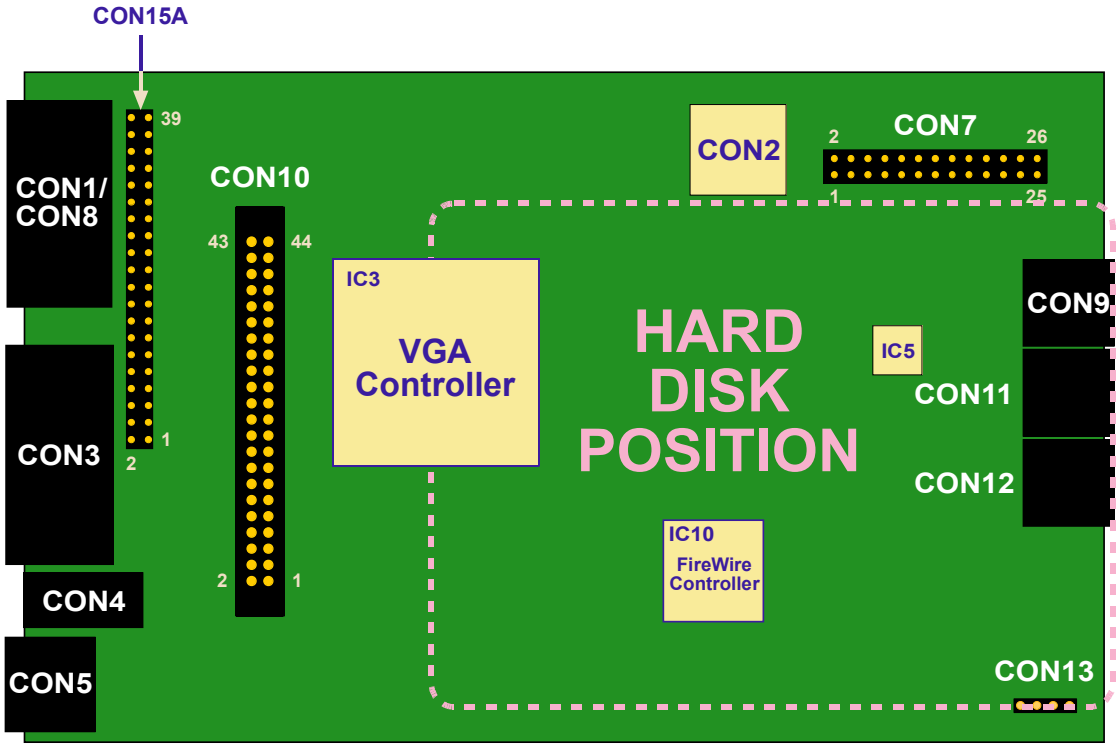
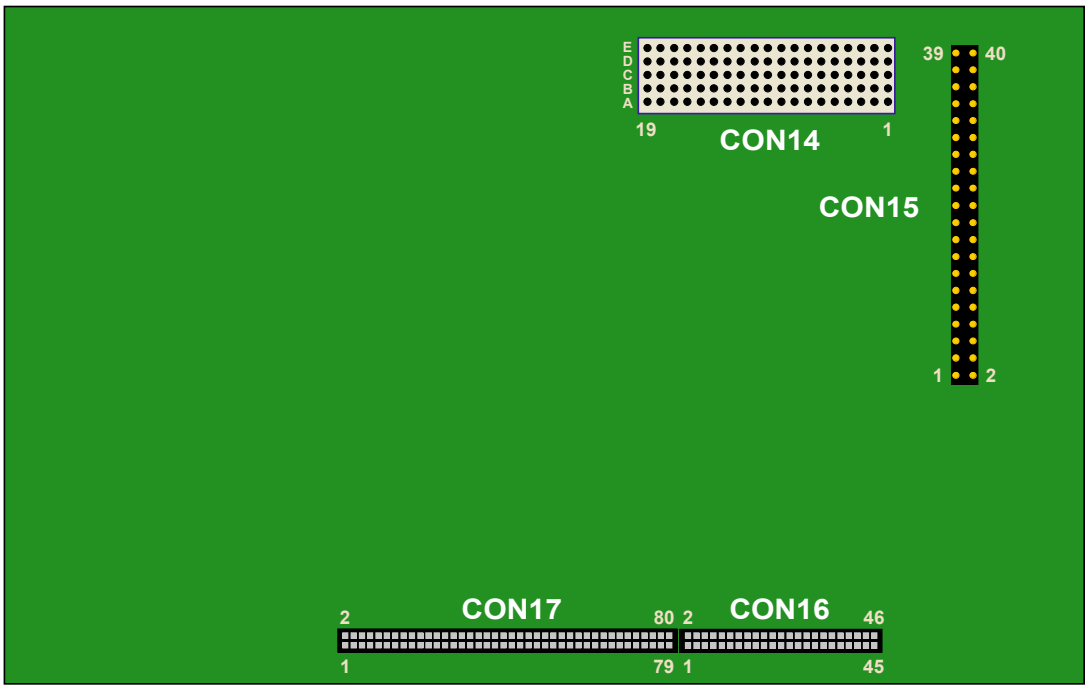


Figure B-4: CP303-VGA1 Module Layout (Reverse Side)



B.6 Module Interfaces (Front Panel and Onboard)

B.6.1 Graphics Controller Interface

The board includes a highly integrated VGA controller from SMI (the Cougar 3DR) with up to 32 MB DDR memory with two high performance graphic engines supporting dual independent graphic displays optimized for MPEG2 and MPEG4 video decoding. The video output configuration is very flexible, allowing a choice of any or all of:- CRT-VGA, DVI, one or two independent LVDS ports and one TV output.

B.6.1.1 Feature Set Cougar 3DR

- Full 2-D and 3-D hardware acceleration
- Integrated H/W Motion Compensation Engines for software MPEG2 and MPEG4 decode
- Internal video memory up to 32 MB DDR memory
- AGP 2X/4X sideband and PCI 2.1 support
- 235 MHz 24-bit RAMDAC supports resolutions up to 1600x1200
- Zoom Video port
- Multi-Display support

B.6.1.2 CRT Interface and Connector CON8

The 15-pin female connector CON8 is used to connect a CRT monitor to the CP303-VGA1 module. The CRT interface is a standard VGA interface for connecting CRT monitors. It is implemented by a 3-row 15-pin D-SUB connector.

Figure B-5: CRT Connector CON8

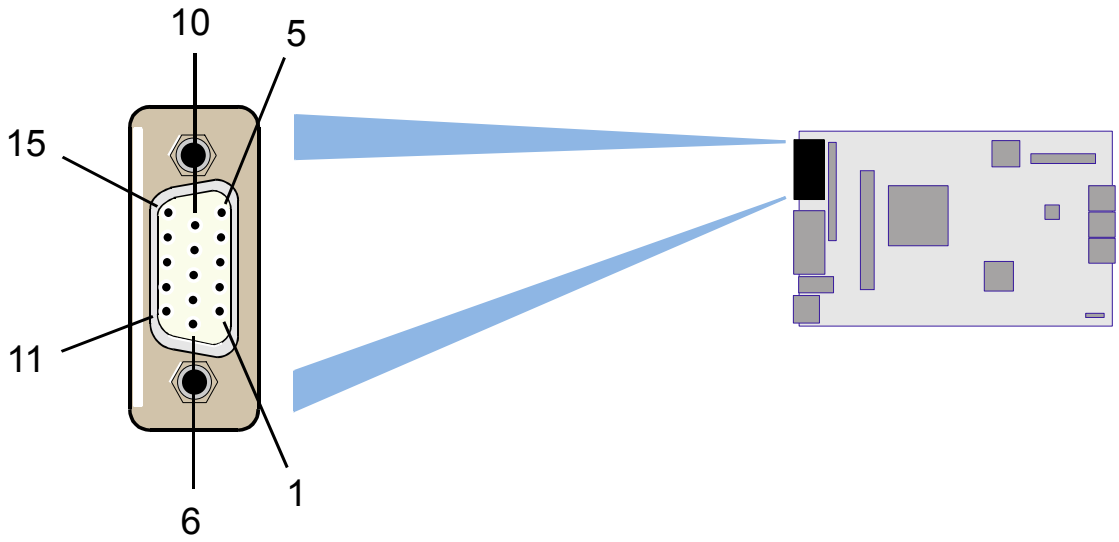


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Table B-2: CRT Connector CON8 Pinout

D-SUB 15	Signal	Function	In/Out
1	Red	Red video signal output	Out
2	Green	Green video signal output	Out
3	Blue	Blue video signal output	Out
13	Hsync	Horizontal sync.	TTL out
14	Vsync	Vertical sync.	TTL out
12	Sdata	I2C™ data	In/Out
15	Sclk	I2C™ clock	Out
9	VCC	Power +5V 200 mA no fuse protection	Out
5,6,7,8,10	GND	Signal ground	--
4,11	Free	--	--

B.6.1.3 DVI-I Interface and Connector CON1

The 29-pin DVI-I female connector CON1 is used to connect an analog or digital monitor to the CP303-VGA1 board

Figure B-6: DVI-I Interface Connector CON1

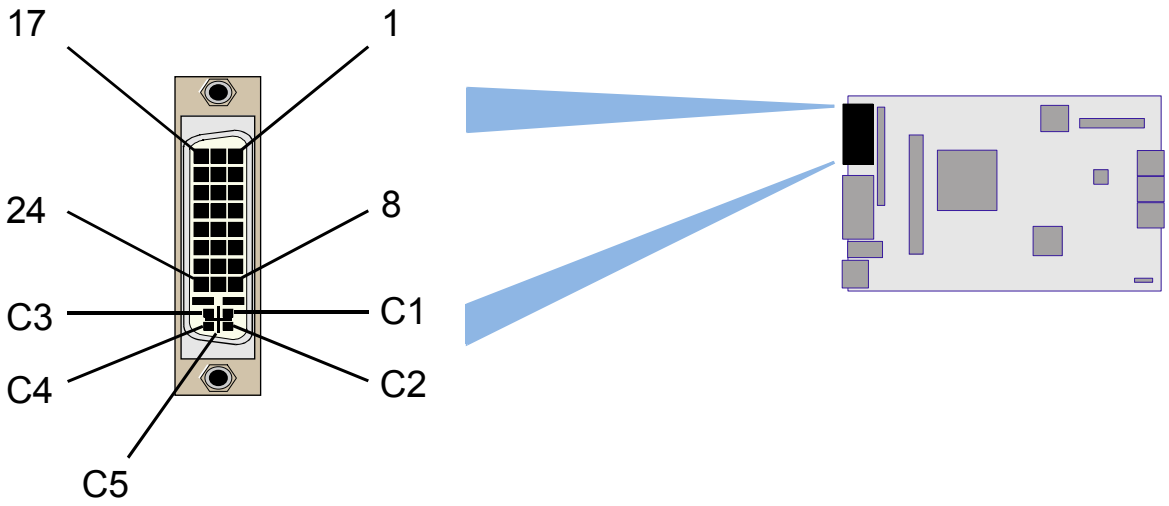

Table B-3: DVI-I Connector CON1 Pinout

Pin Number	Signal	Function	In/Out
1	T.M.D.S Data 2-	T.M.D.S* Link -	Out
2	T.M.D.S Data 2+	T.M.D.S* Link +	Out
3	Data 2/4 Shield	Data 2/4 Shield	--
4	Free		--
5	Free		--
6	DDC Clock	I2C Clock	Out
7	DDC Data	I2C Data	In/Out
8	T.M.D.S Data 1-	T.M.D.S Link -	Out
9	T.M.D.S Data 1+	T.M.D.S Link +	Out
10	Data 1/3 Shield	Data 1/3 Shield	--
11	Free		--
12	Free		--
14	VCC	Power +5 V max. 1.5A	--
15	GND	Signal ground	--
16	Free		--
17	T.M.D.S Data 0-	T.M.D.S Link -	Out
18	T.M.D.S Data 0+	T.M.D.S Link +	Out
19	Data 0/5 Shield	Data 0/5 Shield	--
20	free		--
21	free		--
22	Clock Shield	Clock Shield	--
23	T.M.D.S Clock +	T.M.D.S Link +	Out
24	T.M.D.S Clock -	T.M.D.S Link -	Out
C1	Red	Red video signal output	Out
C2	Green	Green video signal output	Out
C3	Blue	Blue video signal output	Out
C4	Hsync	Horizontal sync. TTL out	Out
C5	Vsync	Vertical sync. TTL out	Out

* T.M.D.S. = Transition minimized differential signaling

Note ...

The CP303-VGA1 is delivered configured either with the VGA-CRT or VGA-DVI interface and cannot subsequently be reconfigured.

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B.6.1.4 LVDS Interface and Connector CON3

To enable the connection of either one or two independent LVDS TFT displays, the CP303-VGA1 is equipped with two 6-bit per color FPD-Link LVDS transmitters.

Warning!

Do not disconnect or connect the LVDS panel with system power applied.

Connecting or disconnecting of the LVDS panel with power applied to the system will result in damage to the CP303 board.

Figure B-7: LVDS Connector CON3

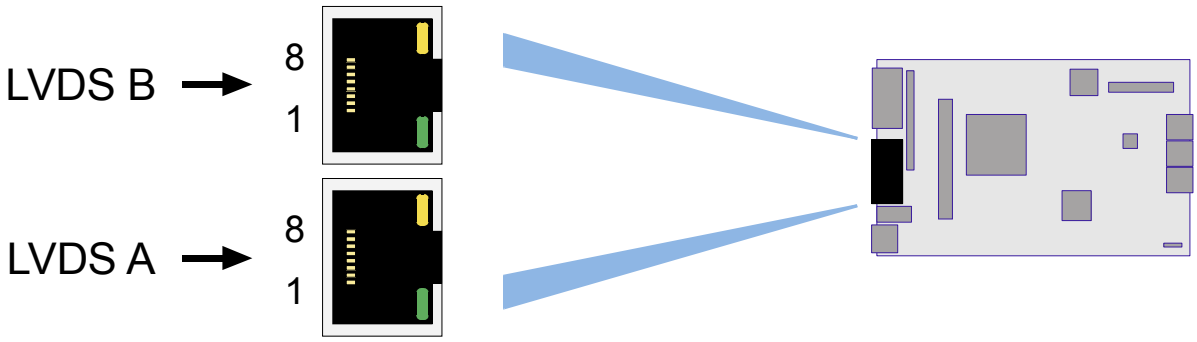

Table B-4: LVDS Connector CON3 Pinout

Pin Number	Signal	Function	In/Out
1	TXOUT0-	LVDS signal	Out
2	TXOUT0+	LVDS signal	Out
3	TXOUT1-	LVDS signal	Out
4	TXOUT1+	LVDS signal	Out
5	TXOUT2-	LVDS signal	Out
6	TXOUT2+	LVDS signal	Out
7	TXCLK_OUT-	LVDS clock signal	Out
8	TXCLK_OUT+	LVDS clock signal	Out

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B.6.2 S-Video Output Interface and Connector CON5

The VGA1 provides one TV S-Video output on a 4 pin MINI-DIN connector.

Figure B-8: S-Video Connector CON5

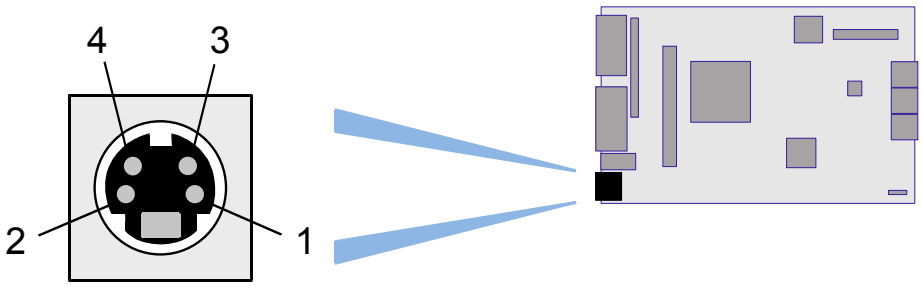

Table B-5: S-Video Connector CON5 Pinout

Pin Number	Signal	Function	In/Out
1	GND		
2	GND	Signal ground	
3	Y	Luminance output	Out
4	C	Chrominance output	Out

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B.6.3 FireWire Controller

The CP303-VGA1 uses the TSB43AA22 iOHCI-Lynx (integrated Link Layer Controller and Physical Transceiver) host adapter, which is compatible with OHCI based software. The chip provides two independent FireWire ports, both of which are hot pluggable so that there is no need to restart the system to enable 1394 functionality.

One 6-pin connector is on the front panel and the other onboard 6-pin connector is for the connection of internal devices.

Feature Set TSB43AA22

- PCI 32-bit 33 MHz master interface
- 4 kB configurable FIFO
- Open Host Controller Interface 1.0 (OHCI)
- Supports data transfer rates of 400,200 or100 Mbps

B.6.3.1 FireWire Connectors CON2 and CON4

Figure B-9: FireWire Connectors CON2 and CON4 (Front View)

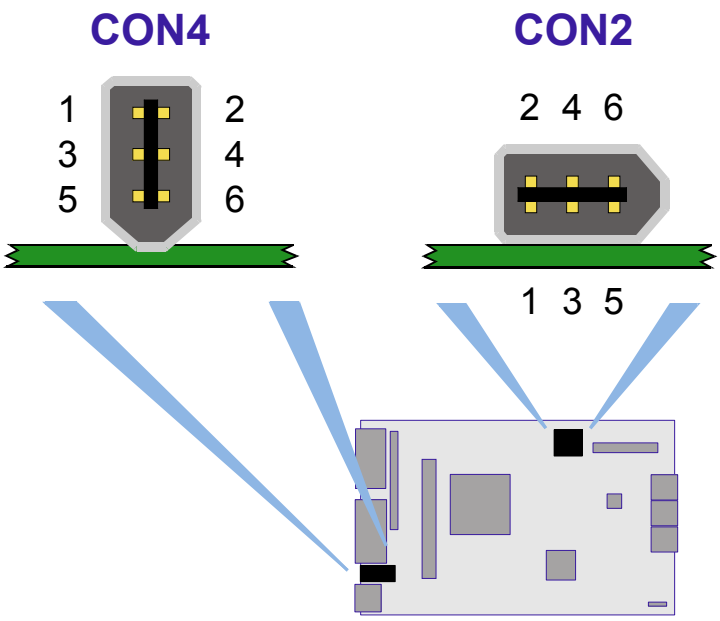

Table B-6: FireWire Connectors CON2 and CON4 Pinout

Pin Number	Signal	Function	In/Out
1	Power	Power input and Output	IN/OUT
2	GND	Signal ground	
3	TPB-	Twisted-pair cable B differential signal terminals	IN/OUT
4	TPB+	Twisted-pair cable B differential signal terminals	IN/OUT
5	TPA-	Twisted-pair cable A differential signal terminals	IN/OUT
6	TPA+	Twisted-pair cable A differential signal terminals	IN/OUT
7	Shield	Shield	
8	Shield	Shield	

Note...

Use only shielded (each pair individually shielded), twisted pair cables. The maximum length of cable that may be used for CON2 and CON4 is 10 metres.

The FireWire power line is protected with a fuse (1.5 A).

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B.6.4 Audio Interface

The audio interface of the CP303-VGA1 is realized using the latest AC '97 compliant codec from Analog Devices, the AD1885. All signals used on the AD1885 codec are routed to an on-board audio connector and three 4-pin ATAPI-style connectors.

Feature Set AD1885 Audio Codec

The AD1885 is a fully AC '97 compliant codec. The codec's features include:

- 90 dB signal-to-noise ratio sound quality
- Playback sample rates up to 48 kHz
- 16 bit stereo full-duplex codec
- Full-duplex operation at asynchronous hardware record/playback samples rates
- Frequency response: 20 Hz to 20 kHz (± 0.1 dB)

B.6.4.1 Audio Interface Signal Implementation

The audio interface signals are implemented on the CP303-VGA1 as follows:

Table B-7: Audio Interface Signal Implementation

Interface on AD1885	Usage on CP303-VGA1
CD-ROM input L/R	Connected to: 4-pin connector and 26-pin Audio extension connector
Line in L/R	Connected to: 4-pin connector and 26-pin Audio extension connector
Aux in L/R	Not used
Video in L/R	Connected to: 26-pin Audio connector
Micro in L/R	Connected to: 4-pin connector and 26-pin Audio extension connector
Line out L/R	Connected to: 26-pin Audio extension connector
Head out L/R	Connected to: 26-pin Audio extension connector
Mono out	Connected to: 26-pin Audio extension connector

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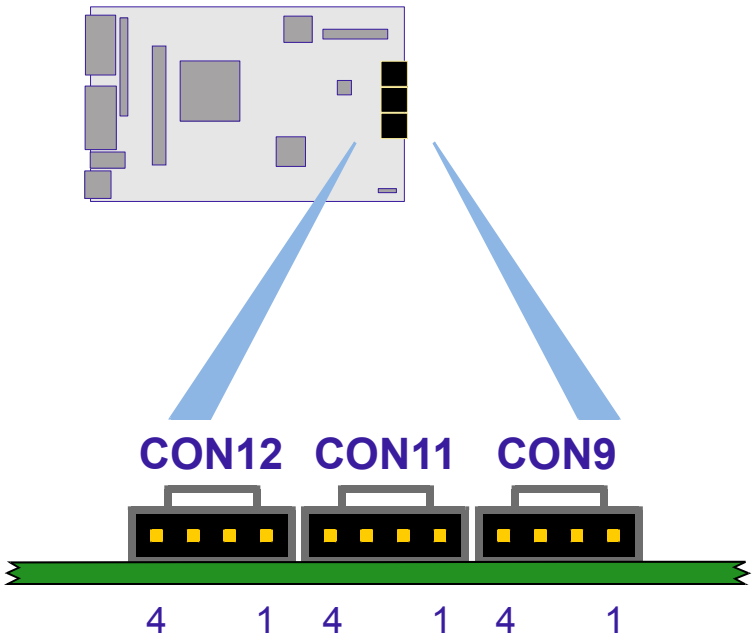
B.6.4.2 Audio Connectors CON9, CON11, CON12

Figure B-10:Audio Connectors CON9, CON11, CON12



The board is equipped with three ATAPI-style 4-pin audio connectors for CD-ROM, line and micro input.

Table B-8: CD-ROM Input Connector CON11

Pin Number	Signal	Function	In/Out
1	CD left	CD Audio left channel	In
2	Audio Gnd	Audio analog ground reference	--
3	Audio Gnd	Audio analog ground reference	--
4	CD right	CD Audio right channel	In

Table B-9: LINE Input Connector CON9

Pin Number	Signal	Function	In/Out
1	Line left	Line Audio left channel	In
2	Audio Gnd	Audio analog ground reference	--
3	Audio Gnd	Audio analog ground reference	--
4	Line right	Line Audio right channel	In

Table B-10:Micro Input Connector CON12

Pin Number	Signal	Function	In/Out
1	Micro In1	Micro input channel 1	In
2	Audio Gnd	Audio analog ground reference	--
3	Audio Gnd	Audio analog ground reference	--
4	Micro In2	Micro input channel 1	In

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B.6.4.3 Audio Extension Connector CON7

The 26-pin Audio extension connector carries all analog audio input and output signals to and from the Audio controller.

Figure B-11:Audio Extension Connector CON7

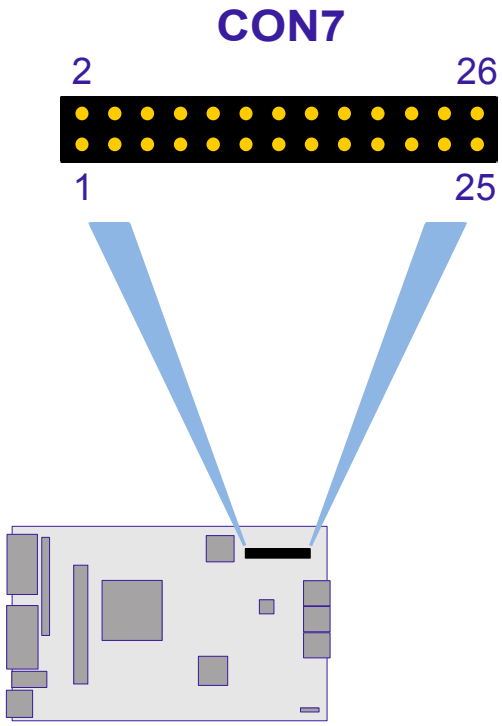

Table B-11:Audio Extension Connector CON7

Pin Number	Signal	Function	In/Out
1	Line left out	Line Audio left output channel	Out
3	Line right out	Line Audio right output channel	Out
5	Head left out	Head Audio left output channel	Out
7	Head right out	Head Audio right output channel	Out
9	Mono out	Mono output channel	Out
11	Micro In2	Micro input channel 2	In
13	CD left	CD Audio left channel	In
15	Audio GND	Audio analog ground reference	--
17	CD right	CD Audio right channel	In
19	Line left	Line Audio left channel	In
21	Line right	Line Audio right channel	In
23	Video left	Video Audio left channel	In
25	Video right	Video Audio right channel	In
Even 2-26	GND	Signal ground	--

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B.6.5 EIDE Interface (Secondary Port)

The EIDE interface on the CP303-VGA1 module comprises three connectors, CON10, CON15 and CON15A. The CON15 connector, situated on the reverse of the board, is used to connect the CP303-VGA1 module to the baseboard, while the other two connectors, CON10 and CON15A, are used to connect devices to the CP303-VGA1 module.

CON10 is a 44-pin 2mm pinrow connector while CON15A is a standard 40-pin 2.54mm pinrow connector. Up to two devices (which must be master/slave pairs) may be attached to the CP303-VGA1 board; either both devices on CON10 or on CON15A or one device on each connector. The maximum length of cable that may be used for CON15A is 25 cm.

Note ...

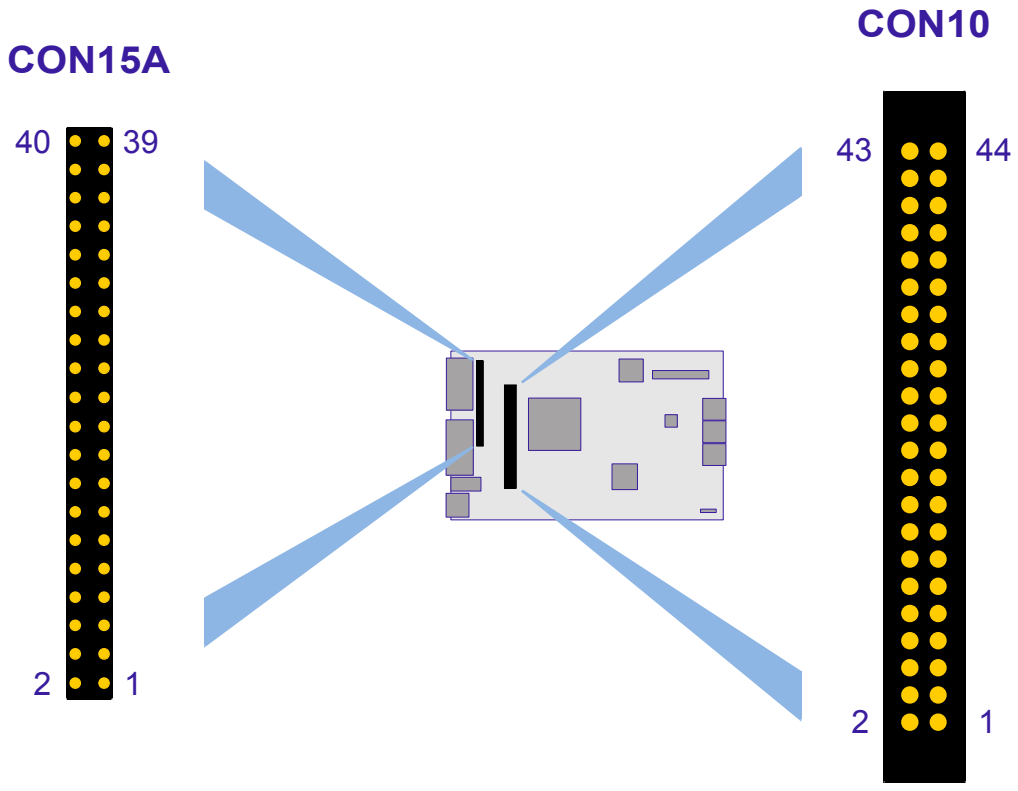
ATA-66 and ATA-100 are faster timings and require a specialized cable which has additional grounding wires to reduce reflections, noise and inductive coupling. This cable will also support all legacy IDE drives.

The onboard 2.5" hard disk or Flash disk (CON10) must be configured as a MASTER device. Due to the ATA-100 cable specification the board does not support a 2.5" slave device and a master device on CON15A.

The blue end of the ATA-100 cable must connect to the motherboard, the gray connector to the UltraDMA /100 slave device and the black connector to the UltraDMA/100 master device.

The CompactFlash (CON9) on the CP303 baseboard is rendered useless by the addition of the VGA1 module, however, its functionality is replaced by the EIDE port for the 2.5” hard disk.

Figure B-12:Frontside EIDE Connectors CON10 and CON15A



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B.6.5.1 Onboard EIDE Connector CON10 Pinout

A 2.5” hard disk or Flash disk may be mounted directly onto the CP303-VGA1 module using the 44-pin connector CON10.

Table B-12:Pinout of the AT 44-pin Connector

Pin Number	Signal	Function	In/Out
1	IDERESET	Reset HD	Out
2	GND	Ground signal	--
3	HD7	HD data 7	In/Out
4	HD8	HD data 8	In/Out
5	HD6	HD data 6	In/Out
6	HD9	HD data 9	In/Out
7	HD5	HD data 5	In/Out
8	HD10	HD data 10	In/Out
9	HD4	HD data 4	In/Out
10	HD11	HD data 11	In/Out
11	HD3	HD data 3	In/Out
12	HD12	HD data 12	In/Out
13	HD2	HD data 2	In/Out
14	HD13	HD data 13	In/Out
15	HD1	HD data 1	In/Out
16	HD14	HD data 14	In/Out
17	HD0	HD data 0	In/Out
18	HD15	HD data 15	In/Out
19	GND	Ground signal	--
20	N/C	--	--
21	IDEDRQ	DMA request	In
22	GND	Ground signal	--
23	IOW	I/O write	Out
24	GND	Ground signal	--
25	IOR	I/O read	Out
26	GND	Ground signal	--
27	IOCHRDY	I/O channel ready	In
28	GND	Ground signal	--
29	IDEDACKA	DMA Ack	Out
30	GND	Ground signal	--
31	IDEIRQ	Interrupt request	In
32	N/C	--	--
33	A1	Address 1	Out
34	ATA66	Detect ATA66	In
35	A0	Address 0	Out
36	A2	Address 2	Out
37	HCS0	HD select 0	Out
38	HCS1	HD select 1	Out
39	LED	LED driving	In
40	GND	Ground signal	--
41	VCC	5V power	--
42	VCC	5V power	--
43	GND	Ground signal	--
44	N/C	--	--

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B.6.5.2 EIDE Connectors CON15 and CON15A Pinouts

A wide range of EIDE devices may be connected to the CP303-VGA1 module at CON15A using a ribbon cable.

The following table describes the pinouts of connectors CON15 and CON15A, which are identical, with the corresponding signal names.

Table B-13:Pinouts of EIDE Connectors CON15 and CON15A

Pin Number	Signal	Function	In/Out
1	IDERESET	Reset HD	Out
2	GND	Ground signal	--
3	HD7	HD data 7	In/Out
4	HD8	HD data 8	In/Out
5	HD6	HD data 6	In/Out
6	HD9	HD data 9	In/Out
7	HD5	HD data 5	In/Out
8	HD10	HD data 10	In/Out
9	HD4	HD data 4	In/Out
10	HD11	HD data 11	In/Out
11	HD3	HD data 3	In/Out
12	HD12	HD data 12	In/Out
13	HD2	HD data 2	In/Out
14	HD13	HD data 13	In/Out
15	HD1	HD data 1	In/Out
16	HD14	HD data 14	In/Out
17	HD0	HD data 0	In/Out
18	HD15	HD data 15	In/Out
19	GND	Ground signal	--
20	N/C	--	--
21	IDEDRQ	DMA request	In
22	GND	Ground signal	--
23	IOW	I/O write	Out
24	GND	Ground signal	--
25	IOR	I/O read	Out
26	GND	Ground signal	--
27	IOCHRDY	I/O channel ready	In
28	GND	Ground signal	--
29	IDEDACKA	DMA Ack	Out
30	GND	Ground signal	--
31	IDEIRQ	Interrupt request	In
32	N/C	--	--
33	A1	Address 1	Out
34	ATA66	Detect ATA66	In
35	A0	Address 0	Out
36	A2	Address 2	Out
37	HCS0	HD select 0	Out
38	HCS1	HD select 1	Out
39	LED	LED driving	In
40	GND	Ground signal	--

B.6.6 Extension Connectors CON14, CON16 and CON17

The I/O extension connectors provide the connections for the AGP4x, PCI and the audio interface.

Appendix C

CP-RIO3-02 Rear IO Module

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C. CP-RIO3-02 Rear IO Module

C.1 Overview

The CP303 provides optional Rear I/O connectivity for peripherals, a feature which may be particularly useful in specialized CompactPCI systems. Some standard PC interfaces are implemented and assigned to the front panel and to the rear connector J2.

When the Rear I/O module is used, the signals of some of the main board/front panel connectors are routed to the module interface. Thus the Rear I/O module makes it much easier to remove the CPU in the rack as there is practically no cabling on the CPU board.

For the system Rear I/O feature a special backplane is necessary. The CPU board with Rear I/O is compatible with all standard CompactPCI passive backplanes with Rear I/O support on the system slot.

The CP-RIO3-02 Rear I/O provides the following interfaces, all signals are available via connector P2.

32-bit CompactPCI and Rear I/O

- 32-bit/33 MHz CompactPCI
- Two USB ports
- Two Ethernet ports without LED
- Two COM ports
- VGA CRT interface
- Fan control input

The following ports may be used either for rear or front I/O, the combination of both rear and front is not possible.

- The two Ethernet ports without LEDs
- Two COM ports
- VGA CRT interface

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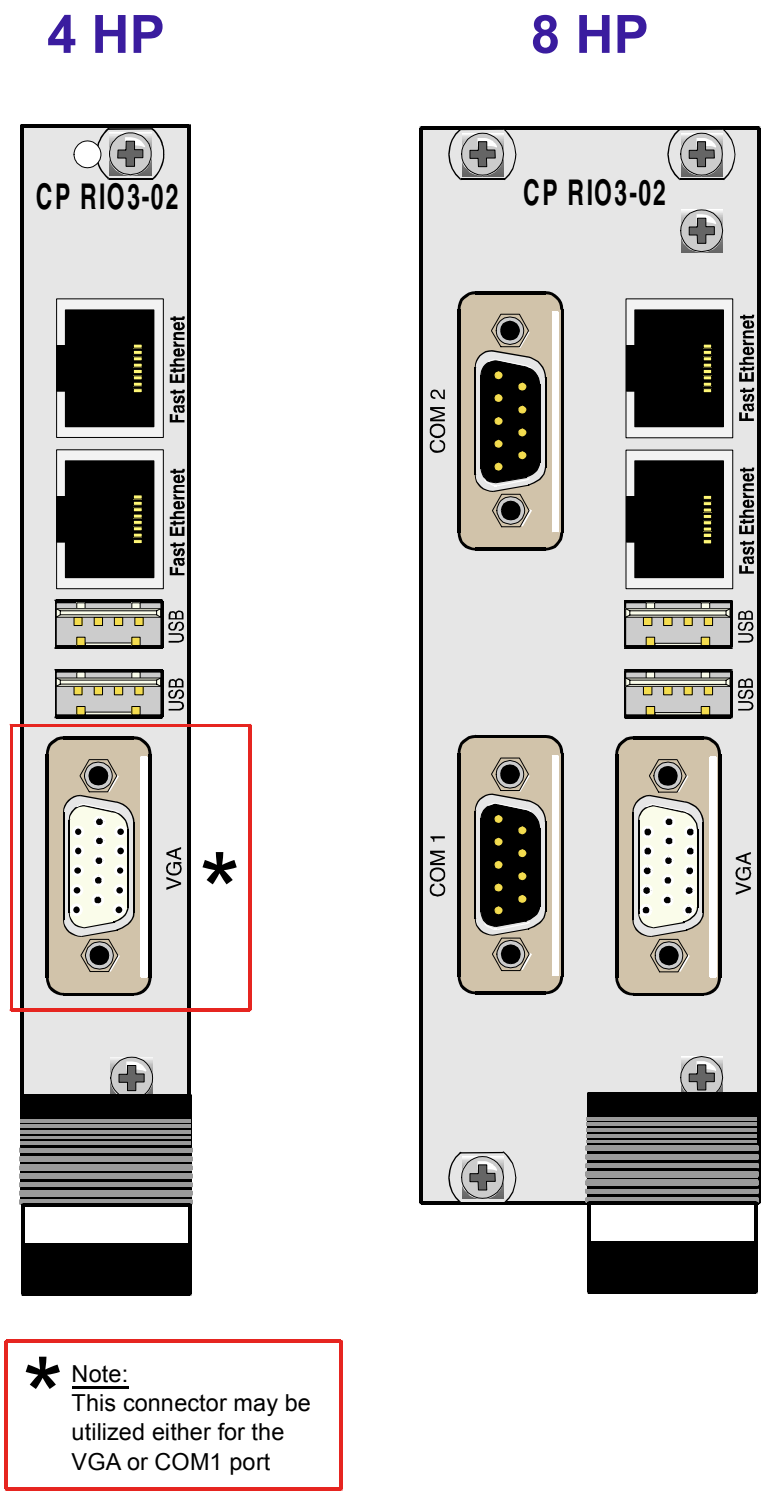
C.2 Front Panels

Note that the four Ethernet LEDs are not active on the CP-RIO3-02.

Figure C-1: CP-RIO3-02 Front Panels, 4HP and 8HP Versions



* Note:
This connector may be utilized either for the VGA or COM1 port

C.3 Module Layout: 4HP and 8HP Versions

Figure C-2: CP-RIO3-02 Module Layout, 4HP Version

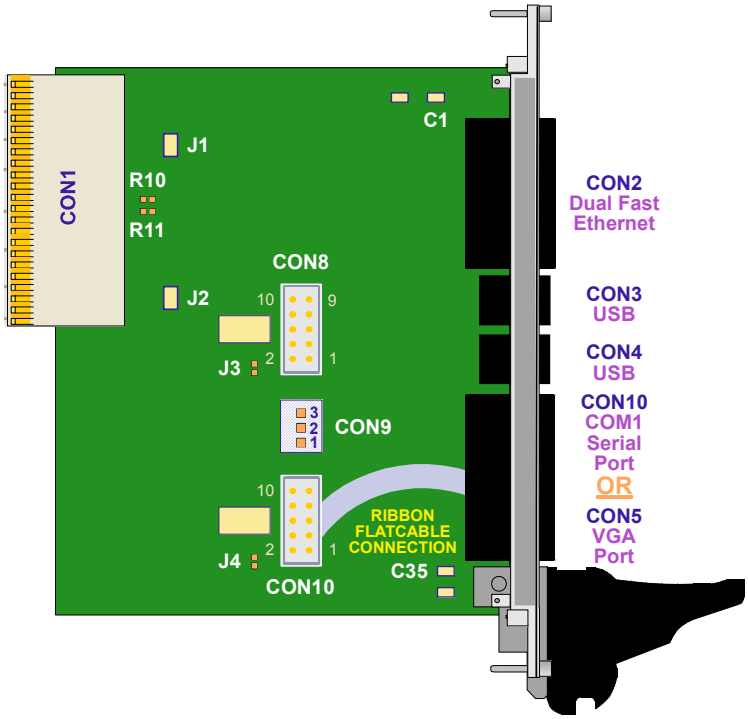
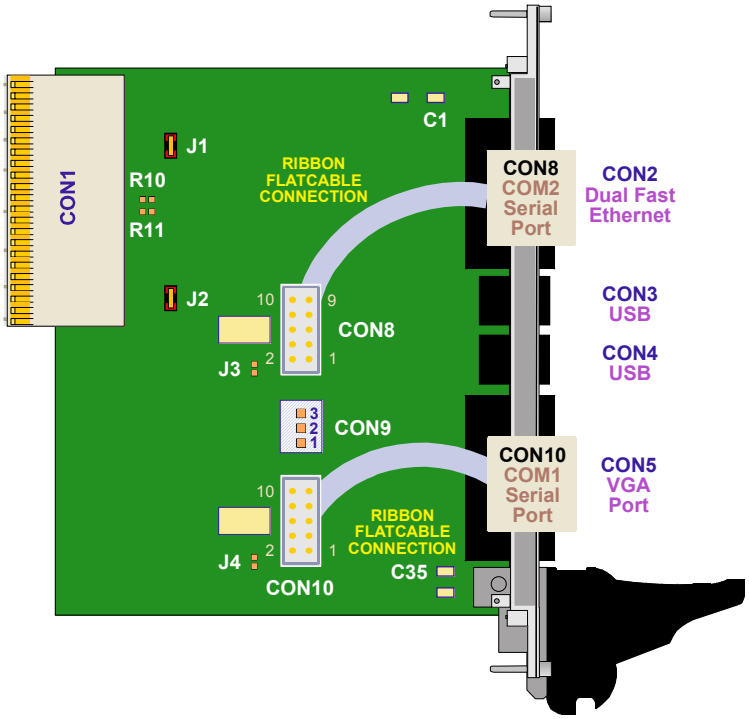


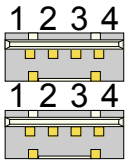
Figure C-3: CP-RIO3-02 Module Layout, 8HP Version



C.4 Module Interfaces

C.4.1 USB Interfaces

Figure C-4: USB Connectors CON3 and CON4



There are two identical USB interfaces on the CP-RIO3-02 module (8HP version) each with a maximum transfer rate of 12 Mbit provided for connecting USB devices. One USB peripheral may be connected to each port. To connect more than two USB devices an external hub is required.

C.4.1.1 USB Connectors CON3 and CON4 Pinout

Table C-1: USB Connectors CON3 and CON4 Pinout

Pin Number	Signal	Function	In/Out
1	VCC	VCC signal	--
2	UV0-	Differential USB-	--
3	UV0+	Differential USB+	--
4	GND	GND signal	--
5	VCC	VCC signal	--
6	UV0-	Differential USB-	--
7	UV0+	Differential USB+	--
8	GND	GND signal	--

Note ...

The USB power supply feeding the two ports is protected by a 500 mA fuse. All signal lines are EMI-filtered.

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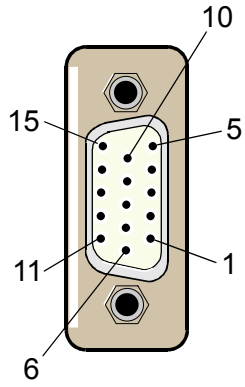
C.4.2 VGA Interface

Figure C-5: D-sub VGA Connector CON5



C.4.2.1 VGA Connector CON5 Pinout

The 15-pin female connector CON5 is used to connect a VGA monitor to the CP-RIO3-02 board.

Table C-2: VGA Connector CON5 Pinout

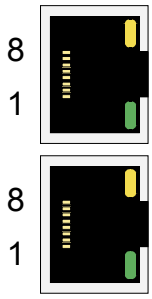
Pin Number	Signal	Function	In/Out
1	Red	Red video signal output	Out
2	Green	Green video signal output	Out
3	Blue	Blue video signal output	Out
13	Hsync	Horizontal sync.	TTL out
14	Vsync	Vertical sync.	TTL out
12	Sdata	Not supported	In/Out
15	Sclk	Not supported	Out
9	VCC	Power +5V 200 mA no fuse protection	Out
5,6,7,8,10	GND	Signal ground	--
4,11	Free	--	--

Note ...

The 75 Ohm termination resistors for the three VGA signals (red, green, blue) are located on the baseboard.

C.4.3 Fast Ethernet Interfaces

Figure C-6: Dual Ethernet/Fast Ethernet Connector CON2



The Ethernet connector are realized as RJ45 twisted-pair connectors. The interfaces provide automatic detection and switching between 10Base-T and 100Base-TX data transmission.

C.4.3.1 RJ45 Connector CON2 Pinout

CON2 supplies the 10Base-TX/100Base-TX interface to the Ethernet controller.

Table C-3: RJ45 Connector CON2 Pinout

Pin Number	Signal	Function	In/Out
1	TX+	Transmit +	Out
2	TX-	Transmit -	Out
3	RX+	Receive +	In
4	NC	--	--
5	NC	--	--
6	RX-	Receive -	In
7	NC	--	--
8	NC	--	--

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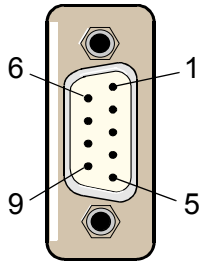
C.4.4 Serial Port Interfaces

Figure C-7:PC-compatible D-sub Serial Interface



C.4.4.1 Serial Port Connectors CON8 and CON10 Pinouts

The serial port male connectors CON8 and CON10 allow the connection of RS232 devices to the CP-RIO3-02 board.

Table C-4: Serial Port Connectors CON8 and CON10 Pinouts

Pin Number	Signal	Function	In/Out
1	DCD	Data carrier detect	In
2	RXD	Receive data	In
3	TXD	Transmit data	Out
4	DTR	Data terminal ready	Out
5	GND	Signal ground	--
6	DSR	Data send request	In
7	RTS	Request to send	Out
8	CTS	Clear to send	In
9	RI	Ring indicator	In

Note ...

To ensure the proper functioning of the Rear I/O serial interfaces, the drivers for COM1 and COM2 on the CP303 module must be disabled.

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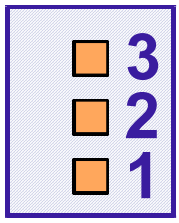
C.4.5 Fan Control Interface (optional)

A fan for CPU cooling can be connected via the power connector CON9.

Figure C-8: Fan Control Interface Connector CON9



C.4.5.1 Fan Control Connector CON9 Pinout

Table C-5: Fan Control Connector CON9 Pinout

Pin Number	Signal	Function	In/Out
1	GND	Ground	--
2	VCC	5V Fan Supply Voltage at a maximum current of 300 mA	Out
3	FAN	Fansense	In

C.4.5.2 External LED

An external LED can be plugged to this jumper.

Table C-6: J2 External LED

Pin Number	Signal	Function	In/Out
1	LED	LED Control	Out max. 4mA
2	VCC	Power	Out max. 10mA

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C.4.6 Rear I/O interface on Compact PCI Connector CON1

The CP-RIO3-02 conducts a wide range of I/O signals through the Rear I/O connector J2.

Note ...

If the Rear I/O feature is selected the PCI interface is only 32-bit. For the 3U Rear I/O a special backplane is necessary.

Table C-7: Rear I/O CompactPCI Bus Connector J2 (CON2) Pinout

Pin	Z	A	B	C	D	E	F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	CLK6	GND	TDN1	RDN1	RDP1	GND
20	GND	CLK5	GND	TDP1	GND	VCC	GND
19	GND	GND	GND	RES	RES	+3.3V	GND
18	GND	RDN2	UV0-	UV3+	RTC Bat	+3.3V	GND
17	GND	RDP2	ROUT (GND)	PRST	REQ6	GNT6	GND
16	GND	TDN2	UV0+	DEG	GND	UV3-	GND
15	GND	TDP2	GOUT (GND)	FAL	REQ5	GNT5	GND
14	GND	2RIN	2DSR	2RTS	VSYNC (GND)	2CTS	GND
13	GND	2RXD	FANSENSE (GND)	BOUT (VIO)	2DTR	2DCD	GND
12	GND	1DSR	1RTS	1CTS	HSYNC (GND)	2TXD	GND
11	GND	1DTR	BOUT (GND)	--	1DCD	1RIN	GND
10	GND	--	--	1TXD	GND	1RXD	GND
9	GND	--	--	--	--	--	GND
8	GND	--	--	--	GND	--	GND
7	GND	--	--	--	--	--	GND
6	GND	--	--	--	GND	--	GND
5	GND	--	GND	--	--	GPLED	GND
4	GND	VIO	VCC	--	GND	--	GND
3	GND	CLK4	GND	GNT3	REQ4	GNT4	GND
2	GND	CLK2	CLK3	SSYSEN	GNT2	REQ3	GND
1	GND	CLK1	GND	REQ1	GNT1	REQ2	GND

Legend for table on preceding page

Ethernet1

TDP1/TDN1	Transmit Differential Pair.
RDP1/RDN1	Receive Differential Pair.

Ethernet2

TDP2/TDN2	Transmit Differential Pair.
RDP2/RDN2	Receive Differential Pair.

USB ports

USB1+/-	USB data differential data signals
USB3+/-	USB data differential data signals

Serial Port 1

S1*	Serial port signals; TTL level

Serial Port 2

S2*	Serial port signals; TTL level

CONTROL Signals

FANSENSE	Schmitt Trigger fan tachometer inputs; TTL level

VGA CRT signals

ROUT	Red signal
GOUT	Green signal
BOUT*	Blue signal
HSYNC	Horizontal Sync.
VSYNC	Vertical Sync.

* Note that this signal (BOUT) appears twice in the rear I/O compactPCI bus connector J2 pinout in order to provide compatibility with the CP302. Pin number B11 refers to the CP303 and C13 refers to the CP302. The default configuration is CP303 (B11).

Reserved Signals

RES	Reserved (leave open)

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C.5 Jumper Setting

C.5.1 External Reset

An external reset button can be enabled via this jumper.

C.5.1.1 External Reset

Table C-8: Jumper J1 External Reset

J1	Function
Open	*Normal operation*
Closed	System reset

The default setting is indicated by italics.

C.5.2 COM Port Configuration

The two COM ports are configured using solder jumpers J3 and J4

C.5.2.1 COM1 Configuration

Table C-9: COM1 Configuration using Jumper J4

J4	Function
Open	*RS232 enabled*
Closed	RS232 disabled

The default setting is indicated by italics.

C.5.2.2 COM2 Configuration

Table C-10:COM2 Configuration using Jumper J3

J3	Function
Open	*RS232 enabled*
Closed	RS232 disabled

The default setting is indicated by italics.

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C.5.3 Shorting Chassis GND (Shield) to Logic GND

The front panel and front panel connectors are isolated to the logic ground.

To enable the connection between the chassis GND and logic GND the capacitors must be exchanged with zero ohm resistors.

Table C-11:Shorting Chassis GND (Shield) to Logic GND

CAPACITOR	SETTING	DESCRIPTION
C1, C35	*Closed 470pF 2KV capacitors*	*Connectors are isolated to logic GND with three 470pF 2KV capacitors*
	Closed zero ohm resistors	Connectors are connected to logic GND and chassis GND

The default setting is indicated by italics.

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Appendix D

CP303-V

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D. CP303-V

D.1 Board Introduction

The CP303-V is designed around the Intel® Celeron® Processor family and the Intel® i815-B0 Chipset. The CPU speeds start at 400 MHz and are available up to 1000 MHz.

The CP303-V offers more features and expandability than other CompactPCI boards in its class. The board comes with an onboard Ultra ATA/100 interface, one 10BASE-T/100BASE-TX Fast Ethernet port integrated in the chipset (82559 type), one CompactFlash type II socket and a built-in Intel® 3D Graphics accelerator for enhanced graphics performance. Several onboard connectors provide flexible 8HP expandability.

To achieve high system performance the board includes one SODIMM socket for flexible memory upgrading up to 512 MB. The board supports one 64-bit/33 MHz CompactPCI interface.

The optional CP303-IDE1 module has been designed to make available all the legacy PC I/O ports. It includes two COM ports, a PS/2 keyboard and mouse port, a parallel port, floppy and a 2.5” onboard hard disk interface.

The following sections describe the main features of the CP303-V. For further information concerning functional description, installation, configuration and BIOS of the CP303-V please refer to chapters 2, 3, 4 and 5 in this manual.

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D.2 Board-Specific Information

The CP303-V is a CompactPCI Celeron® Processor based single-board computer specifically designed for use in highly integrated platforms with solid mechanical interfacing for a wide range of industrial environment applications.

Some of the CP303-V's outstanding features are:

- Intel® Celeron® Processor up to 1000 MHz
- 256 kB L2 cache on-die, running at CPU speed
- up to 133 MHz processor system bus
- 815-B0 and ICH2 chipset
- Up to 512 MB SDRAM memory
- Integrated 3D high performance VGA controller
- Analog display support up to 1600 x 1200 x 8-bit
- One Fast Ethernet interface
- One EIDE Ultra ATA/100 interface
- Onboard CompactFlash type II socket
- Four USB 1.1 ports
- One PCI-to-PCI bridge 32-bit to 64-bit at 33 MHz
- Compatible with CompactPCI spec. Rev. 3.0
- 1 MB onboard flash (1 MB for BIOS)
- Integrated Hardware Monitor
- Watchdog timer
- Two COM ports (four on 8HP version)
- I/O extension connector (LPC, AC97 Link)
- Several rear I/O configurations
- Jumperless board configuration
- Standard temperature range 0°C to + 60°C
- Passive heat sink solution

D.3 Optional Modules

D.3.1 CP303-IDE1 Module

The CP303-IDE1 module has been designed to make available all legacy PC I/O ports. It includes two COM ports, a PS/2 keyboard and mouse port, a parallel port plus floppy and hard disk interfaces. This additional capability opens up the broadest range of expansion possibilities.

For standalone applications the module provides the mounting for a 2.5” hard disk drive or FLASH disk.

See Appendix A for more details.

D.3.2 CP-RIO3-02 Rear I/O Module

Designed for use with a 32-bit rear I/O variant of the CP303-V and a backplane with system slot rear I/O capability, this module provides rear I/O interfacing for the two standard RS232 serial interfaces and the Fast Ethernet interface.

See Appendix C for more details.

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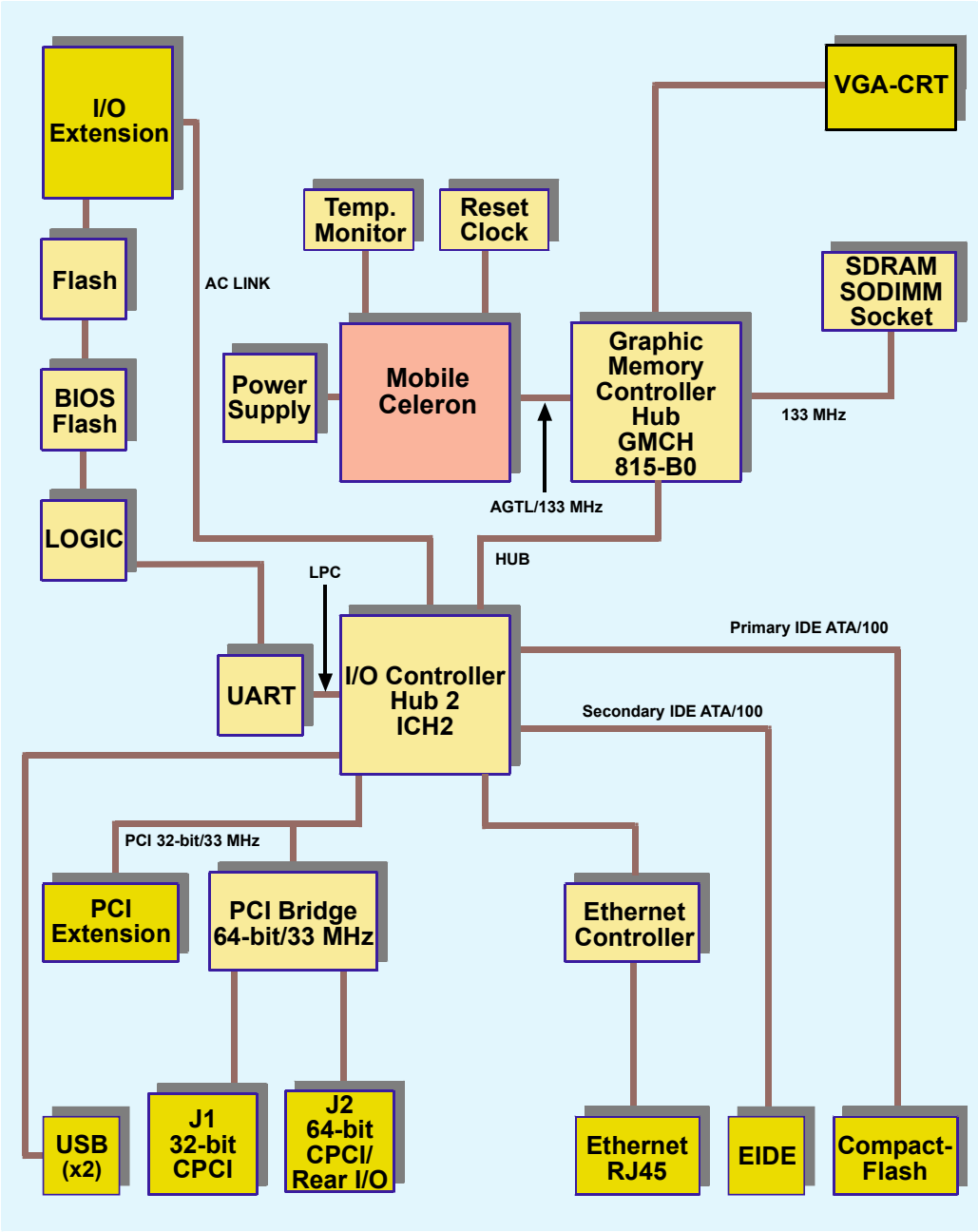
D.4 Board Diagram

The following diagram provides additional information concerning board functionality and component layout.

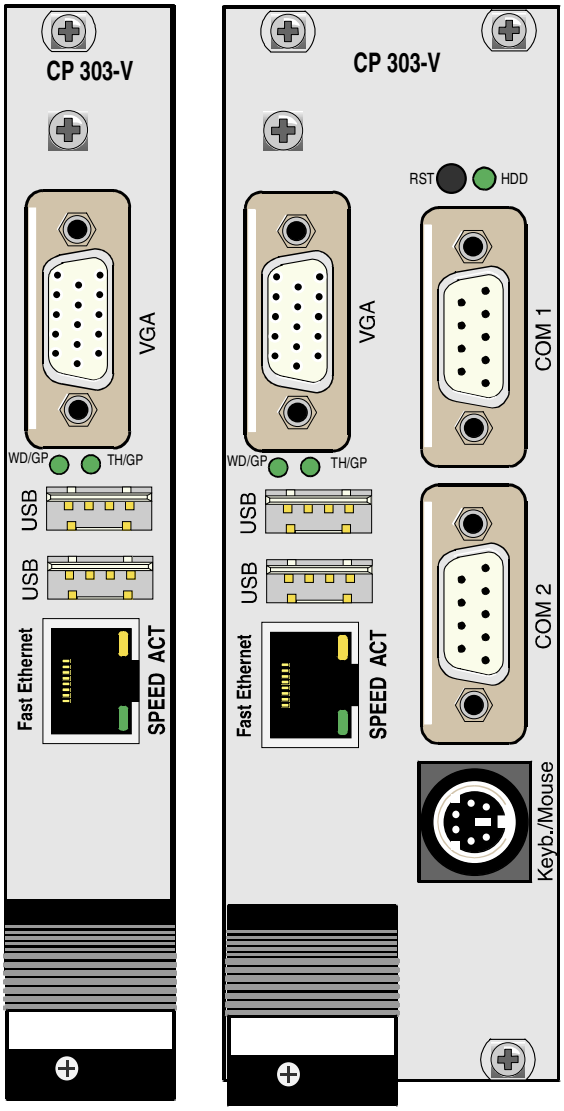
D.4.1 Functional Block Diagram

Figure D-1: CP303-V Functional Block Diagram



D.5 Front Panels

Figure D-2: CP303-V 4HP and 8HP Front Panels



LEGEND:

Left CP303-V: 4HP version

Right CP303-V: 8HP version

General Purpose LEDs

- WD/GP (green): Watchdog or General Purpose
- TH/GP (green): Overtemperature Status or General Purpose

Integral Ethernet LEDs

- ACT (yellow): Ethernet Link/Activity
- SPEED (green): Ethernet Speed

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D.6 Board Layouts

Figure D-3: CP303-V Board Layout (Front View)

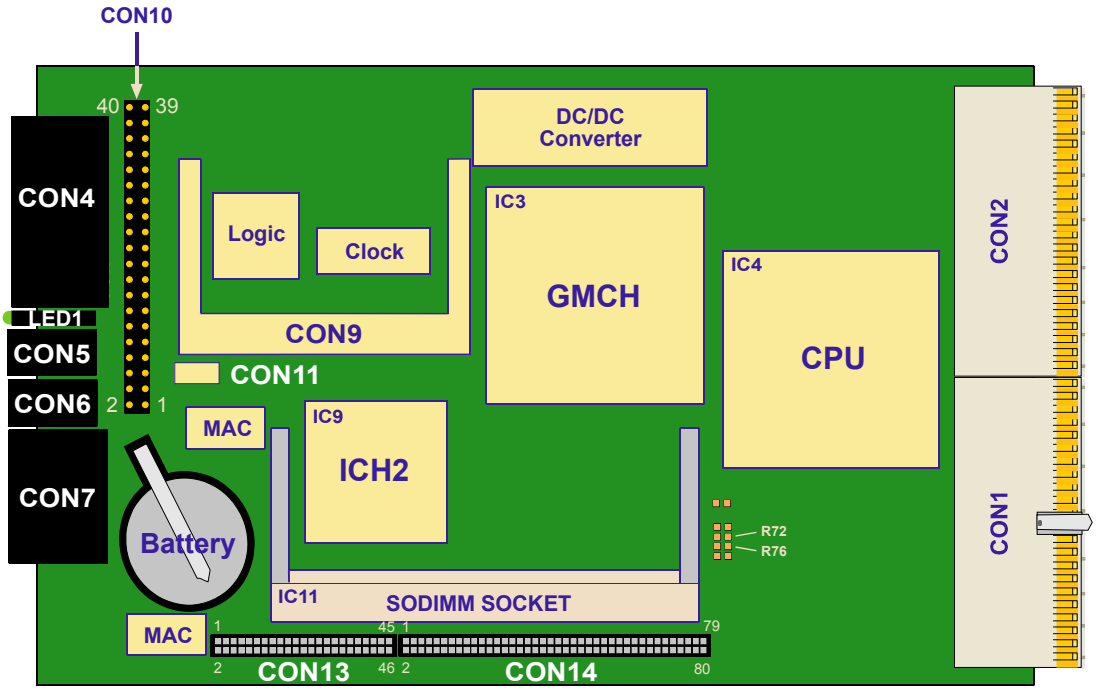
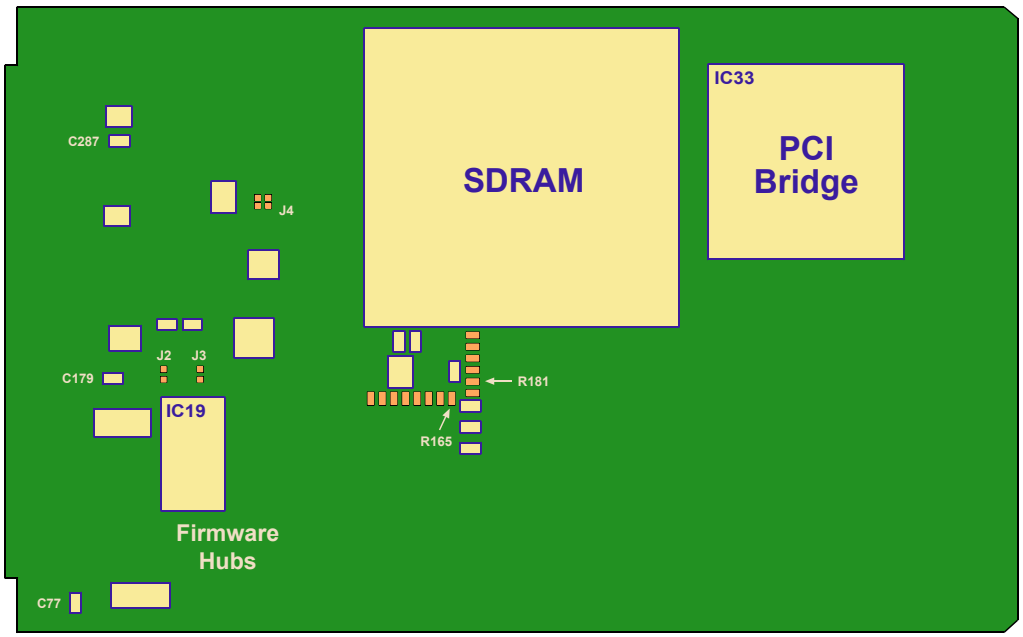


Figure D-4: CP303-V Board Layout (Reverse View)



D.7 Technical Specifications

Table D-1: CP303-V 4HP Version Main Specifications

	CP303-V	SPECIFICATIONS
Processor and Memory	CPU	Ultra Low Voltage Intel® Celeron® Processor (0.13m) 400 MHz Low Voltage Intel® Celeron® Processor (0.13m) 1000 MHz with 256 kB L2 on-die cache in 479 Micro-FCBGA packaging.
	Memory	Main Memory (up to 512 MB total memory): up to 512 MB SDRAM via one SODIMM socket running at 133 MHz Cache structure: 256 kB L2 on-die full speed processor cache Flash Memory: 1 MB Flash for BIOS Memory Extension: CompactFlash socket type II (true IDE mode / no DMA support) EEPROM: Two 256 byte EEPROMs for storing CMOS data when operating without battery and two 256 byte EEPROM for user purposes
Chipset	Intel 815-B0 Graphics Memory Controller Hub (GMCH) chipset	Support for a single Celeron® microprocessor 64-bit AGTL/AGTL+ based System Bus interface at 66/100/133 MHz 64-bit System Memory interface with optimized support for SDRAM at 133 MHz Integrated 2D and 3D Graphics Engines Integrated H/W Motion Compensation Engine Integrated 230 MHz DAC Integrated Digital Video Out Port AGP 1X/2X/4X Controller
	Intel ICH2 I/O Controller Hub (ICH)	PCI Rev 2.2 compliant with support for 32-bit/33 MHz PCI operations Supports up to six Req/Gnt pairs Power management logic support Enhanced DMA controller, interrupt controller, and timer functions Integrated IDE controller Ultra ATA/100/66/33 USB host interface with two host controllers; supports 4 USB ports Integrated LAN controller (82559 style) System Management Bus (SMBus) compatible with most I2C devices AC™97 2.1 compliant link for audio codecs Low Pin Count (LPC) interface Firmware Hub (FWH) interface support

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Table D-1: CP303-V 4HP Version Main Specifications (Continued)

	CP303-V	SPECIFICATIONS
External Interfaces	VGA interface	Built-in Intel® 3D Graphics accelerator for enhanced graphics performance. Supports resolutions of up to 1600 x 1200 x 8-bit colors at a 75 Hz refresh rate or 1280 x 1024 x 24-bit true colors at an 85 Hz refresh rate. Hardware motion compensation for software MPEG2 and MPEG4 decoding. The graphics controller provides flexible allocation of video memory (frame buffer) up to 16 MB and 1MB legacy video memory for real-time operating systems (e.g. MS DOS).
	Fast Ethernet Interface	Single Channel Ethernet by Intel® 82801 (ICH2) chipset integrated LAN controller Data Rate: 10 & 100 MBit/s Ethernet: Full 802.2 & 802.3 IEEE compliance supporting 10Base-T and 100Base-TX. Cabling: Category 5 two-pair cabling
	USB Interface	The ICH2 contains two USB 1.1 UHCI compliant host controllers with a data transfer rate of up to 12 Mbit/s. Each Host controller includes a root hub with two separate USB ports for each, making a total of four USB ports (two at front I/O, two at rear I/O).
	Serial Ports	Up to Four UARTs, 16C550 compatible. Two on the 4HP version (rear I/O) and two on the CP303-IDE1 module
	CompactPCI Bus Interface	Compatible with CompactPCI Specification V 2.0, Rev. 3.0 64-bit/33 MHz master interface 3.3V/5.0V compatible (default configuration 5.0 V)
	Hot Swap Compatible	The CP303-V supports the addition or removal of other boards whilst in a powered-up state. Individual clocks for each slot and Enum signal handling are in compliance with the PICMG 2.1 Hot Swap Specification.
	Rear I/O	When the rear I/O is enabled the CompactPCI interface is configured for 32-bit/33 MHz. The 32-bit CompactPCI bus has rear I/O capability. The following interfaces are routed to the rear I/O connector J2: COM1 and COM2 (TTL signaling), 2xUSBs, CRT VGA, 2xEthernets and general purpose signals.
General	Dimensions, Operating Temperatures, Climatic Humidity, Weight	Dimensions: 100 mm x 160 mm Operating temp.: 0°C to +60°C Storage temp.: -55°C to +85°C Climatic humidity: 93% RH at 40 °C, non-condensing Weight: CP303-V 4HP with heat sink: 337 grams

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Table D-1: CP303-V 4HP Version Main Specifications (Continued)

	CP303-V	SPECIFICATIONS
Interfaces	Front Panel Interfaces - 4HP VGA Version	VGA: 15-pin D-SUB connector USB: two 4-pin connectors Ethernet: one RJ-45 connectors One LED yellow: (integrated in Ethernet RJ45 jack): Ethernet Link/Activity One LED green: (integrated in Ethernet RJ45 jack): Ethernet Speed Two LED green: Watchdog, Overtemperature Status or General Purpose
	Onboard interfaces	One EIDE interface supporting Ultra ATA/100/66/33 for two devices (hard disks or CD-ROMs) on a 40-pin 2.54mm connector. CompactFlash socket for type II devices (primary EIDE interface) I/O extension connector
Hardware Monitoring	Thermal Management/ System Monitoring	Watchdog: software configurable watchdog generates IRQ, NMI or hardware reset. Hardware monitor: LM81 monitoring temperature, fan speed and all onboard voltages. Temperature monitor: MAX 1617 monitoring the CPU on-die and board temperature.
	Common Features	DC power monitors (3.3V and 5V) Battery socket and 3.0V lithium battery for RTC: VARTA Type CR2025 PANASONIC BR2020
Software	Software BIOS and Operating System Support	Award BIOS within 1 MB of Flash memory and having the following features: - Award Preboot Agent included; this allows BIOS updates and service functions without VGA or a local disk - LAN-boot capability for diskless systems - Boot from USB floppy and CD-ROM - BIOS boot support for USB keyboards - Software enable/disable function for the rear I/O, Ethernet and COM port configuration for the 4 HP version - Plug and Play capability - Dual BIOS support - The BIOS parameters are saved in the EEPROM - Board serial number in EEPROM - PC Health Monitoring, which allows you to protect your system from problems even before they occur Operating systems supported: Linux, VxWorks®, Windows NT®4.0, Windows 2000 etc.

Note ...

For a description of the additional 8HP version interfaces, please refer to the Technical Specifications table in Appendix A, CP303-IDE1 module.

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D.8 Power and System Considerations

D.8.1 CP303-V Voltage Ranges

The CP303-V board itself has been designed for optimal power input and distribution. Still it is necessary to observe certain criteria essential for application stability and reliability.

The table below indicates the absolute maximum input voltage ratings that must not be exceeded. Power supplies to be used with the CP303-V should be carefully tested to ensure compliance with these ratings.

Table D-2: Absolute Maximum Ratings

SUPPLY VOLTAGE	ABSOLUTE MAXIMUM RATINGS
+3.3 V	+3.6 V
+5 V	+5.5 V
+12 V	+14.0 V
-12 V	-14.0 V

Warning!

The maximum permitted voltage indicated in the table above must not be exceeded. Failure to comply with the above may result in damage to your board.

The following table specifies the ranges for the different input power voltages within which the board is functional. The CP303-V is not guaranteed to function if the board is not operated within the prescribed limits.

Table D-3: DC Operational Input Voltage Ranges

INPUT SUPPLY VOLTAGE	ABSOLUTE RANGE	RECOMMENDED RANGE	REMARKS
+3.3 V	3.2 V min. to 3.47 V max.	3.3 V min. to 3.47 V max.	Main voltage
+5 V	4.85 V min. to 5.25 V max.	5.0 V min. to 5.25 V max.	Main voltage
+12 V	11.4 V min. to 12.6 V max.	12 V min. to 12.6 V max.	Not required
-12 V	-11.4 V min. to -12.6 V max.	-12 V min. to -12.6 V max.	Not required

D.8.2 Backplane Requirements

Backplanes to be used with the CP303-V must be adequately specified. The backplane must provide optimal power distribution for the +3.3 V, +5 V and +12 V power inputs. It is recommended to use only backplanes which have two power planes for the 3.3 V and +5 V voltages.

Input power connections to the backplane itself should be carefully specified to ensure a minimum of power loss and to guarantee operational stability. Long input lines, under dimensioned cabling or bridges, high resistance connections, etc. must be avoided. It is recommended to use POSITRONIC or M-type connector backplanes and power supplies where possible.

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D.8.3 Power Supply Units

Power supplies for the CP303-V must be specified with enough reserve for the remaining system consumption. In order to guarantee a stable functionality of the system, it is recommended to provide more power than the system requires. An industrial power supply unit should be able to provide at least twice as much power as the entire system requires. An ATX power supply unit should be able to provide at least three times as much power as the entire system requires.

As the design of the CP303-V has been optimized for minimal power consumption, the power supply unit shall be stable even without minimum load.

Where possible, power supplies which support voltage sensing should be used. Depending on the system configuration this may require an appropriate backplane. The power supply should be sufficient to allow for die resistance variations.

Note ...

Non-industrial ATX PSUs require a greater minimum load than a single CP303-V is capable of creating. When a PSU of this type is used, it will not power up correctly and the CP303-V may hangup. The solution is to use an industrial PSU or to add more load to the system.

The start-up behavior of CompactPCI and PCI (ATX) power supplies is critical for all new CPU boards. These boards require a defined power of sequence and start-up behavior of the power supply. The required behavior is described in the ATX (http://www.formfactors.org/FFDetail.asp?FFID=1&CatID=2) and the CompactPCI (PICMG, http://www.picmgeu.org/) specification.

D.8.3.1 Voltage Ramp

Power supplies must comply with the following guidelines, in order to be used with the CP303-V.

- Beginning at 10% of the nominal output voltage, the voltage must rise within > 0.1 ms to < 20 ms to the specified regulation range of the voltage. Typically: > 5 ms to < 15 ms.
- There must be a smooth and continuous ramp of each DC output voltage from 10% to 90% of the regulation band.
- The slope of the turn-on waveform shall be a positive, almost linear voltage increase and have a value from 0 V to nominal Vout.

D.8.3.2 Voltage Sequencing Requirements

The +5 VDC output level must always be equal to or higher than the +3.3 VDC output during power-up and normal operation.

D.8.3.3 Rise Time Diagram

The following figure illustrates an example of the recommended voltage ramp of a CompactPCI power supply for all Kontron boards delivered up to now.

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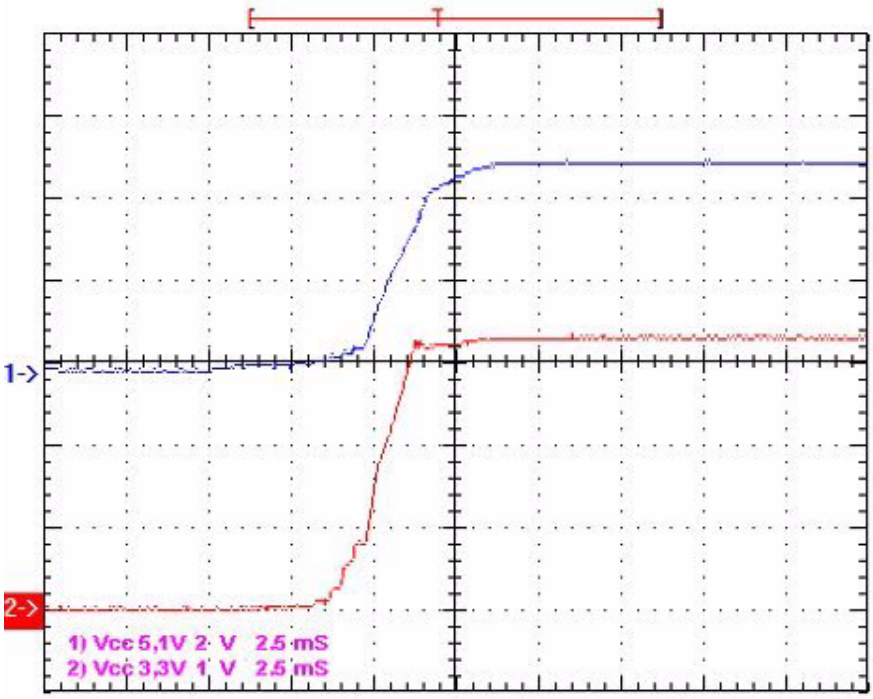
Figure D-5: Voltage Ramp of the CP3-SVE180 AC Power Supply



D.8.3.4 Recommended Operating Conditions

The tolerance of the voltage lines is described in the CompactPCI specification (PICMG 2.0 R3.0).The recommended measurement point for the voltage is the CompactPCI connector on the CPU board.

The following table provides information regarding the required characteristics for each board input voltage.

Table D-4: Input Voltage Characteristics

VOLTAGE	NOMINAL VALUE	TOLERANCE	MAX. RIPPLE (p-p)
5 V	+5.0 VDC	+5%/-3%	50 mV
3.3 V	+3.3 VDC	+5%/-3%	50 mV
+12 V	+12 VDC	+5%/-5%	240 mV
-12 V	-12 VDC	+5%/-5%	240 mV
V I/O (PCI signaling voltage)	+3.3 VDC or +5 VDC	+5%/-3%	50 mV
GND	Ground, not directly connected to potential earth (PE)		

The output voltage overshoot generated during the application (load changes) or during the removal of the input voltage must be less than 5% of the nominal value. No voltage of reverse polarity may be present on any output during turn-on or turn-off.

D.8.3.5 Supply Voltage Regulation

The power supply shall be unconditionally stable under line, load, unload and transient load conditions including capacitive loads. The operation of the power supply must be consistent even without the minimum load on all output lines.

Note ...

Non-industrial ATX PSUs require a greater minimum load than a single CP303-V is capable of creating. When a PSU of this type is used, it will not power up correctly and the CP303-V may hang up. The solution is to use an industrial PSU or to add more load to the system.

Note ...

If the main power input is switched off, the supply voltages will not go to 0V instantly. It will take a couple of seconds until capacitors are discharged. If the voltage rises again before it has gone below a certain level, the circuits may enter a latch-up state where even a hard RESET will not help any more. The system must be switched off for at least 3 seconds before it may be switched on again. If problems still occur, turn off the main power for 30 seconds before turning it on again.

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D.8.4 Power Consumption

The CP303-V board is based on the Intel® Celeron® Processor. Intel® has developed mobile processors to meet the specific needs of mobile PC's. As such, they operate at lower voltages than their desktop counterparts, are significantly smaller in size, consume less power and dissipate less heat. The design is optimized for low power consumption applications.

The goal of this description is to provide a method to calculate the power consumption for the CP303-V base board and for additional configurations. The processor dissipates the majority of the thermal power.

The power consumption tables below list the voltage and current specifications for the CP303-V board and the CP303-V accessories. The values were measured using an 8-slot passive CompactPCI backplane with two power supplies, one for the CPU and the other for the hard disk. During measurement the power consumption of the backplane was ignored. The operating systems in use were DOS 6.22 without power management and Windows 2000 with power management. All measurements were conducted at a temperature of 25°C. The measured values varied, because power consumption was dependent on processor activity.

Table D-5: Power Consumption Table Windows 2000/NT IDLE MODE

POWER	400 MHz 256 MB MEMORY	1000 MHz 256 MB MEMORY
Core Voltage	0.95 V	1.15 V
5 V	1.7 W	3.1 W
3.3 V	6.6 W	6.5 W
Total	8.3 W	9.6 W

Note ...

The above values were measured with no application started and without keyboard.

Table D-6: Power Consumption DOS (without keyboard)

POWER	400 MHz 256 MB MEMORY	1000 MHz 256 MB MEMORY
Core Voltage	0.95 V	1.15 V
5V	2.7 W	7.9 W
3.3V	6.6 W	7.1 W
Total	9.3 W	15 W

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Table D-7: Power Consumption Windows 2000/NT 100% CPU Usage

POWER	400 MHz 256 MB MEMORY	1000 MHz 256 MB MEMORY
Core Voltage	0.95 V	1.15 V
5 V	3.5 W	10.9 W
3.3 V	6.6 W	6.5 W
Total	10.1 W	17.4 W

Note ...

The above values are with Windows/NT running with 100% CPU usage, the INTEL HiPower tool started and without keyboard.

Analysis indicates that real applications does not reach the maximum possible power consumption of the HiPower tool, the maximum power consumption is 20 - 30% lower than the measured value.

Table D-8: Power Consumption for CP303-V Accessories

MODULE	POWER 5V	POWER 3.3V
Keyboard	100 mW	--
SODIMM module	--	500 mW - 1.5 W
CompactFlash	--	100 mW - 300 mW

D.8.5 Temperature Range

The CP303-V is a CompactPCI board capable of operating within the temperature range from 0°C up to +60°C.

D.8.5.1 Temperature Range and Air Flow

These values have been measured with typical applications under DOS and Windows 2000. In worst case situations the values and the temperature range must be reduced accordingly. For all situations the maximum junction temperature of the Intel® Celeron® Processor must be below 100°C. This temperature value can be measured with the onboard remote temperature sensor. In instances of overtemperature the hardware monitor will reduce the processor clock to reduce power consumption.

Table D-9: Typical Temperature Range and Minimum Required Air Flow

HEAT SINK VERSION	TA RANGE	400 MHz	1000 MHz
4HP	0°C to 60°C	0.2 m/s	0.5 m/s - 0.8 m/s

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Warning!

The temperature ranges detailed above assume that any appended hard disk is capable of operating at these temperatures. The user must ensure that any appended hard disk can function at the operating temperatures expected.

TA is the initial temperature of the ambient air used for convectional cooling of the board. In a typical installation where the board is mounted vertically in a system rack, this would be the temperature of the air measured at the bottom of the board before the air flows over the board.

If the board is to be operated at or near the minimum air flow speed, it is imperative to verify that it can be safely operated before the board is integrated in an application system. This will require an empirical thermal design analysis and verification by the system designer.

0.2 m/s air flow means standard convection cooling with the board in an upright position. An airflow of 1 - 1.2 m/s is a typical value for a standard *Kontron* ASM 4 rack (3U CompactPCI rack with 1U cooling fans). For other racks or housings the available airflow will differ. The maximum ambient temperature must be recalculated and/or measured for such environments. For the calculation of the maximum ambient temperature the processor junction temperature must never exceed 100°C. The maximum heat sink temperature depends on the physical characteristics of the heat sink and thermal connection to the processor. To ensure that the heat sink temperature does not exceed its limits an airflow may be needed for a given ambient temperature. Heat sink temperature is measured at the top of the heat sink base, closest to the processor.

Warning!

It is the responsibility of the end user to ensure that the processor junction temperate never exceeds 100°C in order to protect the board against overheating. Permanent overheating can damage the board.

If the temperature on the processor junction is greater than 100°C the maximum ambient temperature must be reduced or an external airflow must be provided by means of an additional fan.

Note ...

The BIOS supports a temperature control function, If the temperature is too high, the sensors automatically reduce the CPU clock frequency, depending on the mode chosen in the BIOS setup.

D.8.6 Storage Temperatures

- Storage temperature without hard disk –55°C to +85°C
- Storage temperature with hard disk –40°C to +65°C
- Humidity non-condensing 93% RH at 40 °C, non-condensing

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D.9 Applied Standards

The *Kontron Modular Computers'* CompactPCI systems comply with the requirements of the following standards.

Table D-10: Applied Standards

COMPLIANCE	TYPE	STANDARD	TEST LEVEL (RUGGEDIZED VERSION)
CE	Emission	EN55022 EN61000-6-3	--
	Immission	EN55024 EN61000-6-2	--
	Electrical Safety	EN60950	--
Mechanical	Mechanical Dimensions	IEEE 1101.10	--
Environmental Aspects	Vibration (Sinusoidal)	IEC68-2-6	2g/12-300Hz/10 acceleration / frequency range / test cycles
	Random Vibration (Broadband)	IEC68-2-64 (3U boards)	20-500Hz,0.1g²/500-2000Hz, 0.01g²/7g rms/3/30min frequency range1 / frequency range2 /acceleration / cycle / duration
	Permanent Shock	IEC68-2-29	15g/11ms/3000/1s peak acceleration / shock duration half sine / number of shocks / recovery time
	Single Shock	IEC68-2-27	30g/9ms/18/5s peak acceleration / shock duration / number of shocks / recovery time in sec.
	Climatic Humidity	IEC60068-2-78	--

D.10 Related Publications

The following publications contain information relating to this product.

Table D-11: Related Publications

PRODUCT	PUBLICATION
CompactPCI Systems and Boards	CompactPCI Specification 2.0, Rev. 3.0
	Hot Swap Specification PICMG 2.1
	Kontron Modular Computers' CompactPCI System Manual, ID 19954
CompactFlash Cards	CF+ and CompactFlash Specification Revision 1.4

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