Kontron User's Guide

COMe-bCD2

Document Revision 120

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1 User Information

1.1 About This Manual

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For the circuits, descriptions and tables indicated, Kontron assumes no responsibility as far as patents or other rights of third parties are concerned.

1.2 Copyright Notice

1.3 Trademarks

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- Microsoft is a registered trademark of Microsoft Corp.
- Intel is a registered trademark of Intel Corp.
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1.4 Standards

Kontron Embedded Modules GmbH is certified to ISO 9000 standards.

1.5 Warranty

This Kontron Embedded Modules GmbH product is warranted against defects in material and workmanship for the warranty period from the date of shipment. During the warranty period, Kontron Embedded Modules GmbH will at its discretion decide to repair or replace defective products.

Within the warranty period, the repair of products is free of charge as long as warranty conditions are observed.

The warranty does not apply to defects resulting from improper or inadequate maintenance or handling by the buyer, unauthorized modification or misuse, operation outside of the product's environmental specifications or improper installation or maintenance.

Kontron Embedded Modules GmbH will not be responsible for any defects or damages to other products not supplied by Kontron Embedded Modules GmbH that are caused by a faulty Kontron Embedded Modules GmbH product.

1.6 Technical Support

Technicians and engineers from Kontron Embedded Modules GmbH and/or its subsidiaries are available for technical support. We are committed to making our product easy to use and will help you use our products in your systems. Please consult our Web site at http://www.kontron.com/support for the latest product documentation, utilities, drivers and support contacts. Consult our customer section http://emdcustomersection.kontron.com for the latest BIOS downloads, Product Change Notifications and additional tools and software. In any case you can always contact your board supplier for technical support.

2 Introduction

2.1 COMe-bCD2

Based on the COM Express standard, Kontron's COMe-bCD2, powered by a variety of Intel Pentium core duo processors, is a next-generation embedded module that brings advanced technology to tomorrow's applications, as well as continuing today's legacy devices. Built around serial differential signaling technologies, COMe-bCD2 modules incorporate the following interfaces into a 95 x 125 small form factor embedded module:

- Core 2 Duo / Core Duo / Celeron M
- PCI Express, which provides a high performance I/O infrastructure with transfer rates starting at 2.5 Giga transfers per second over a x1 PCI Express lane
- PCI
- Serial ATA (SATA II)
- USB 2.0
- LVDS
- Intel High Definition Audio
- Advanced Configuration and Power Interface (ACPI) for optimized power management

The COMe-bCD2 is built around the Intel Core Duo processors that use the Yonah and Merom Cores and the Mobile Intel 945GME Express chipset, which is the first mobile platform to offer PCI Express functionality with extended life cycle support. These modules feature the most current desktop features such as USB 2.0, SATA, and PCI Express buses.

The COMe-bCD2 delivers up to 2GHz performance and up to 2GB DDR2 RAM. For applications that require advanced real-time video capabilities, the COMe-bCD2 has integrated graphics based on the Intel® Graphics Media Accelerator 900 architecture and also supports PCI Express graphics.

Fast communications are possible courtesy of a Gigabit Ethernet port.

The COMe-bCD2 supports 5 PCI Express x1 Lanes and PCI Express cards as well as established hardware solutions based on current buses such as 32-bit PCI. A Gigabit Ethernet port provides fast connectivity to LAN/WAN and 8 USB 2.0 ports provide fast and sufficient interfaces for external peripherals.

COMe-bCD2 modules also provide the following interfaces that are always located in the same physical position on each board:

PCI-express, PCI32, USB, serial ATA (SATA), parallel ATA (PATA), LVDS Multi Media ports, as well as an ACPI (Advanced Configuration and Power Interface) for optimized power management. Six mounting holes on the board provide secure mounting to allow the module increased shock and vibration resistance.

2.2 COMe-bCD2 Release Versions

The COMe-bCD2 module is available in two different versions. The single channel version has one memory socket and the dual channel verison has two memory sockets. All statements in this document are valid for both versions, except they market to be only valid for one version. Statements only valid for the single channel version are highlighted in a light blue color and statements only valid for the dual channel version are highlighted in a green color.

The main differences are:

2.2.1 Single Channel Version

- Article number ends with a "-0", "-1", "-2" or "-3"
- One memory socket
- 5 PCIexpress lanes of the chipset; Onboard LAN uses PCIexpress lane 1
- No S3 cold support
- Strict 12V supply voltage
- Intel® 945GM
- Ethernetcontroller: Realtec RTL8111B
- Temperature sensor: LM 64

2.2.2 Dual Channel Version

- Article number ends with a "-4", "-5" or "-6"
- Two memory sockets
- 5PCIexpress lanes of the chipset; Onboard LAN uses PCIexpress lane 5 which allows optionally a x4 lane
- S3 cold support
- Wide Range power input from 8.5V to 18V
- Intel® 945GME
- Ethernetcontroller: Realtec RTL8111C
- Temperature sensor: LM 87

2.3 COMe-bCD2 Module Overview

The international COM Express standard defines two new form factor sizes: Basic and Extended. The primary difference between the Basic and Extended size is a larger board size and thermal envelope in the Extended size. The COMe-bCD2 follows the basic form factor.

Five module Pin-out Type definitions exist for Basic and Extended modules. Pin-out Types 1-5 apply to Basic and Extended module form factors. Pin-out Types 1-5 offer different functionalities. For a complete explanation of the features of each of the Pin-out Types 1-5, please see the COM Express® Specification.

The COMe-bCD2 uses the Pin-out Type 2 architecture, which includes PCI and IDE interfaces. These modules either use onboard graphics capabilities or may use 16 PEG lanes to connect to an external video controller. In case of onboard graphics, PEG pins may be alternatively used for two SDVO ports.

Pin-out Type 2 features include:

- Dual 220 pin connectors (Primary Connector: Rows A-B and Secondary Connector: Rows C-D, 440 pins total)
- 32-bit PCI interface
- IDE port (to support legacy ATA devices)
- Up to 5 PCI Express general purpose lanes
- One, x16 PCI Express Graphics (PEG) slot
- SDVO option (pins shared with PCI Express Graphics)
- Maximum module input power capability extended to 188W
- Up to 8 USB 2.0 ports; 4 shared over-current lines
- Up to 4 Serial ATA or SAS ports
- Dual 24-bit LVDS channels
- Analog VGA and TV Out: Composite Video, S-Video, Component Video (YPbPr)
- Intel High Definition Audio (Azalia) and AC '97 digital audio interface (external CODEC)
- Single Ethernet interface with integrated PHY
- +12V primary power supply input, +5V standby and 3.3V RTC power supplies

2.4 Understanding COM Express® functionality

All Kontron COM Express® basic and compact modules contain two connectors, each of which has two rows. The primary connector has two rows called Row A and Row B. The secondary connector has two rows called Row C and Row D.

The primary connector (Row A and Row B) feature the following legacy-free functionality:

- Ethernet
- Serial ATA (SATA)
- USB 2.0
- LVDS/VGA and dual display video
- Intel High Definition Audio (Azalia)
- LPC, an Intel proprietary low-pin count (LPC), which supports low-speed devices such as RS-232 serial and parallel ports.

The secondary connector (Row C and Row D) provides support for the following buses and I/O:

- PCI Express
- PCI
- IDE

2.5 COM Express® Documentation

This product manual serves as one of three principal references for an COM Express® design. It documents the specifications and features of COMe-bCD2. The other two references, which are available from your Kontron Support, include:

- The COMexpress Specification define the module form factor, pinout, and signals.
- The Carrier Board Design Guide serves as a general guide for baseboard design, with a focus on maximum flexibility to accommodate a wide range of COM Express® modules.

Note: Some of the information contained within this product manual applies only to certain product revisions (CE: xxx). If certain information applies to specific product revisions (CE: xxx) it will be stated. Please check the product revision of your module to see if this information is applicable.

2.6 COM Express® Benefits

COM Express® basic modules are very compact (125 x 95 mm, 12mm thick), highly integrated computers. All COM Express® modules feature a standardized form factor and a standardized connector layout that carry a specified set of signals. Each COM Express® module is based on connector type of the COMexpress specification. This standardization allows designers to create a single-system baseboard that can accept present and future COM Express® modules.

COM Express® modules include common personal computer (PC) peripheral functions such as:

- Graphics
- USB ports
- Ethernet
- Sound
- IDE (and SATA)

The baseboard designer can optimize exactly how each of these functions implements physically. Designers can place connectors precisely where needed for the application on a baseboard designed to optimally fit a system's packaging.

A peripheral PCI bus can be implemented directly on the baseboard rather than on mechanically unwieldy expansion cards. The ability to build a system on a single baseboard using the computer as one plug-in component simplifies packaging, eliminates cabling, and significantly reduces system-level cost.

A single baseboard design can use a range of COM Express® modules. This flexibility can differentiate products at various price/performance points, or to design future proof systems that have a built-in upgrade path. The modularity of an COM Express® solution also ensures against obsolescence as computer technology evolves. A properly designed COM Express® baseboard can work with several successive generations of COM Express® modules.

An COM Express® baseboard design has many advantages of a custom, computer-board design but delivers better obsolescence protection, greatly reduced engineering effort, and faster time to market.

3 Specifications

3.1 Functional Specifications

Processor

- Intel® Celeron® M, Core Duo® (Yonah Core)or Core2Duo® (Merom core) processor

Bus

- 533 / 667 MHz CPU bus
- 533/667 MHz memory bus

Chipset

- Intel® 945GM (see 2.2.1)
- Intel® 945GME (see 2.2.2)
- ICH7M-DH

Cache, Second level

- 1MB (Celeron® M)
- 2x1MB (Core Duo®)
- 4MB (Core2Duo®)

Memory

- One 200-pin DDR2-SO-DIMM (-533 or -667) (see 2.2.1)
- Two 200-pin DDR2-SO-DIMM (-533 or -677) (see 2.2.2)

Note: COMe-bCD2 equipped with the CeleronM423 is not able to drive memory modules faster than DDR2-533.

Note: The dual channel version would be theoretically able to support 4GB of RAM. Practically this feature is in the chipset not supported, therefore that maximum amount of RAM is about 3.3 GByte

PCI Express Graphics (PEG): Intel® 945GM/GME

- One 16-lane PCI Express port for external PCI Express based graphics card

Serial Digital Video Output (SDVO): Intel® 945GM/GME

- Concurrent Operation of PCI Express Graphics with SDVO
- Supports appropriate external SDVO compontents (DVI, LVDS, TV-out)

PCI Express: Intel® ICH7M-DH

- 5 PCI Express x1 lanes
- Optionally 1 x4 lane and 1 x1 lane is possible by strapping option on the baseboard. (see 2.2.2) To use this feature please pull-up AC_SYNC (A29) and AC_SDOUT (A33) to 3.3V.

PCI 32: Intel® ICH7M-DH

- Parallel PCI Bus 32 bit 33 MHz

Low Pincount Bus (LPC): Intel® ICH7M-DH

Enhanced Intelligent Drive Electronics (EIDE): Intel® ICH7M-DH

- One PCI Bus Master IDE port
- Supports 2 IDE devices
- Ultra 100 Direct Memory Access (DMA) mode
- Programmed Input/Output (PIO) modes up to Mode 4 timing
- Multiword DMA Mode 0,1,2 with independent timing

Serial ATA: Intel® ICH7M-DH

- 2 Channels Serial ATA
- SATA Spec. Rev. 1.0 up to 150 MB/s per channel
- SATA II (AHCI)
- Supports RAID level 0 and 1

Universal Serial Bus: Intel® ICH7M-DH

- 8 USB 1.1/2.0 ports (UHCI and EHCI)
- USB legacy keyboard support
- USB floppy, CD-ROM, Hard drive, and memory stick boot support

Gigabit Ethernet: Realtek RTL8111B/C 10/100/1000

- Fully compatible with IEEE 802.3, IEEE 802.3u, IEEE 802.3ab

Onboard video graphics array (VGA): Intel® 945GM/GME:

- Intel® Gen 3.5 Graphics engine
- Dynamic Video Memory Technology (DVMT 3.0)
- Cathode ray tube (CRT) up do QXGA
- low voltage differential signaling (LVDS) liquid-crystal display (LCD) and SDVO interfaces up to UXGA
- Supports DX 9.1

AC '97 (Audio): Intel® 945GM/GME;

- Up to 20 bit sample resolution
- Multiple sample rates up to 48bit
- Independent bus master logic for dual Microphone Input, dual PCM audio input, PCM audio input, modem input, modem output and S/PDIF output.

Television output: Intel® 945GM/GME

- 3 integrated 10bit DACs
- Overscaling
- NTSC/PAL
- HDTV support: 480p / 780p / 1080i / 1080p

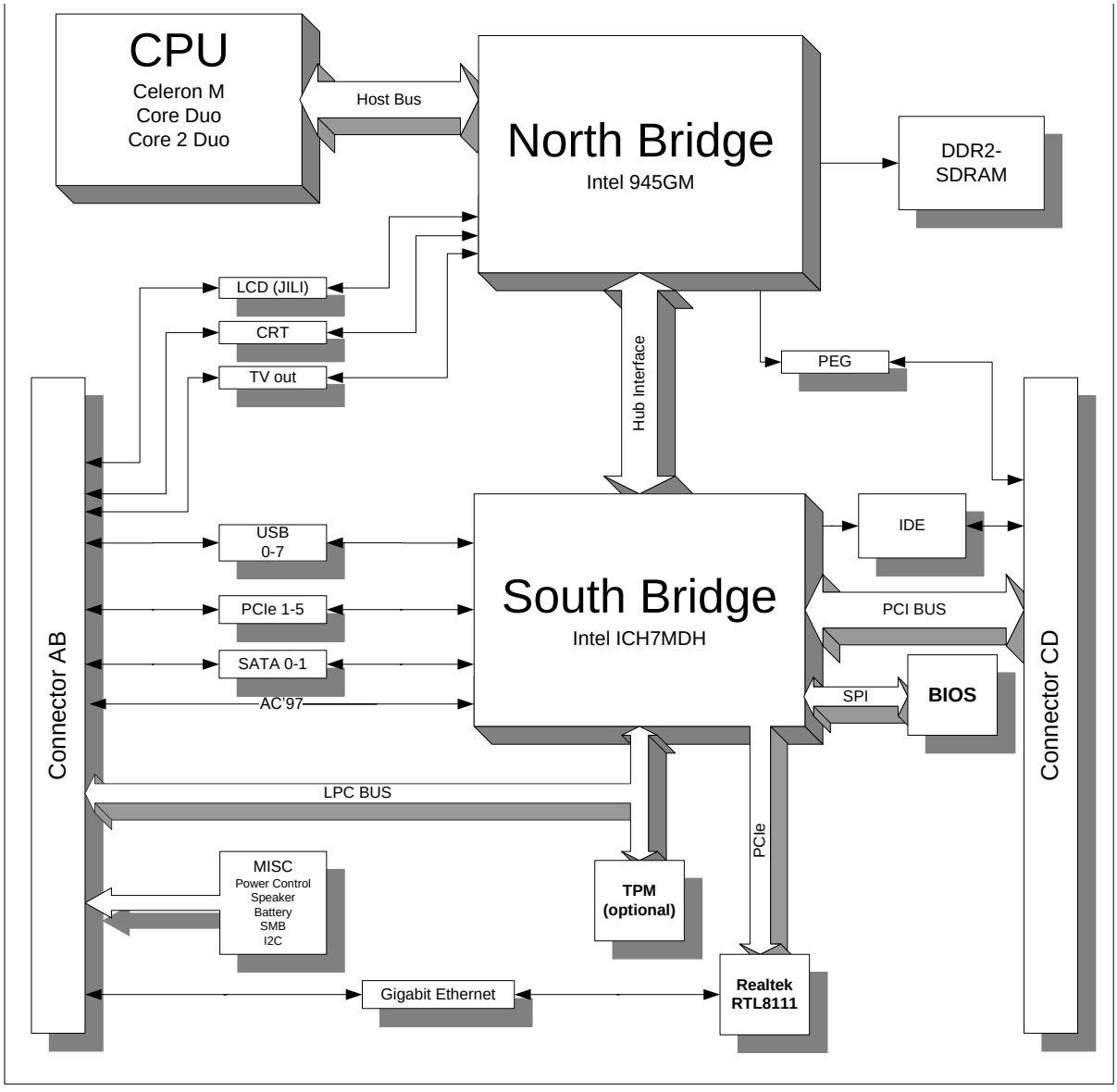
BIOS: Phoenix, 1MB Flash-BIOS in Firmware Hub Flash Memory

- NV-EEPROM for CMOS-setup retention without battery

Watchdog timer (WDT): Xilinx Microcontroller

Real-time clock (requires external battery)

3.1.1 Block diagram



3.2 Mechanical Specifications

Dimensions

- 95.0 mm x 125.0 mm
- Height approx. 12 mm (0.4”)

3.3 Electrical Specifications

Supply Voltage

- 12V DC +/- 5%
- 8.5V DC to 18V DC widerange input (see 2.2.2)

Supply Voltage Ripple

- Maximum 100 mV peak to peak 0 – 20 MHz

Supply Current 5 V_SB

- 0,33 A in S5 mode
- 0,43 A in S0

Note: S3 cold will drive all the powersupply for memory refreshing and chip supply through the 5V_SB line. Therefore up to 2A of current is specified for the connectors and should be in mind when the powersupply is dimenstioned.
The board works also without a 5V_SB line but not the ACPI states S3 and S5.

3.3.1 Power Consumption

The maximum Power Consumption of the different COMe-bCD2 modules is between 18 - 40W (100% CPU load; 90°C CPU temperature). Further details with measurements and TDP values of the single variants can be found in our customer section. Information there is available after registration.

All boards were equipped with DDR2 SDRAM. The Modules were tested using maximum CPU frequency.

3.4 Environmental Specifications

3.4.1 Temperature

Operating: (with Kontron Embedded Modules heat-spreader plate assembly):

- Ambient temperature: 0°C to 60°C
- Maximum heatspreader-plate temperature: 0°C to 60°C

Non-operating: -30°C to 85°C

Note: The maximum operating temperature with the heatspreader plate is the maximum measurable temperature on any spot on the heatspreader's surface. You must maintain the temperature according to the above specification.

Operating (without Kontron Embedded Modules heat-spreader plate assembly):

- Maximum operating temperature: 0°C to 60°C

Non operating: -30 to +85 °C

Note: The maximum operating temperature is the maximum measurable temperature on any spot on a module's surface. You must maintain the temperature according to the above specification.

3.4.2 Humidity

- Operating: 10% to 90% (non condensing)
- Non operating: 5% to 95% (non condensing)

3.5 MTBF

The following MTBF (Mean Time Between Failure) values were calculated using a combination of manufacturer's test data, if the data was available, and a Bellcore calculation for the remaining parts. The Bellcore calculation used is "Method 1 Case 1". In that particular method the components are assumed to be operating at a 50 % stress level in a 40° C ambient environment and the system is assumed to have not been burned in. Manufacturer's data has been used wherever possible. The manufacturer's data, when used, is specified at 50° C, so in that sense the following results are slightly conservative. The MTBF values shown below are for a 40° C in an office or telecommunications environment. Higher temperatures and other environmental stresses (extreme altitude, vibration, salt water exposure, etc.) lower MTBF values.

- System MTBF (hours) for single channel memory version: **152941**
- System MTBF (hours) for dual channel memory version: **191206**

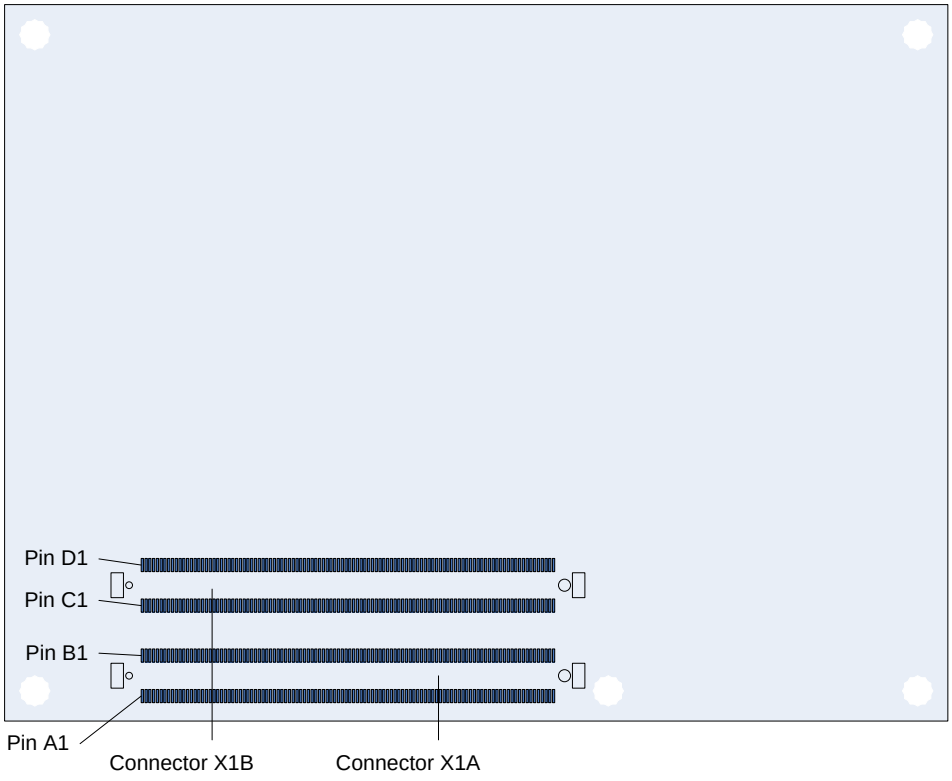
Notes: Fans usually shipped with Kontron Embedded Modules GmbH products have 50,000-hour typical operating life. The above estimates assume no fan, but a passive heat sinking arrangement.
Estimated RTC battery life (as opposed to battery failures) is not accounted for in the above figures and need to be considered for separately. Battery life depends on both temperature and operating conditions. When the Kontron unit has external power; the only battery drain is from leakage paths.

4 Connector Pinouts

4.1 Connector location

There are 2 connectors on the basic sized module. Connector X1A and Connector X1B are shown in the following drawing. It is a top layer view and the connectors are seen "through" the PCB.

Each connector consist s of 2 connector rows. Connector X1A has rows A and B and connector X1B has rows C and D.



4.2 Pinout tables

Type	Signal Description
I	Differential Pair Input
IO-2,5	Bi-directional 2,5 V IO-Signal
IO-3,3	Bi-directional 3,3 V IO-Signal
IO-5	Bi-directional 5 V IO-Signal
I-3,3	3,3 V Input
I-5	5 V Input
O	Differential Pair Output
OA	Output Analog
O-2,5	2,5 V Output
O-3,3	3,3 V Output
O-5	5 V Output
DP	Differential Pair Input/Output
PU	Pull-Up Resistor
PD	Pull-Down Resistor
PWR	Power Connection
Nc	Not Connected / Reserved

Notes: To protect external power lines of peripheral devices, make sure that: the wires have the right diameter to withstand the maximum available current the enclosure of the peripheral device fulfils the fire-protection requirements of IEC/EN60950

4.2.1 Connector X1A

Connector X1A (Signal Levels A1-A55)

Pin A1-A55 [LAN | Power | USB | SATA | PCIe | AUDIO]

Pin	Signal	Description	Type	Termination	Comment
A1	GND	Power Ground	PWR	-	-
A2	GBE0_MDI3-	LAN_RXD- | Ethernet Receive Data -	I	-	-
A3	GBE0_MDI3+	LAN_RXD- | Ethernet Receive Data -	I	-	-
A4	GBE0_LINK100#	LAN_100LED# | Ethernet Speed LED	O-3,3	-	On at 100Mb/s
A5	GBE0_LINK1000#	LAN_1000LED# | Ethernet Speed LED	O-3,3	-	On at 1000Mb/s
A6	GBE0_MDI2-	LAN_RXD- | Ethernet Receive Data -	I	-	-
A7	GBE0_MDI2+	LAN_RXD- | Ethernet Receive Data -	I	-	-
A8	GBE0_LINK#	LAN_LILED# | LAN Link LED	O-3,3	-	-
A9	GBE0_MDI1-	LAN_RXD- | Ethernet Receive Data -	I	-	-
A10	GBE0_MDI1+	LAN_RXD+ | Ethernet Receive Data +	I	-	-
A11	GND	Power Ground	PWR	-	-
A12	GBE0_MDI0-	LAN_TXD- | Ethernet Transmit Data -	O	-	-
A13	GBE0_MDI0+	LAN_TXD+ | Ethernet Transmit Data +	O	-	-
A14	GBE0_CTREF	ETH_CTREF	O-3,3	-	-
A15	SUS_S3#	PM_SLP_S#3	O-3,3	-	-
A16	SATA0_TX+	SATA0_TX+ | SATA 0 Transmit Data +	O	-	-
A17	SATA0_TX-	SATA0_TX- | SATA 0 Transmit Data -	O	-	-
A18	SUS_S4#	PM_SLP_S#4	O-3,3	-	-
A19	SATA0_RX+	SATA0_RX+ | SATA 0 Receive Data +	I	-	-
A20	SATA0_RX-	SATA0_RX- | SATA 0 Receive Data -	I	-	-
A21	GND	Power Ground	PWR	-	-
A22	SATA2_TX+	SATA0_TX+ | SATA 2 Transmit Data +	O	-	-
A23	SATA2_TX-	SATA0_TX- | SATA 2 Transmit Data -	O	-	-
A24	SUS_S5#	PM_SLP_S#5	O-3,3	-	-
A25	SATA2_RX+	SATA0_RX+ | SATA 2 Receive Data +	O	-	-
A26	SATA2_RX-	SATA0_RX- | SATA 2 Receive Data -	O	-	-
A27	BATLOW#	PM_BATLOW# | Battery Low	I-3,3	PU 8k2 3,3V	-
A28	ATA_ACT#	ATA_LED# | SATA LED	O-3,3	PU 10k 3,3V	-
A29	AC_SYNC	AC_SYNC | AC'97 Sync	O-3.3	-	int. PD 20k in ICH7–PU to 3.3V f. x4
A30	AC_RST#	AC_RST# | AC'97 Reset	O-3,3	-	int. PD 20k in ICH7
A31	GND	Power Ground	PWR	-	-
A32	AC_BITCLK	AC_BITCLK | AC'97 Clock	I-3,3	-	int. PD 20k in ICH7
A33	AC_SDOUT	AC_SDATAOUT | AC'97 Data	O-3,3	-	int. PD 20k in ICH7–PU to 3.3V f. x4
A34	BIOS_DISABLE#	BIOS_DISABLE#	I-3,3	-	-
A35	THRMTRIP#	PM_THRMTRIP#_CON	IO-3,3	PU 10k 3,3V	-
A36	USB6-	USB_PN6 | USB Data – Port6	DP	-	int. PD 15k in ICH7
A37	USB6+	USB_PP6 | USB Data + Port6	DP	-	int. PD 15k in ICH7
A38	USB_6_7_OC#	USB_OC#_6_7 | USB OverCurrent Port 6/7	I-3,3	-	-
A39	USB4-	USB_PN4 | USB Data - Port4	DP	-	int. PD 15k in ICH7
A40	USB4+	USB_PP4 | USB Data + Port4	DP	-	int. PD 15k in ICH7
A41	GND	Power Ground	PWR	-	-
A42	USB2-	USB_PN2 | USB Data - Port2	DP	-	int. PD 15k in ICH7
A43	USB2+	USB_PP2 | USB Data + Port2	DP	-	int. PD 15k in ICH7
A44	USB_2_3_OC#	USB_OC#_2_3 | USB OverCurrent Port 2/3	I-3,3	PU 10k 3,3V	-
A45	USB0-	USB_PN0 | USB Data - Port0	DP	-	int. PD 15k in ICH7
A46	USB0+	USB_PP0 | USB Data + Port0	DP	-	int. PD 15k in ICH7
A47	VCC_RTC	+V_BAT	PWR	-	-
A48	EXCD0_PERST#	Express Card Support [0]|card reset	O-3,3	-	-
A49	EXCD0_CPPE#	Express Card Support [0]| capable c. request	I-3,3	-	-
A50	LPC_SERIRQ	INT_SERIRQ | Serial Interrupt Request	IO-3,3	PU 8k2 3,3V	-
A51	GND	Power Ground	PWR	-	-
A52	PCIE_TX5+	n.c.	Nc	-	-
A53	PCIE_TX5-	n.c.	Nc	-	-
A54	GPI0	GPI0 | General Purpose Input 0	I-3,3	PU 10k 3,3V	-
A55	PCIE_TX4+	PCI Express lane 4 + Transmit	O	-	-

Note: The termination resistors in this table are already mounted on the COM Express® board. Refer to the design guide for information about additional termination resistors.

Connector X1A (Signal Levels A56-A110)

Pin A56-A110 [Power | LVDS | PCIe]

Pin	Signal	Description	Type	Termination	Comment
A56	PCIE_TX4-	PCI Express lane 4 -	O	-	-
A57	GND	Power Ground	PWR	-	-
A58	PCIE_TX3+	PCI Express lane 3 +	O	-	-
A59	PCIE_TX3-	PCI Express lane 3 -	O	-	-
A60	GND	Power Ground	PWR	-	-
A61	PCIE_TX2+	PCI Express lane 2 +	O	-	-
A62	PCIE_TX2-	PCI Express lane 2 -	O	-	-
A63	GPI1	GPI1 | General Purpose Input 1	I-3,3	PU 10k 3,3V	-
A64	PCIE_TX1+	PCI Express lane 1 +	O	-	-
A65	PCIE_TX1-	PCI Express lane 1 -	O	-	-
A66	GND	Power Ground	PWR	-	-
A67	GPI2	GPI2 | General Purpose Input 2	I-3,3	PU 10k 3,3V	-
A68	PCIE_TX0+	PCI Express lane 0 +	O	-	-
A69	PCIE_TX0-	PCI Express lane 0 -	O	-	-
A70	GND	Power Ground	PWR	-	-
A71	LVDS_A0+	LVDS_YAP0 | LVDS Channel A Data0+	O	-	-
A72	LVDS_A0-	LVDS_YAM0 | LVDS Channel A Data0-	O	-	-
A73	LVDS_A1+	LVDS_YAP1 | LVDS Channel A Data1+	O	-	-
A74	LVDS_A1-	LVDS_YAM1 | LVDS Channel A Data1-	O	-	-
A75	LVDS_A2+	LVDS_YAP2 | LVDS Channel A Data2+	O	-	-
A76	LVDS_A2-	LVDS_YAM2 | LVDS Channel A Data2 -	O	-	-
A77	LVDS_VDD_EN	LVDS_VDDEN | LVDS Panel Power Control	O-2,5	-	-
A78	LVDS_A3+	LVDS_YAP3 | LVDS Channel A Data3+	O	-	-
A79	LVDS_A3-	LVDS_YAM3 | LVDS Channel A Data3-	O	-	-
A80	GND	Power Ground	PWR	-	-
A81	LVDS_A_CK+	LVDS_CLKAP | LVDS Channel A Clock+	O	-	-
A82	LVDS_A_CK-	LVDS_CLKAM | LVDS Channel A Clock-	O	-	-
A83	LVDS_I2C_CK	LVDS_DDCPCLK | JILI I2C Clock	IO-3,3	PU 4k7 3,3V	-
A84	LVDS_I2C_DAT	LVDS_DDCPDATA | JILI I2C Data	IO-3,3	PU 4k7 3,3V	-
A85	GPI3	GPI3 | General Purpose Input 3	I-3,3	PU 10k 3,3V	-
A86	KBD_RST#	H_RCIN# | Keyboard Reset	I-3,3	PU 10k 3,3V	-
A87	KBD_A20GATE	H_A20GATE	I-3,3	PU 10k 3,3V	-
A88	PCIE0_CK_REF+	CLK_PCIE_REF P	O	-	-
A89	PCIE0_CK_REF-	CLK_PCIE_REF P	O	-	-
A90	GND	Power Ground	PWR	-	-
A91	RSVD	n.c.	Nc	-	-
A92	RSVD	n.c.	Nc	-	-
A93	GPO0	GPO0 | General Purpose Output 0	O-3,3	PD 10k	-
A94	RSVD	n.c.	Nc	-	-
A95	RSVD	n.c.	Nc	-	
A96	GND	Power Ground	PWR	-	-
A97	VCC_12V	12V VCC	PWR	-	-
A98	VCC_12V	12V VCC	PWR	-	-
A99	VCC_12V	12V VCC	PWR	-	-
A100	GND	Power Ground	PWR	-	-
A101	VCC_12V	12V VCC	PWR	-	-
A102	VCC_12V	12V VCC	PWR	-	-
A103	VCC_12V	12V VCC	PWR	-	-
A104	VCC_12V	12V VCC	PWR	-	-
A105	VCC_12V	12V VCC	PWR	-	-
A106	VCC_12V	12V VCC	PWR	-	-
A107	VCC_12V	12V VCC	PWR	-	-
A108	VCC_12V	12V VCC	PWR	-	-
A109	VCC_12V	12V VCC	PWR	-	-
A110	GND	Power Ground	PWR	-	-

Note: The termination resistors in this table are already mounted on the COM Express® board. Refer to the design guide for information about additional termination resistors.

Connector X1B (Signal Levels B1-B55)

Pin B1-B55 [LAN | Power | USB | SATA | PCIe | AUDIO | LPC]

Pin	Signal	Description	Type	Termination	Comment
B1	GND	Power Ground	PWR	-	-
B2	GBE0_ACT	LAN_ACTLED# | Ethernet Activity LED	O-3,3	-	-
B3	LPC_FRAME#	LPC_FRAME# | LPC Frame Indicator	I-3,3	-	-
B4	LPC_AD0	LPC_AD0 | LPC Adress & DATA Bus	IO-3,3	-	-
B5	LPC_AD1	LPC_AD1 | LPC Adress & DATA Bus	IO-3,3	-	-
B6	LPC_AD2	LPC_AD2 | LPC Adress & DATA Bus	IO-3,3	-	-
B7	LPC_AD3	LPC_AD3 | LPC Adress & DATA Bus	IO-3,3	-	-
B8	LPC_DRQ0#	SIO_DRQ#0 | LPC Request 0	I-3,3	-	-
B9	LPC_DRQ1#	SIO_DRQ#1 | LPC Request 1	I-3,3	-	-
B10	LPC_CLK	CLK_SIOEXTPCI	O-3,3	-	-
B11	GND	Power Ground	PWR	-	-
B12	PWRBTN#	Power Button	I-5	-	-
B13	SMB_CK	SMB_CLK | SMBUS Clock	O-3,3	PU 2k2 3,3V	-
B14	SMB_DAT	SMB_DATA | SMBUS Data	IO-3,3	PU 2k2 3,3V	-
B15	SMB_ALERT#	SMB_ALERT#	IO-3,3	PU 2k2 3,3V	-
B16	SATA1_TX+	SATA1_TX+	O	-	-
B17	SATA1_TX-	SATA1_TX-	O	-	-
B18	SUS_STAT#	PM_SUS_ STAT#	O-3,3	-	-
B19	SATA1_RX+	SATA1_RX+	I	-	-
B20	SATA1_RX-	SATA1_RX-	I	-	-
B21	GND	Power Ground	PWR	-	-
B22	SATA3_TX+	SATA3_TX+	O	-	-
B23	SATA3_TX-	SATA3_TX-	O	-	-
B24	PWR_OK	ETX_PWR_OK | Power OK	I-3,3	-	-
B25	SATA3_RX+	SATA3_RX+	I	-	-
B26	SATA3_RX-	SATA3_RX-	I	-	-
B27	WDT	Watch Dog Timer	O-3,3	-	-
B28	AC_SDIN2	AC_SDATAIN2 | AC'97 Serial Input Data 2	I-3,3	-	int. PD 20k in ICH7
B29	AC_SDIN1	AC_SDATAIN1 | AC'97 Serial Input Data 1	I-3,3	-	int. PD 20k in ICH7
B30	AC_SDIN0	AC_SDATAIN0 | AC'97 Serial Input Data 0	I-3,3	-	int. PD 20k in ICH7
B31	GND	Power Ground	PWR	-	-
B32	SPKR	AC_SPKR | Speaker	O-3,3	-	int. PD 20k in ICH7
B33	I2C_CK	I2CLK	O-3,3	PU 2k2 3,3V	-
B34	I2C_DAT	I2DAT	IO-3,3	PU 2k2 3,3V	-
B35	THRM#	PM THRM# CON | Over Temperature	O-3,3	PU 10k 3,3V	-
B36	USB7-	USB_PN7 | USB Data – Port7	DP	-	int. PD 15k in ICH7
B37	USB7+	USB_PP7 | USB Data + Port7	DP	-	int. PD 15k in ICH7
B38	USB_4_5_OC#	USB_OC#_4_5 | USB OverCurrent Port 4/5	I-3.3	PU 10k 3,3V	-
B39	USB5-	USB_PN5 | USB Data- Port5	DP	-	int. PD 15k in ICH7
B40	USB5+	USB_PP5 | USB Data+ Port5	DP	-	int. PD 15k in ICH7
B41	GND	Power Ground	PWR	-	-
B42	USB3-	USB_PN3 | USB Data- Port3	DP	-	int. PD 15k in ICH7
B43	USB3+	USB_PP3 | USB Data+ Port3	DP	-	int. PD 15k in ICH7
B44	USB_0_1_OC#	USB_OC#_0_1 | USB OverCurrent Port 0/1	I-3.3	PU 10k 3,3V	-
B45	USB1-	USB_PN1 | USB Data- Port1	DP	-	int. PD 15k in ICH7
B46	USB1+	USB_PP1 | USB Data+ Port1	DP	-	int. PD 15k in ICH7
B47	EXCD1_PERST#	Express Card Support [1]|card reset	O-3,3	-	-
B48	EXCD1_CPPE#	Express Card Support [1]| capable c.	I-3,3	-	-
B49	SYS_RESET#	ETX_SYS_RESET# | Reset Input	I-3,3	PU 10k 3,3V	-
B50	CB_RESET#	PCI_RST# | PCI Bus Reset	O-3,3	-	-
B51	GND	Power Ground	PWR	-	-
B52	PCIE_RX5+	n.c.	Nc	-	-
B53	PCIE_RX5-	n.c.	Nc	-	-
B54	GPO1	GPO1 | General Purpose Output 1	O-3,3	PD 10k	-
B55	PCIE_RX4+	PCI Express lane 4 + Recieve	I	-	availlable when ICH7-MDH or

Note: The termination resistors in this table are already mounted on the COM Express® board. Refer to the design guide for information about additional termination resistors.

Connector X1A (Signal Levels B56-B110)

Pin B56-B110 [Power | PCIe | LVDS | TV]

Pin	Signal	Description	Type	Termination	Comment
B56	PCIE_RX4-	PCI Express lane 4 - Recieve	I	-	availlable when ICH7-MDH or
B57	GPO2	GPO2 | General Purpose Output 2	O-3,3	PD 10k	
B58	PCIE_RX3+	PCI Express lane 3 + Recieve	I	-	availlable when ICH7-MDH or
B59	PCIE_RX3-	PCI Express lane 3 - Recieve	I	-	availlable when ICH7-MDH or
B60	GND	Power Ground	PWR	-	-
B61	PCIE_RX2+	PCI Express lane 2 + Recieve	I	-	-
B62	PCIE_RX2-	PCI Express lane 2 - Recieve	I	-	-
B63	GPO3	GPO3 | General Purpose Output 3	O-3,3	PD 10k	-
B64	PCIE_RX1+	PCI Express lane 1 + Recieve	I	-	-
B65	PCIE_RX1-	PCI Express lane 1 - Recieve	I	-	-
B66	WAKE0#	PCIE_WAKEI#	IO-3,3	PU 1k 3,3V	-
B67	WAKE1#	WAKE1#	I-3,3	PU 8k2 3,3V	-
B68	PCIE_RX0+	PCI Express lane 0 + Recieve	I	-	-
B69	PCIE_RX0-	PCI Express lane 0 - Recieve	I	-	-
B70	GND	Power Ground	PWR	-	-
B71	LVDS_B0+	LVDS_YBP0 | LVDS Channel B Data0+	O	-	-
B72	LVDS_B0-	LVDS_YBM0 | LVDS Channel B Data0-	O	-	-
B73	LVDS_B1+	LVDS_YBP1 | LVDS Channel B Data1+	O	-	-
B74	LVDS_B1-	LVDS_YBM1 | LVDS Channel B Data1-	O	-	-
B75	LVDS_B2+	LVDS_YBP2 | LVDS Channel B Data2+	O	-	-
B76	LVDS_B2-	LVDS_YBM2 | LVDS Channel B Data2 -	O	-	-
B77	LVDS_B3+	LVDS_YBP2 | LVDS Channel B Data3+	O	-	-
B78	LVDS_B3-	LVDS_YBM2 | LVDS Channel B Data3 -	O	-	-
B79	LVDS_BKLT_EN	BLON# | Panel Backlight ON	O-3,3	-	-
B80	GND	Power Ground	PWR	-	-
B81	LVDS_B_CK+	LVDS_CLKBP | LVDS Channel B Clock+	O	-	-
B82	LVDS_B_CK-	LVDS_CLKBM | LVDS Channel B Clock-	O	-	-
B83	LVDS_BKLT_CTRL	LVDS BKLTCTL | Backlight Brightness Contr.	O-3,3	-	-
B84	VCC_5V_SBY	+V_STBY_ETX | 5V Standby	PWR	-	-
B85	VCC_5V_SBY	+V_STBY_ETX | 5V Standby	PWR	-	-
B86	VCC_5V_SBY	+V_STBY_ETX | 5V Standby	PWR	-	-
B87	VCC_5V_SBY	+V_STBY_ETX | 5V Standby	PWR	-	-
B88	RSVD	n.c.	nc	-	-
B89	VGA_RED	CRT_RED | Analog Video RGB-RED	O	-	-
B90	GND	Power Ground	PWR	-	-
B91	VGA_GRN	CRT_GREEN | Analog Video RGB-GREEN	O	-	-
B92	VGA_BLU	CRT_BLUE | Analog Video RGB-BLUE	O	-	-
B93	VGA_HSYNC	CRT_HSYNC | Analog Video H-Sync	O-3,3	-	-
B94	VGA_VSYNC	CRT_VSYNC | Analog Video V-Sync	O-3,3	-	-
B95	VGA_I2C_CK	CRT_DDCACLK | Display Data Channel Clock	IO-5	PU 4k7 5V	-
B96	VGA_I2C_DAT	CRT_DDCADATA | Display Data Channel Data	IO-5	PU 4k7 5V	-
B97	TV_DAC_A	TV_DACA_CVBS | Composite CVBS	OA	-	-
B98	TV_DAC_B	TV_DADB_Y | TV Luminance Signal	OA	-	-
B99	TV_DAC_C	TV_DADC_C | TV Chrominance Signal	OA	-	-
B100	GND	Power Ground	PWR	-	-
B101	VCC_12V	12V VCC	PWR	-	-
B102	VCC_12V	12V VCC	PWR	-	-
B103	VCC_12V	12V VCC	PWR	-	-
B104	VCC_12V	12V VCC	PWR	-	-
B105	VCC_12V	12V VCC	PWR	-	-
B106	VCC_12V	12V VCC	PWR	-	-
B107	VCC_12V	12V VCC	PWR	-	-
B108	VCC_12V	12V VCC	PWR	-	-
B109	VCC_12V	12V VCC	PWR	-	-
B110	GND	Power Ground	PWR	-	-

Note: The termination resistors in this table are already mounted on the COM Express® board. Refer to the design guide for information about additional termination resistors.

4.2.2 Connector X1B

Connector X1B (Signal Levels C1-C55)

Pin A1-A55 [LAN | Power | USB | SATA | PCIe | AUDIO]

Pin	Signal	Description	Type	Termination	Comment
C1	GND	Power Ground	PWR	-	-
C2	IDE_D7	IDE Data Bus	IO	-	-
C3	IDE_D6	IDE Data Bus	IO	-	-
C4	IDE_D3	IDE Data Bus	IO	-	-
C5	IDE_D15	IDE Data Bus	IO	-	-
C6	IDE_D8	IDE Data Bus	IO	-	-
C7	IDE_D9	IDE Data Bus	IO	-	-
C8	IDE_D2	IDE Data Bus	IO	-	-
C9	IDE_D13	IDE Data Bus	IO	-	-
C10	IDE_D1	IDE Data Bus	IO	-	-
C11	GND	Power Ground	PWR	-	-
C12	IDE_D14	IDE Data Bus	IO	-	-
C13	IDE_IORDY	IDE Ready	I-3,3	PU 8k2 3,3V	-
C14	IDE_IOR#	IDE IO Read	O-3,3	-	-
C15	PCI_PME#	PCI Power Management Event	IO-3,3	-	-
C16	PCI_GNT2#	PCI Bus Grant 2	O-3,3	-	-
C17	PCI_REQ2#	PCI Bus Request 2	I-3,3	PU 8k2 3,3V	-
C18	PCI_GNT1#	PCI Bus Grant 1	O-3,3		-
C19	PCI_REQ1#	PCI Bus Request 1	I-3,3	PU 8k2 3,3V	-
C20	PCI_GNT0#	PCI Bus Grant 0	O-3,3		-
C21	GND	Power Ground	PWR	-	-
C22	PCI_REQ0#	PCI Bus Reqest 0	I-3,3	PU 8k2 3,3V	-
C23	PCI_RESET#	PCI Bus Reset	O-3,3	-	-
C24	PCI_AD0	PCI Adress & Data Bus line	IO-3,3	-	-
C25	PCI_AD2	PCI Adress & Data Bus line	IO-3,3	-	-
C26	PCI_AD4	PCI Adress & Data Bus line	IO-3,3	-	-
C27	PCI_AD6	PCI Adress & Data Bus line	IO-3,3	-	-
C28	PCI_AD8	PCI Adress & Data Bus line	IO-3,3	-	-
C29	PCI_AD10	PCI Adress & Data Bus line	IO-3,3	-	-
C30	PCI_AD12	PCI Adress & Data Bus line	IO-3,3	-	-
C31	GND	Power Ground	PWR	-	-
C32	PCI_AD14	PCI Adress & Data Bus line	IO-3,3	-	-
C33	PCI_C/BE1#	PCI Bus Command and Byte enables 1	IO-3,3	-	-
C34	PCI_PERR#	PCI Bus Grant Error	IO-3,3	PU 8k2 3,3V	-
C35	PCI_LOCK#	PCI Bus Lock	IO-3,3	PU 8k2 3,3V	-
C36	PCI_DEVSEL#	PCI Bus Device Select	IO-3,3	PU 8k2 3,3V	-
C37	PCI_IRDY#	PCI Bus Bus Initiator Ready	IO-3,3	PU 8k2 3,3V	-
C38	PCI_C/BE2#	PCI Bus Command and Byte enables 2	IO-3,3	-	-
C39	PCI_AD17	PCI Adress & Data Bus line	IO-3,3	-	-
C40	PCI_AD19	PCI Adress & Data Bus line	IO-3,3	-	-
C41	GND	Power Ground	PWR	-	-
C42	PCI_AD21	PCI Adress & Data Bus line	IO-3,3	-	-
C43	PCI_AD23	PCI Adress & Data Bus line	IO-3,3	-	-
C44	PCI_C/BE3#	PCI Bus Command and Byte enables 3	IO-3,3	-	-
C45	PCI_AD25	PCI Adress & Data Bus line	IO-3,3	-	-
C46	PCI_AD27	PCI Adress & Data Bus line	IO-3,3	-	-
C47	PCI_AD29	PCI Adress & Data Bus line	IO-3,3	-	-
C48	PCI_AD31	PCI Adress & Data Bus line	IO-3,3	-	-
C49	PCI_IRQA#	PCI Bus Interrupt Request A	I-3,3	PU 8k2 3,3V	-
C50	PCI_IRQB#	PCI Bus Interrupt Request B	I-3,3	PU 8k2 3,3V	-
C51	GND	Power Ground	PWR	-	-
C52	PEG_RX0+	PCIexpress Graphics Recieve + (0)	I	-	-
C53	PEG_RX0-	PCIexpress Graphics Recieve - (0)	I	-	-
C54	TYPE0#	n.c.	nc	-	-
C55	PEG_RX1+	PCIexpress Graphics Recieve + (1)	I	-	-

Note: The termination resistors in this table are already mounted on the COM Express® board. Refer to the design guide for information about additional termination resistors.

Connector X1B (Signal Levels C56-C110)

Pin C56-C110 [Power | LVDS | PCIe]

Pin	Signal	Description	Type	Termination	Comment
C56	PEG_RX1-	PCIexpress Graphics Recieve - (1)	I	-	-
C57	TYPE1#	n.c.	nc	-	-
C58	PEG_RX2+	PCIexpress Graphics Recieve + (2)	I	-	-
C59	PEG_RX2-	PCIexpress Graphics Recieve - (2)	I	-	-
C60	GND	Power Ground	PWR	-	-
C61	PEG_RX3+	PCIexpress Graphics Recieve + (3)	I	-	-
C62	PEG_RX3-	PCIexpress Graphics Recieve - (3)	I	-	-
C63	RSVD	n.c.	nc	-	-
C64	RSVD	n.c.	nc	-	-
C65	PEG_RX4+	PCIexpress Graphics Recieve + (4)	I	-	-
C66	PEG_RX4-	PCIexpress Graphics Recieve - (4)	I	-	-
C67	RSVD	n.c.	nc	-	-
C68	PEG_RX5+	PCIexpress Graphics Recieve + (5)	I	-	-
C69	PEG_RX5-	PCIexpress Graphics Recieve - (5)	I	-	-
C70	GND	Power Ground	PWR	-	-
C71	PEG_RX6+	PCIexpress Graphics Recieve + (6)	I	-	-
C72	PEG_RX6-	PCIexpress Graphics Recieve - (6)	I	-	-
C73	SDVO_DATA	SDVO_CTRLDATA	IO-2,5	PU 5k6 2,5V	-
C74	PEG_RX7+	PCIexpress Graphics Recieve + (7)	I	-	-
C75	PEG_RX7-	PCIexpress Graphics Recieve - (7)	I	-	-
C76	GND	Power Ground	PWR	-	-
C77	RSVD	n.c.	nc	-	-
C78	PEG_RX8+	PCIexpress Graphics Recieve + (8)	I	-	-
C79	PEG_RX8-	PCIexpress Graphics Recieve - (8)	I	-	-
C80	GND	Power Ground	PWR	-	-
C81	PEG_RX9+	PCIexpress Graphics Recieve + (9)	I	-	-
C82	PEG_RX9-	PCIexpress Graphics Recieve - (9)	I	-	-
C83	RSVD	n.c.	nc	-	-
C84	GND	Power Ground	PWR	-	-
C85	PEG_RX10+	PCIexpress Graphics Recieve + (10)	I	-	-
C86	PEG_RX10-	PCIexpress Graphics Recieve - (10)	I	-	-
C87	GND	Power Ground	PWR	-	-
C88	PEG_RX11+	PCIexpress Graphics Recieve + (11)	I	-	-
C89	PEG_RX11-	PCIexpress Graphics Recieve – (11)	I	-	-
C90	GND	Power Ground	PWR	-	-
C91	PEG_RX12+	PCIexpress Graphics Recieve + (12)	I	-	-
C92	PEG_RX12-	PCIexpress Graphics Recieve - (12)	I	-	-
C93	GND	Power Ground	PWR	-	-
C94	PEG_RX13+	PCIexpress Graphics Recieve + (13)	I	-	-
C95	PEG_RX13-	PCIexpress Graphics Recieve - (13)	I	-	-
C96	GND	Power Ground	PWR	-	-
C97	RSVD	n.c.	nc	-	-
C98	PEG_RX14+	PCIexpress Graphics Recieve + (14)	I	-	-
C99	PEG_RX14-	PCIexpress Graphics Recieve - (14)	I	-	-
C100	GND	Power Ground	PWR	-	-
C101	PEG_RX15+	PCIexpress Graphics Recieve + (15)	I	-	-
C102	PEG_RX15-	PCIexpress Graphics Recieve - (15)	I	-	-
C103	GND	Power Ground	PWR	-	-
C104	VCC_12V	12V VCC	PWR	-	-
C105	VCC_12V	12V VCC	PWR	-	-
C106	VCC_12V	12V VCC	PWR	-	-
C107	VCC_12V	12V VCC	PWR	-	-
C108	VCC_12V	12V VCC	PWR	-	-
C109	VCC_12V	12V VCC	PWR	-	-
C110	GND	Power Ground	PWR	-	-

Note: The termination resistors in this table are already mounted on the COM Express® board. Refer to the design guide for information about additional termination resistors.

Connector X1B (Signal Levels D1-D55)

Pin D1-D55 [LAN | Power | USB | SATA | PCIe | AUDIO | LPC]

Pin	Signal	Description	Type	Termination	Comment
D1	GND	Power Ground	PWR	-	-
D2	IDE_D5	IDE Data Bus	IO	-	-
D3	IDE_D10	IDE Data Bus	IO	-	-
D4	IDE_D11	IDE Data Bus	IO	-	-
D5	IDE_D12	IDE Data Bus	IO	-	-
D6	IDE_D4	IDE Data Bus	IO	-	-
D7	IDE_D0	IDE Data Bus	IO	-	-
D8	IDE_REQ	IDE Data Bus	IO	-	-
D9	IDE_IOW#	IDE IO Write	O-3,3	-	-
D10	IDE_ACK#	IDE DMA Acknowledge	O-3,3	-	-
D11	GND	Power Ground	PWR	-	-
D12	IDE_IRQ	IDE Interrupt Request	I-3,3	PU 8k2 3,3V	-
D13	IDE_A0	IDE Adress Bus	O-3,3	-	-
D14	IDE_A1	IDE Adress Bus	O-3,3	-	-
D15	IDE_A2	IDE Adress Bus	O-3,3	-	-
D16	IDE_CS1#	IDE Chip Select Channel 0	O-3,3	-	-
D17	IDE_CS3#	IDE Chip Select Channel 1	O-3,3	-	-
D18	IDE_RESET#	IDE Hard Drive Reset	O-3,3	-	-
D19	PCI_GNT3#	PCI Bus Grant 3	O-3,3	-	-
D20	PCI_REQ3#	PCI Bus Reqest 0	I-3,3	PU 8k2 3,3V	-
D21	GND	Power Ground	PWR	-	-
D22	PCI_AD1	PCI Adress & Data Bus line	IO-3,3	-	-
D23	PCI_AD3	PCI Adress & Data Bus line	IO-3,3	-	-
D24	PCI_AD5	PCI Adress & Data Bus line	IO-3,3	-	-
D25	PCI_AD7	PCI Adress & Data Bus line	IO-3,3	-	-
D26	PCI_C/BE0#	PCI Bus Command and Byte enables 0	IO-3,3	-	-
D27	PCI_AD9	PCI Adress & Data Bus line	IO-3,3	-	-
D28	PCI_AD11	PCI Adress & Data Bus line	IO-3,3	-	-
D29	PCI_AD13	PCI Adress & Data Bus line	IO-3,3	-	-
D30	PCI_AD15	PCI Adress & Data Bus line	IO-3,3	-	-
D31	GND	Power Ground	PWR	-	-
D32	PCI_PAR	PCI Bus Parity	IO-3,3	-	-
D33	PCI_SERR#	PCI Bus System Error	IO-3,3	PU 8k2 3,3V	-
D34	PCI_STOP#	PCI Bus Stop	IO-3,3	PU 8k2 3,3V	-
D35	PCI_TRDY#	PCI Bus Target Ready	IO-3,3	PU 8k2 3,3V	-
D36	PCI_FRAME#	PCI Bus Cycle Frame	IO-3,3	PU 8k2 3,3V	-
D37	PCI_AD16	PCI Adress & Data Bus line	IO-3,3	-	-
D38	PCI_AD18	PCI Adress & Data Bus line	IO-3,3	-	-
D39	PCI_AD20	PCI Adress & Data Bus line	IO-3,3	-	-
D40	PCI_AD22	PCI Adress & Data Bus line	IO-3,3	-	-
D41	GND	Power Ground	PWR	-	-
D42	PCI_AD24	PCI Adress & Data Bus line	IO-3,3	-	-
D43	PCI_AD26	PCI Adress & Data Bus line	IO-3,3	-	-
D44	PCI_AD28	PCI Adress & Data Bus line	IO-3,3	-	-
D45	PCI_AD30	PCI Adress & Data Bus line	IO-3,3	-	-
D46	PCI_IRQC#	PCI Bus Interrupt Request C	I-3,3	PU 8k2 3,3V	-
D47	PCI_IRQD#	PCI Bus Interrupt Request D	I-3,3	PU 8k2 3,3V	-
D48	PCI_CLKRUN#	PCI Clock Run	I-3,3	PU 10k 3,3V	-
D49	PCI_M66EN	n.c.	nc	-	-
D50	PCI_CLK	PCI Clock	O-3,3	-	-
D51	GND	Power Ground	PWR	-	-
D52	PEG_TX0+	PCIexpress Graphics Transmit + (0)	I	-	DVOBD8
D53	PEG_TX0-	PCIexpress Graphics Transmit - (0)	I	-	DVOBD9
D54	PEG_LANE_RV#	PCIexpress Graphics Lane Reversal	I	-	-
D55	PEG_TX1+	PCIexpress Graphics Transmit + (1)	I	-	-

Note: The termination resistors in this table are already mounted on the COM Express® board. Refer to the design guide for information about additional termination resistors.

Connector X1B (Signal Levels D56-D110)

Pin D56-D110 [LAN | Power | USB | SATA | PCIe | AUDIO | LPC]

Pin	Signal	Description	Type	Termination	Comment
D56	PEG_TX1-	PCIexpress Graphics Transmit - (1)	I	-	-
D57	TYPE2#	n.c.	nc	-	-
D58	PEG_TX2+	PCIexpress Graphics Transmit + (2)	I	-	-
D59	PEG_TX2-	PCIexpress Graphics Transmit - (2)	I	-	-
D60	GND	Power Ground	PWR	-	-
D61	PEG_TX3+	PCIexpress Graphics Transmit + (3)	I	-	-
D62	PEG_TX3-	PCIexpress Graphics Transmit - (3)	I	-	-
D63	RSVD	-	nc	-	
D64	RSVD	-	nc	-	
D65	PEG_TX4+	PCIexpress Graphics Transmit + (4)	I	-	-
D66	PEG_TX4-	PCIexpress Graphics Transmit - (4)	I	-	-
D67	GND	Power Ground	PWR	-	-
D68	PEG_TX5+	PCIexpress Graphics Transmit + (5)	I	-	-
D69	PEG_TX5-	PCIexpress Graphics Transmit - (5)	I	-	-
D70	GND	Power Ground	PWR	-	-
D71	PEG_TX6+	PCIexpress Graphics Transmit + (6)	I	-	-
D72	PEG_TX6-	PCIexpress Graphics Transmit - (6)	I	-	-
D73	SDVO_CLK	SDVO_CTRLCLK	IO-2,5	PU 5k6 2,5V	-
D74	PEG_TX7+	PCIexpress Graphics Transmit + (7)	I	-	-
D75	PEG_TX7-	PCIexpress Graphics Transmit - (7)	I	-	-
D76	GND	Power Ground	PWR	-	-
D77	IDE_CBLID	IDE Primary ATA Detect	I-3,3	PD 10k	
D78	PEG_TX8+	PCIexpress Graphics Transmit + (8)	I	-	-
D79	PEG_TX8-	PCIexpress Graphics Transmit - (8)	I	-	-
D80	GND	Power Ground	PWR	-	-
D81	PEG_TX9+	PCIexpress Graphics Transmit + (9)	I	-	-
D82	PEG_TX9-	PCIexpress Graphics Transmit - (9)	I	-	-
D83	RSVD	n.c.	nc	-	-
D84	GND	Power Ground	PWR	-	-
D85	PEG_TX10+	PCIexpress Graphics Transmit + (10)	I	-	-
D86	PEG_TX10-	PCIexpress Graphics Transmit - (10)	I	-	-
D87	GND	Power Ground	PWR	-	-
D88	PEG_TX11+	PCIexpress Graphics Transmit + (11)	I	-	-
D89	PEG_TX11-	PCIexpress Graphics Transmit - (11)	I	-	-
D90	GND	Power Ground	PWR	-	-
D91	PEG_TX12+	PCIexpress Graphics Transmit + (12)	I	-	-
D92	PEG_TX12-	PCIexpress Graphics Transmit - (12)	I	-	-
D93	GND	Power Ground	PWR	-	-
D94	PEG_TX13+	PCIexpress Graphics Transmit + (13)	I	-	-
D95	PEG_TX13-	PCIexpress Graphics Transmit - (13)	I	-	-
D96	GND	Power Ground	PWR	-	-
D97	PEG_ENABLE#	PCIexpress Graphics Enable	I-3,3	PU 10k 3,3V	-
D98	PEG_TX14+	PCIexpress Graphics Transmit + (14)	nc	-	-
D99	PEG_TX14-	PCIexpress Graphics Transmit - (14)	nc	-	-
D100	GND	Power Ground	PWR	-	-
D101	PEG_TX15+	PCIexpress Graphics Transmit + (15)	I	-	-
D102	PEG_TX15-	PCIexpress Graphics Transmit - (15)	I	-	-
D103	GND	Power Ground	PWR	-	-
D104	VCC_12V	12V VCC	PWR	-	-
D105	VCC_12V	12V VCC	PWR	-	-
D106	VCC_12V	12V VCC	PWR	-	-
D107	VCC_12V	12V VCC	PWR	-	-
D108	VCC_12V	12V VCC	PWR	-	-
D109	VCC_12V	12V VCC	PWR	-	-
D110	GND	Power Ground	PWR	-	-

Note: The termination resistors in this table are already mounted on the COM Express® board. Refer to the design guide for information about additional termination resistors.

4.3 Signal description

4.3.1 PCIexpress x1 lanes

The PCI express x1 lanes is a fast connection interface for many different system devices, such as network controllers, I/O controllers or express card devices. The implementation of this subsystem complies with the COM Express® / COMexpress Specification. Implementation information is provided in the COM Express® Design Guide. Refer to the documentation for additional information.

4.3.2 USB

Eight USB host controllers (EHCI high-speed 2.0 controller) are on the Intel® 82801GB south bridge device. The USB controllers comply with both versions 1.1 and 2.0 of the USB standard and are backward compatible.

Configuration

The USB controllers are PCI bus devices. The BIOS allocates required system resources during configuration of the PCI bus.

4.3.3 SATA

The Intel® 82801GB south bridge device offers the possibility to connect 2 SATA Harddisks according SATA with 150 MB/s per channel or SATA II with 150 MB/s per channel in AHCI mode.

Configuration

The SATA controller is a PCI bus device. The BIOS allocates required system resources during configuration of the PCI bus.

4.3.4 Audio

The COMe-bCD2 PCI AC'97 audio controller is integrated in the Intel® 82801GB Southbridge.

Configuration

The audio controller is a PCI bus device. The BIOS allocates required system resources during configuration of the PCI device.

4.3.5 Serial IRQ

The serial IRQ pin offers a standardized interface to link interrupt request lines to a single wire.

Configuration

The serial IRQ machine is in "Continuous Mode"

4.3.6 VGA Output

➤ The COMe-bCD2 graphics subsystem is integrated in the Intel® 945GM/GME northbridge. It has the following features:

- 250MHz core render clock and 200 MHz core display clock at 1.05V core voltage
- Supports TV-out, LVDS, CRT and SDVO
- Dynamic Video Memory Technology (DVMT 3.0)
- 2D graphics engine
- 3D graphics engine
- 3D setup and render engine
- Zone rendering
- High quality performance texture engine
- Viewpoint transform and perspective divide
- Max. resolution CRT: QXGA 2048x1536
- Max. resolution LCD: UXGA 1600x1200 (4G colors)
- Bits/Pixels supported on LCD: 1x18 bit, 2x18 bit, 1x24 bit, 2x24 bit

Note: The 945GM/GME does not support 24 bit LVDS but emulates the missing 2 bits per color and most of the panels can be used with this limitation. SDVO supports full 24 bit.

Configuration

The graphics controller requires the following resources:

- An IRQ
- Several I/O addresses
- Memory-address blocks in high memory

The BIOS allocates the resources during AGP configuration. Many resources are set for compatibility with industry-standard settings.

4.3.7 LVDS Flat Panel Interface (JILI)

The user interface for flat panels is the JUMPtec Intelligent LVDS Interface (JILI). The implementation of this subsystem complies with the COM Express® Specification. Implementation information is provided in the COM Express® Design Guide. Refer to the documentation for additional information.

4.3.8 Digital Flat Panel Interface (JIDI)

The COMe-bCD2 does not support the JUMPtec Intelligent Digital Interface (JIDI).

4.3.9 Ethernet

The Ethernet interface is based on the Realtek RTL8111b/c Gigabit Ethernet PCIexpress controller. This PCIexpress controller is a fully integrated 10/100/1000BASE-TX LAN solution.

The Ethernet interface requires an external transformer. See the COM Express® Design Guide for suggestions on transformer selection.

Configuration

The Ethernet interface is a PCIexpress device. The BIOS setup automatically configures it during configuration of the PCI device.

Note: Implementation and limitation information is provided in the COM Express® Design Guide. Refer to the documentation for additional information.

4.3.10 Power Control

Power Good / Reset Input

The COMe-bCD2 provides an external input for a power-good signal or a manual- reset pushbutton. The implementation of this subsystem complies with the COM Express® Specification. Implementation information is provided in the COM Express® Design Guide. Refer to the documentation for additional information.

4.3.11 Power Management

ATX PS Control

The COMe-bCD2 can control the main power output of an ATX-style power supply. The implementation of this subsystem complies with the COM Express® Specification. Implementation information is provided in the COM Express® Design Guide. Refer to the documentation for additional information.

External SMI Interrupt

Contact Kontron Embedded Modules technical support for information on this feature.

4.3.12 Miscellaneous Circuits

Speaker

The implementation of the speaker output complies with the COM Express® Specification. Implementation information is provided in the COM Express® Design Guide. Refer to the documentation for additional information.

Battery

The implementation of the battery input complies with the COM Express® Specification. Implementation information is provided in the COM Express® Design Guide. Refer to the documentation for additional information.

In compliance with EN60950, there are at least two current-limiting devices (resistor and diode) between the battery and the consuming component.

I2C Bus

The I2C Bus is implemented by using general purpose I/O.

You also can access the I2C Bus via JUMPtec's Intelligent Device Architecture (JIDA) BIOS functions.

For additional information, refer to the COM Express® Design Guide, I2C application notes and JIDA specifications which are available at the Kontron Web site.

SM Bus

System Management (SM) bus signals are connected to the SM bus controller, which is located in the Intel 82801GB (ICH7) device. For more information about the SM bus, please see the System Management (SM) Bus section in the Appendix A: System Resources chapter.

LPC Bus

The Low Pin Count Interface signals are connected to the LPC Bus bridge, which is located in the Intel 82801GB (ICH7). The LPC low speed interface can be used for peripheral circuits such as an external Super I/O Controller, which typically combine legacy-device support into a single IC. The implementation of this subsystem complies with the COM Express® Specification. Implementation information is provided in the COM Express® Design Guide. Refer to the documentation for additional information.

4.3.13 PCIexpress Graphics

The PCI express Graphics interface allows the connection of high performace graphics chips on an high bandwidth interface.

The implementation of this subsystem complies with the COM Express® / COMexpress Specification. Implementation information is provided in the COM Express® Design Guide. Refer to the documentation for additional information.

4.3.14 PCI Bus

The implementation of this subsystem complies with the COM Express® / COMexpress Specification. Implementation information is provided in the COM Express® Design Guide. Refer to the documentation for additional information.

4.3.15 IDE Port

The IDE host adapter is capable of DMA-33/66/100 operation. The implementation of this subsystem complies with the COM Express® Specification. Implementation information is provided in the COM Express® Design Guide. Refer to those documents for additional information.

Configuration

The IDE host adapter is a PCI bus device. It is configured by the BIOS during PCI device configuration. You can disable it in setup. Resources used by the IDE host adapter are compatible with the PC/AT.

4.3.16 SDVO Output

The COMe-bCD2 Serial Digital Video Output port is integrated in the Intel® 945GM northbridge. It has the following features:

- Share it's pins with the PEG interface

- Serial Digital Video Out Port (DVOB & DVOC) support
- Two 12-bit channels
- The SDVO B/C ports can drive a variety of SDVO devices (TV-Out Encoders, TMDS and LVDS transmitters, etc.)

5 Special Features

5.1 Watchdog Timer

This feature is implemented in the Xilinx XC9536XL microcontroller. You can configure the Watchdog Timer (WDT) in BIOS setup to start after a set amount of time after power-on boot. The WDT can also be controlled by the JIDA32 Library API (Refer to Appendix F: JIDA Standard). The application software should strobe the WDT to prevent its timeout. Upon timeout, the WDT resets and restarts the system. This provides a way to recover from program crashes or lockups.

Configuration

You can program the timeout period for the watchdog timer in two ranges:

- 1-second increments from 1 to 255 seconds
- 1-minute increments from 1 to 255 minutes

Contact Kontron Embedded Modules technical support for information on programming and operating the WDT.

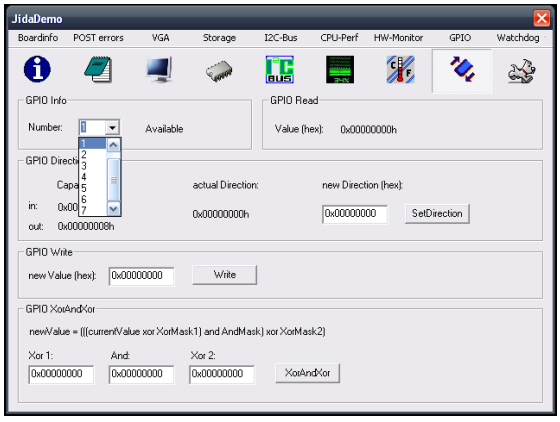
5.2 General Purpose Input and Output

COMe-bCD2 offers 4 General Purpose Input (GPI) pins and 4 General Purpose Output (GPO) pins. On a 3.3V level digital in- and outputs are available.

Signal	Pin	Description
GPI0	A54	General Purpose Input 0
GPI1	A63	General Purpose Input 1
GPI2	A67	General Purpose Input 2
GPI3	A85	General Purpose Input 3
GPO0	A93	General Purpose Output 0
GPO1	B54	General Purpose Output 1
GPO2	B57	General Purpose Output 2
GPO3	B63	General Purpose Output 3

Configuration

The GPI and GPO pins can be configured via JIDA32. Please refer to the JIDA32 manual in the driver download packet on our website.



6 Important Information

Kontron Embedded Modules currently offers different variants of the COMe-bCD2 with different processors: Intel® Celeron® M, or Core Duo® and Core2Duo® processor. These variants utilize a smart BIOS that is capable of identifying the CPU that the module is equipped with.

6.1 Cooling Solutions

With introduction of higher frequency CPUs into the embedded market the need to design more efficient cooling solutions is now a necessity. These higher frequency CPUs generate much more heat, which must be removed from the application. One solution that has become more common in the embedded market is the use of heat pipes when designing a cooling solution. Kontron Embedded Modules has designed some cooling solutions that utilize heat pipes in order to perform some tests. Although Kontron Embedded Modules designed these cooling solutions strictly for test purposes, and not as a standard COM Express® cooling solution, the knowledge gained from these tests is being made available to customers in the form of an application note called PM_Thermal_Guidelines_E1xx.pdf. This application note should be used as a guideline to help evaluate potential thermal designs. It can be found on Kontron's web site at www.kontron.com on the COM Express® product page and in the Tech Support section.

7 Design Considerations

7.1 Thermal Management

A heat-spreader plate assembly is available from Kontron Embedded Modules for the COMe-bCD2. The heat-spreader plate on top of this assembly is NOT a heat sink. It works as an ETXexpress®-standard thermal interface to use with a heat sink or other cooling device.

External cooling must be provided to maintain the heat-spreader plate at proper operating temperatures. Under worst-case conditions, the cooling mechanism must maintain an ambient air and heat-spreader plate temperature of 60° C or less.

The aluminum slugs and thermal pads on the underside of the heat-spreader assembly implement thermal interfaces between the heat spreader plate and the major heat-generating components on the COMe-bCD2. About 80 percent of the power dissipated within the module is conducted to the heat-spreader plate and can be removed by the cooling solution.

For 2166MHz modules, the heat dissipated into the plate ranges from 45 to 55 watts. Design a cooling solution to dissipate the heat load on a heat-spreader plate at a minimum of 55 watts to accommodate all COMe-bCD2 modules.

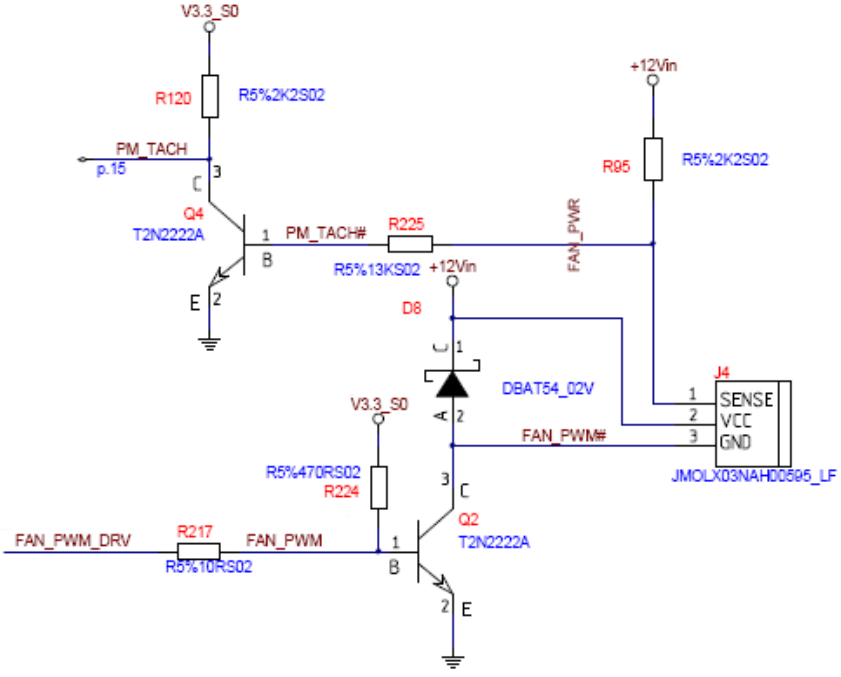
You can use many thermal-management solutions with the heat-spreader plates, including active and passive approaches. The optimum cooling solution varies, depending on the COM Express® application and environmental conditions. Please see the COM Express® Design Guide for further information on thermal management.

7.2 COMe-bCD2 onboard Fan connector

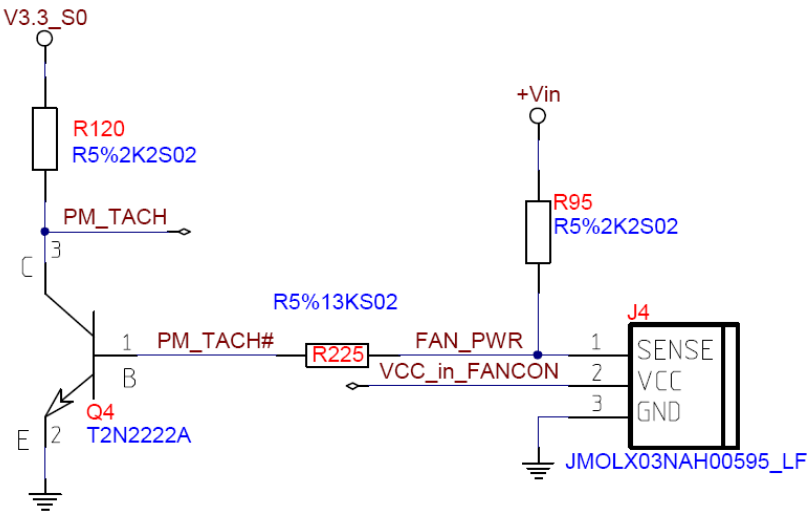
This section describes how to connect a fan to the connector located directly on the COMe-bCD2. With certain BIOS-settings it is possible to control the fan depending on the Active Trip Point temperature. The fan switches on/off depending on the adjusted Active Trip Point temperature. In order for this feature to function properly an ACPI compliant OS is necessary.

Note: The COM Express® CD BIOS supports continuous fan control in order to accommodate the CPU temperature characteristic curve.

Single channel version



Dual channel version

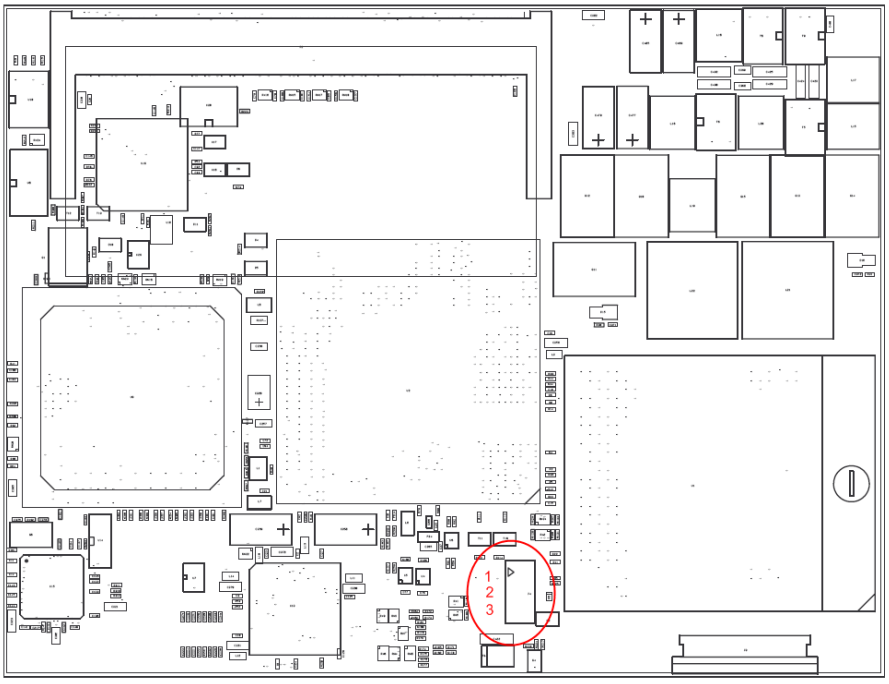


- Part number (Molex) J4: 53261-0390
- Mates with: 51021-0300
- Crimp terminals: 50079-8100

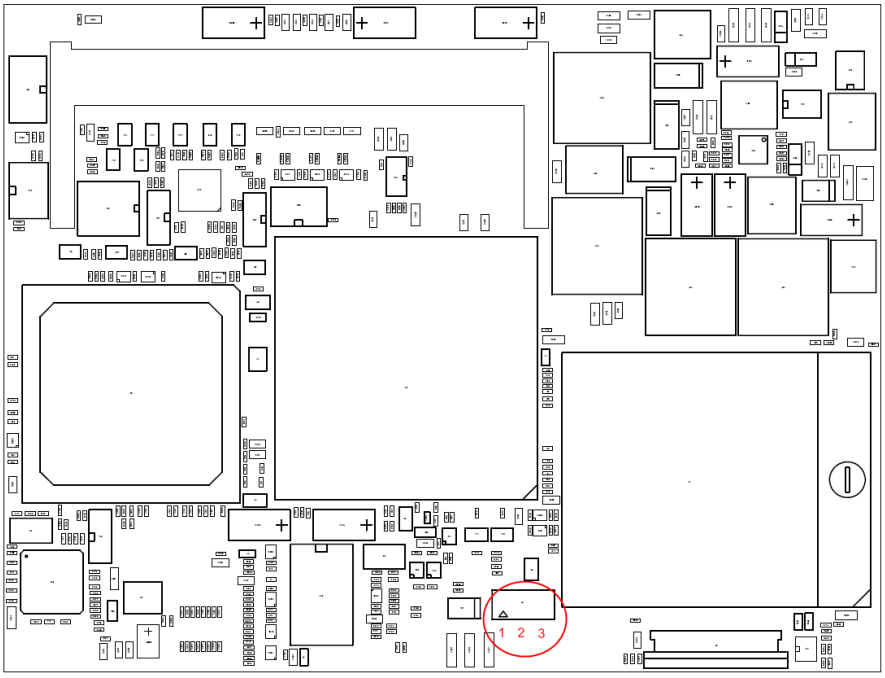
Warning: The VCC_in_FANCON is the output voltage, limited to 12V. Please be aware that in widerange input situations the fan speed depends on the used voltage level of the board supply and is limited to a maximum of 12V. (see 2.2.2)

7.2.1 Location and pinout of fan connector J4

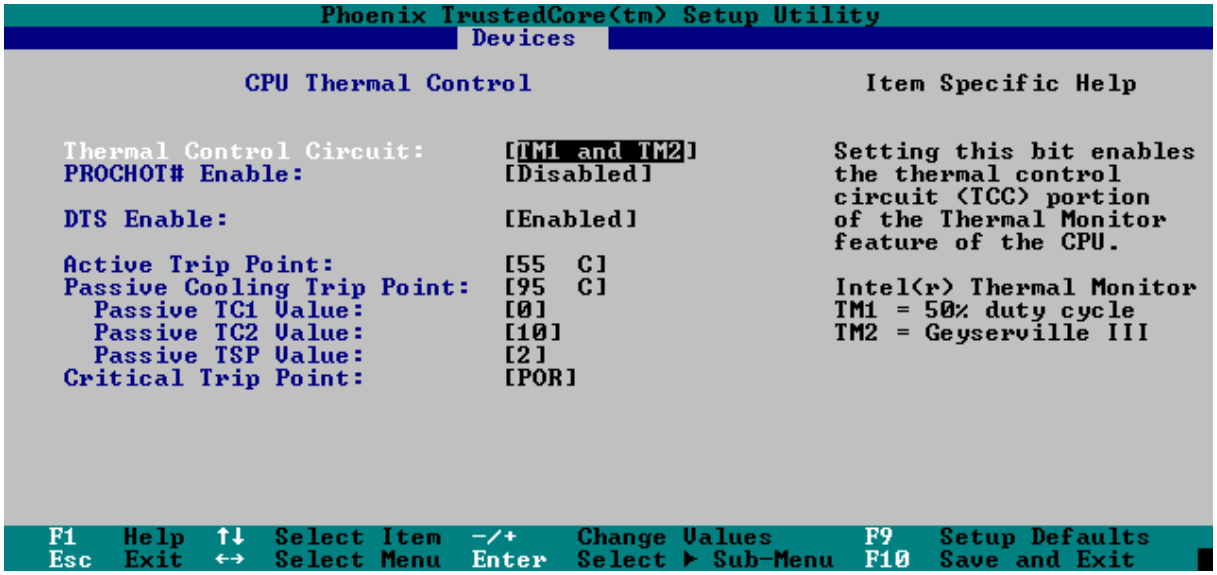
Single channel version (see 2.2.1)



Dual channel version (see 2.2.2)



7.2.2 BIOS settings for fan control



7.2.3 Electrical Characteristics

VCC_in_FANCON	=	VCC of board, limited to 12V
Imax	=	0,40 A

Note:	*The VCC_in_FANCON output is not short circuit proof. If necessary the user has to ensure that the circuit is protected externally, for example by a fuse on the backplane.*

8 Important Technology Information

The following technological information is designed to give the reader a better understanding of some of features of the COMe-bCD2. This information can be referenced when reading the Chapter System Resources and the Chapter BIOS Operation sections that follow. There are also references to additional documentation that will help to develop a better understanding of the technical information described herein.

8.1 I/O APIC mode

The I/O APIC (Advanced Programmable Interrupt Controller) handles interrupts differently then the 8259 PIC. The following information explains these differences.

8.1.1 Method of interrupts transmission

The I/O APIC transmits interrupts through the system bus and interrupts are handled without the needs for the processor to run an interrupt acknowledge cycle.

8.1.2 Interrupt priority

The priority of interrupts in the I/O APIC is independent of the interrupt number.

8.1.3 More interrupts

The I/O APIC in the chipset of the COMe-bCD2 supports a total of 24 interrupts.

The APIC is not supported by all operating systems. Only Windows Xp, Windows Vista and Linux supports APIC.

For more information see chapter 8 of the IA-32 Intel Architecture Software Developer's Manual, Volume 3.

8.2 Thermal Monitor and Catastrophic Thermal Protection

The Thermal Monitor within the Intel® processor helps to control the processor temperature by activating the TCC (Thermal Control Circuit) when the processor silicon reaches its maximum operating temperature. The temperature at which the Intel Thermal Monitor activates the TCC is not user-configurable and is not software visible.

The Thermal Monitor controls the processor temperature by modulating (starting and stopping) the CPU core clocks at a 50% duty cycle (TM1) or by initiating an Enhanced Intel SpeedStep technology transition (TM2) when the processor silicon reaches its maximum operating temperature (selectable in setup).

Note: TM2 is the recommended mode for the used Intel® processors.

Thermal Monitor supports two modes to activate the TCC: Automatic and On-Demand mode. The Intel Thermal Monitor Automatic Mode must be enabled via BIOS for the processor to be operating within specification.

Automatic mode does not require any additional hardware, software drivers, or interrupt handling routines.

Note: With a properly designed thermal solution, the TCC is only active for very short periods, hence processor performance impact is expected to be so minor that it would not be detectable.

The Intel® processor supports the THERMTRIP# signal for catastrophic thermal protection.

In the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached a temperature of approximately 125°C. At this point the system BUS signal THERMTRIP# will go active.

THERMTRIP# activation is independent of processor activity and does not generate any bus cycles.

8.2.1 Summary

Thermal Control Circuit reduces performance when the processor reaches its max. operating temperature (100°C). THERMTRIP# shuts down the system in case of catastrophic cooling failure.

8.3 Processor Performance Control

The Intel® processor can run in different performance states (multiple frequency/voltage operating points). The CPU performance can be altered while the computer is functioning. This allows the processor to run at different core frequencies and voltages depending on CPU thermal state and OS policy.

Windows XP includes built-in processor performance control to operate the processor more efficiently when it is not fully utilized. Win2k, WinME and Win9x do not support processor performance control. Special software is required for OSes not capable of processor performance control.

In Windows, the processor performance control policy is linked to the Power Scheme setting in the control panel power option applet.

Note: Windows always runs at the highest performance state when the "Home/Office" or "Always On" power scheme is selected.
For a more detailed information about processor performance control, see:
Chapter 8 of the ACPI Specification Revision 2.0c available at www.acpi.info Windows platform design note at: http://www.microsoft.com/whdc/hwdev/tech/onnow/procperfctrl.mspx

8.4 Thermal Management

ACPI allows the OS to play a role in the thermal management of the system. With the OS in control of the operating environment, cooling decisions can be made based on the application load on the CPU and the thermal heuristics of the system.

The ACPI thermal solution on COMe-bCD2 supports three cooling policies:

Active Cooling

The OS is turning the fan on/off. Active cooling devices typically consume power and produce noise, but are able to cool a thermal zone without limiting system performance. The active cooling trip point declares the temperature threshold the OS uses to decide when to start/stop active cooling devices.
Passive Cooling

The OS reduces the power consumption of the processor by throttling the processor clock to reduce the temperature of the thermal zone. Passive cooling devices (processor) produce no noise. The passive cooling trip point declares the temperature threshold where the OS will start or stop passive cooling.

Critical Trip Point

The OS performs an orderly, but critical, shutdown of the system when the temperature reaches the critical trip point.

9 System Ressources

9.1 Interrupt Request (IRQ) Lines

In 8259 PIC mode:

IRQ #	Used For	Available	Comment
0	Timer0	No	
1	Keyboard	No	
2	Slave 8259	No	
3	COM2	No	Note (2)
4	COM1	No	Note (2)
5	-	Yes	
6	Reserved for FDC	No	
7	LPT1	No	Note (2)
8	RTC	No	
9	SCI	No	
10	-	Yes	
11	-	Yes	
12	PS/2 Mouse	No	Note (2)
13	FPU	No	
14	IDE0	No	Note (1)
15	SATA	No	Note (3)

Note: *1 If the "Used For" device is disabled in setup, the corresponding interrupt is available for other devices.*
2 Unavailable if baseboard is equipped with an I/O controller Winbond W627, and the device is enabled in setup. Always available in legacy free BIOS versions.
3 Unavailable in SATA legacy mode. It cannot be used for PCI, but for ISA bus, when SATA is in enhanced mode.

In APIC mode:

IRQ #	Used For	Available	Available for PCI	Comment
0	Timer0	No	No	
1	Keyboard	No	No	
2	Slave 8259	No	No	
3	COM2	No	Yes	Note (2)
4	COM1	No	Yes	Note (2)
5	PCI	Yes	Yes	
6	Floppy Drive Controller	No	Yes	Note (2)
7	LPT1	No	Yes	Note (2)
8	RTC	No	No	
9	SCI	No	No	System Control Interrupt
10	-	Yes	Yes	
11	-	Yes	Yes	
12	PS/2 Mouse	No	Yes	Note (2)
13	FPU	No	No	
14	IDE0	No	No	
15	SATA	No	No	Note (3)
16	PIRQ[A]	For PCI		PCI IRQ line 1 + USB UHCI controller #3 + Graphics controller + PCIE Slot 0 + PCIE Slot 4
17	PIRQ[B]	For PCI		PCI IRQ line 2 + AC97 Audio controller + PCIe Slot 1 + PCIe Slot 5
18	PIRQ[C]	For PCI		PCI IRQ line 3 + USB UHCI controller #2 + Native IDE + PCIe Slot 2
19	PIRQ[D]	For PCI		PCI IRQ line 4 + USB UHCI controller #1 + SATA + SMBus + PCIe Slot 3
20	PIRQ[E]	No		
21	PIRQ[F]	No		
22	PIRQ[G]	No		
23	PIRQ[H]	No		USB UHCI Controller #0 + USB EHCI controller

Note: 1 If the "Used For" device is disabled in setup, the corresponding interrupt is available for other devices.
2 Unavailable if baseboard is equipped with an I/O controller Winbond W627, and the device is enabled in setup. Always available in legacy free versions of the BIOS.
3 Unavailable in SATA legacy mode. It cannot be used for PCI, but for ISA bus, when SATA is in enhanced mode.

9.2 Direct Memory Access (DMA) Channels

DMA #	Used for	Available	Comment
0		Yes	
1		Yes	
2		Yes	
3	LPT	Yes	Unavailable if LPT is used in ECP mode.
4	Cascade	No	
5		Yes	
6		Yes	
7		Yes	

9.3 Memory Area

Upper Memory	Used for	Available	Comment
C0000h – CFFFFh	VGA BIOS	No	
D0000h – DDFFFh		Yes	shadow RAM (ISA bus restriction)
DE000h – DFFFFh	USB registers	No	
E0000h – FFFFFh	System BIOS	No	

9.4 I/O Address Map

The I/O-port addresses of the COMe-bCD2 are functionally identical with a standard PC/AT.

The following I/O ports are additionally used:

I/O Address	Used for	Available	Comment
2e-2fh	Winbond external I/O controller	No	Available if external I/O controller not used.
4e-4fh	TPM	No	Available if TPM not populated.
2F8-2FFh	COM1	No	Available if device is disabled in setup
3F8-3FFh	COM2	No	Available if device is disabled in setup
1000h >	PCI	No	I/O ports 1000h and above might be allocated by PCI devices or onboard hardware.

9.5 Peripheeral Component Interconnect (PCI) Devices

PCI Device	Busmaster	PCI Interrupt	Comment
Audio, USB and Ethernet		See IRQ resource tables above	Integrated in the Intel chipset. No REQx/GNTx pair needed.

Note: You can use REQ0/GNT0, REQ1/GNT1, REQ2/GNT2, and REQ3/GNT3 pairs for external PCI devices.

9.6 Inter IC (I^2C) Bus

I2C Address	Used For	Available	Comment	JIDA-Bus-Nr.
A0h	JIDA-EEPROM	No	EEPROM for CMOS data.	0
A2h	JIDA-EEPROM	No		0
B0h	WD-PIC	No	Reserved for internal use.	0

9.7 System Managment (SM) Bus

Following SM bus addresses are reserved.

SM Bus Address	SM Device	Comment	JIDA-Bus-Nr.
10h	SMB Host	Do not use under any circumstances.	1
12h	SMART_CHARGER	Not to be used with any SM bus device except a charger	1
14h	SMART_SELECTOR	Not to be used with any SM bus device except a selector	1
16h	SMART_BATTERY	Not to be used with any SM bus device except a battery	1
30h	HW-Monitor	Can be used when there is no external SuperI/O	1
5Ch	HW-Monitor	Can be used when there is no external SuperI/O	1
A0h	SPD	SDRAM EEPROM	1
D2h	Clock generator	Do not use under any circumstances.	1
D4	Clockgenerator	Do not use under any circumstances	1

The standard COMe-bCD2 Power management BIOS supports the Smart Battery System M.A.R.S. If you require further information about this topic, please contact Kontron Embedded Modules GmbH Technical Support.

9.8 JILI I^2C Bus

I2C Address	Used For	Available	Comment	JIDA-Bus-Nr.
A0h	JILI-EEPROM	No	EEPROM for JILI-Data	2
62h	Brightness control	No	MAX536262	2

10 BIOS Operation

The module is equipped with a Phoenix BIOS, which is located in an onboard Flash EEPROM. The device has 8-bit access. Faster access (16 bit) is provided by the shadow RAM feature. You can update the BIOS using a Flash utility.

10.1 Determining the BIOS Version

To determine the PhoenixBIOS version, immediately press the Pause key on your keyboard as soon as you see the following text display in the upper left corner of your screen:

PhoenixBIOS 4.0 Release 6.1

Copyright 1985-2003 Phoenix Technology Ltd

All Rights Reserved

Kontron® BIOS Version <CCALR418>

© Copyright 2002-2010 Kontron Embedded Modules GmbH

For legacy and legacy free systems please use BIOS files called CCALR2XX. (See 2.2.1)

For legacy and legacy free systems please use BIOS files called CCALR4xx. (See 2.2.2)

10.2 Setup Guide

The PhoenixBIOS Setup Utility changes system behavior by modifying the BIOS configuration. The setup program uses a number of menus to make changes and turn features on or off.

Note: Selecting incorrect values may cause system boot failure. Load setup default values to recover by pressing <F9>. It might also be necessary to use the "reset configuration data" option in the BIOS setup and set it to "yes". In certain circumstances this may also help to recover from system boot failure or a resource conflict.

10.2.1 Start Phoenix BIOS Setup Utility

To start the PhoenixBIOS setup utility, press <F2> when the following string appears during bootup.

Press <F2> to enter Setup

The Main Menu then appears.

The Setup Screen is composed of several sections:

Setup Screen	Location	Function
Menu Bar	Top	Lists and selects all top level menus.
Legend Bar	Bottom	Lists setup navigation keys.
Item Specific Help Window	Right	Help for selected item.
Menu Window	Left Center	Selection fields for current menu.
General Help Window	Overlay (center)	Help for selected menu.

Menu Bar

The menu bar at the top of the window lists different menus. Use the left/right arrow keys to make a selection.

Legend Bar

Use the keys listed in the legend bar on the bottom to make your selections or exit the current menu. The table below describes the legend keys and their alternates.

Key	Function
<F1> or <Alt-H>	General Help window.
<Esc>	Exit menu.
← or → Arrow key	Select a menu.
↑ or ↓ Arrow key	Select fields in current menu.
<Tab> or <Shift-Tab>	Cycle cursor up and down.
<Home> or <End>	Move cursor to top or bottom of current window.
<PgUp> or <PgDn>	Move cursor to next or previous page.
<F5> or <->	Select previous value for the current field.
<F6> or <+> or <Space>	Select next value for the current field.
<F9>	Load the default configuration values for this menu.
<F10>	Save and exit.
<Enter>	Execute command or select submenu.
<Alt-R>	Refresh screen.

Selecting an Item

Use the ↑ or ↓ key to move the cursor to the field you want. Then use the + and – keys to select a value for that field. The Save Value commands in the Exit menu save the values displayed in all the menus.

Displaying Submenus

Use the ← or → key to move the cursor to the submenu you want. Then press <Enter>. A pointer (▸) marks all submenus.

Item Specific Help Window

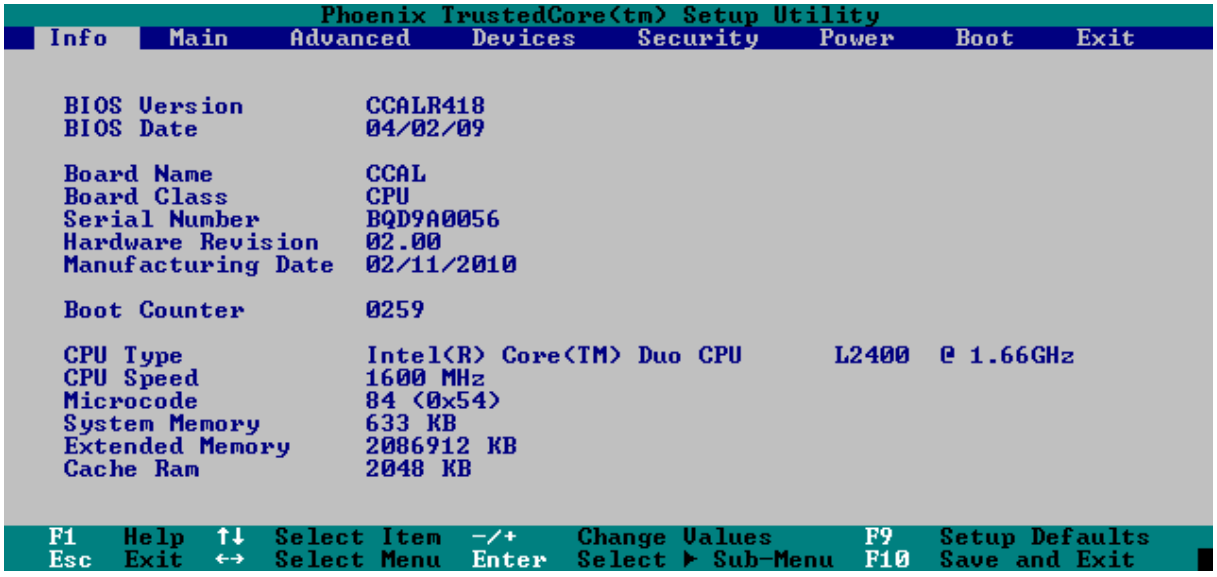
The Help window on the right side of each menu displays the Help text for the selected item. It updates as you move the cursor to each field.

General Help Window

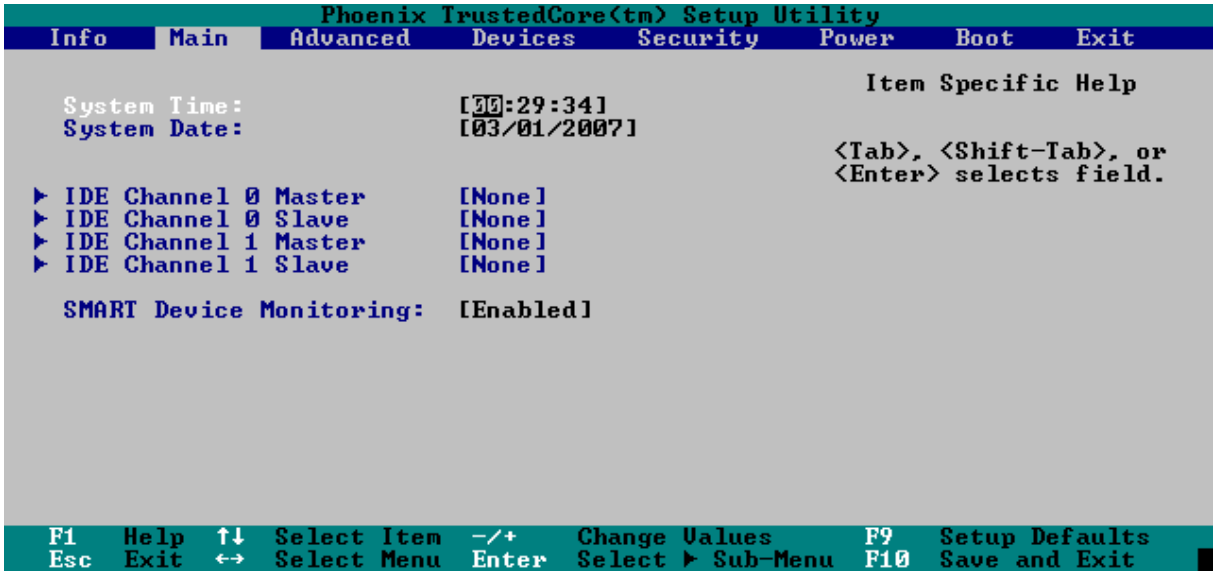
Pressing <F1> or <Alt-F1> on a menu brings up the General Help window that describes the legend keys and their alternates. Press <Esc> to exit the General Help window.

11 BIOS Setup

11.1 Info Screen

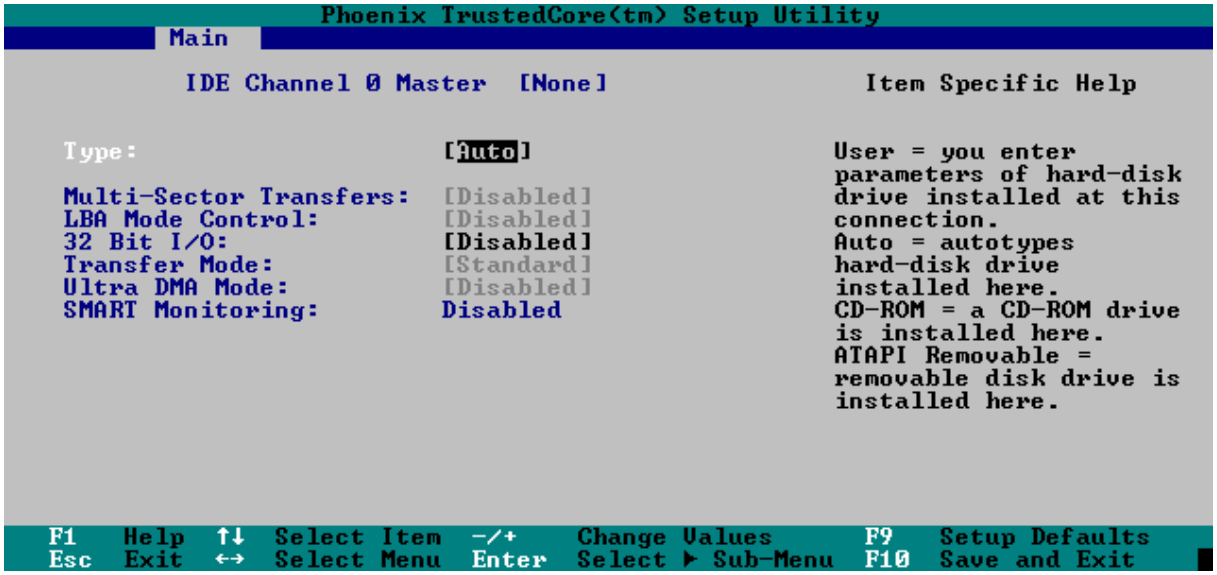


11.2 Main Menu



Feature	Option	Description
System Time	[hh:mm:ss]	<Tab>, <Shift-Tab>, or <Enter> selects field
System Date	[mm-dd-yyyy]	<Tab>, <Shift-Tab>, or <Enter> selects field
SMART Device Monitoring	**Enabled** Disabled	Enables and disables the harddisk error prediction tool

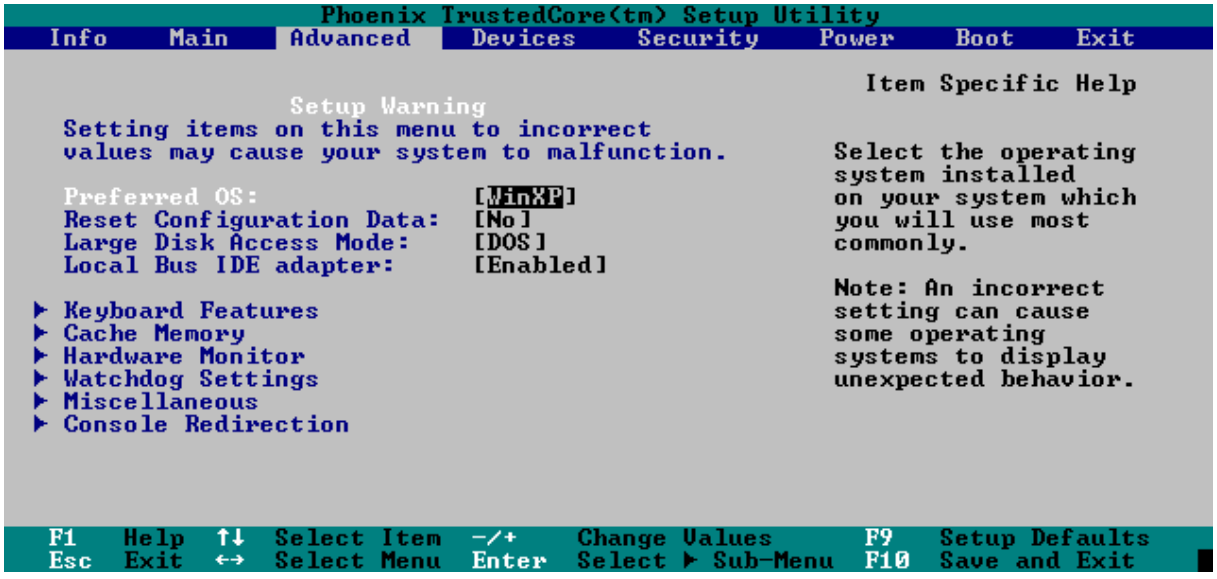
11.2.1 IDE Channels Submenu



Feature	Option	Description
Type	User **Auto** CD-ROM ATAPI Removable	
Multi-Sector Transfers	Disabled 2 Sectors 4 Sectors 8 Sectors 16 Sectors	Specify the number of sectors per block for multiple sector transfers
LBA Mode Control	Disabled Enabled	Enabled LBA causes Logical Block Addressing to be used in place of Cylinders, Heads _Sectors.
32 Bit I/O	**Disabled** Enabled	This setting enables or disables 32 bit data transfers.
Transfer Mode	Standard Fast PIO 1 Fast PIO 2 Fast PIO 3 Fast PIO 4 FPIO 3 / DMA 1 FPIO 4 / DMA 2	Selects the method for moving data to/from the drive. Autotype the drive to select the optimum transfer mode.
Ultra DMA Mode	Disabled	Selects the Ultra DMA mode used for moving data to/from the drive. Autotype the drive to select the optimum transfer mode.
SMART Monitoring		Shows if the device is capable of using the error prediction tool

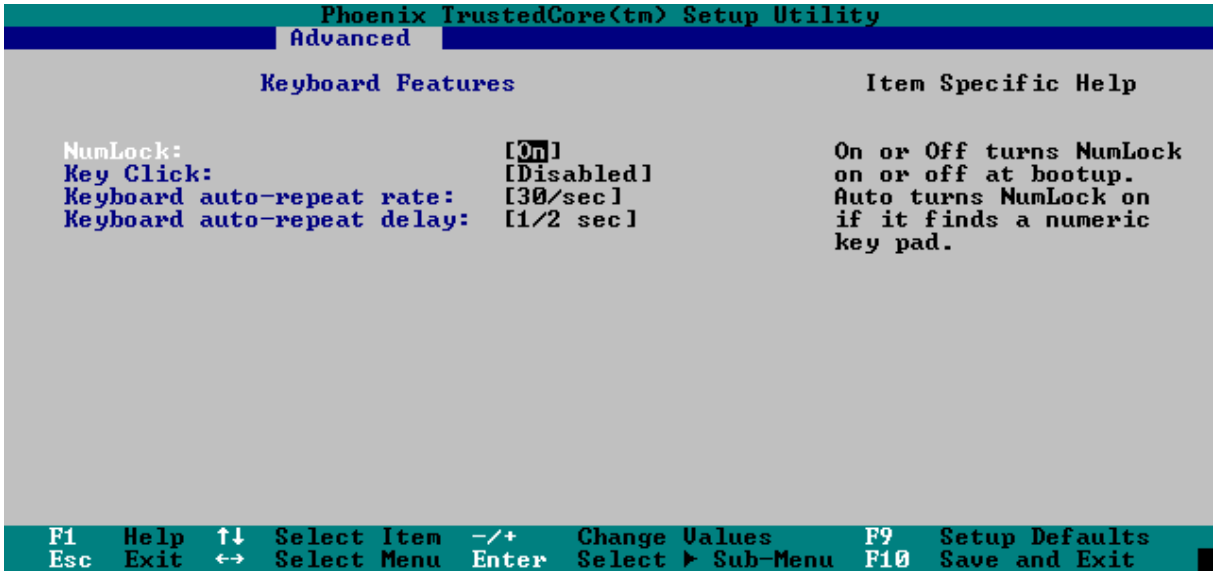
Note: Menu appearing depends on the connection of device

11.3 Advanced



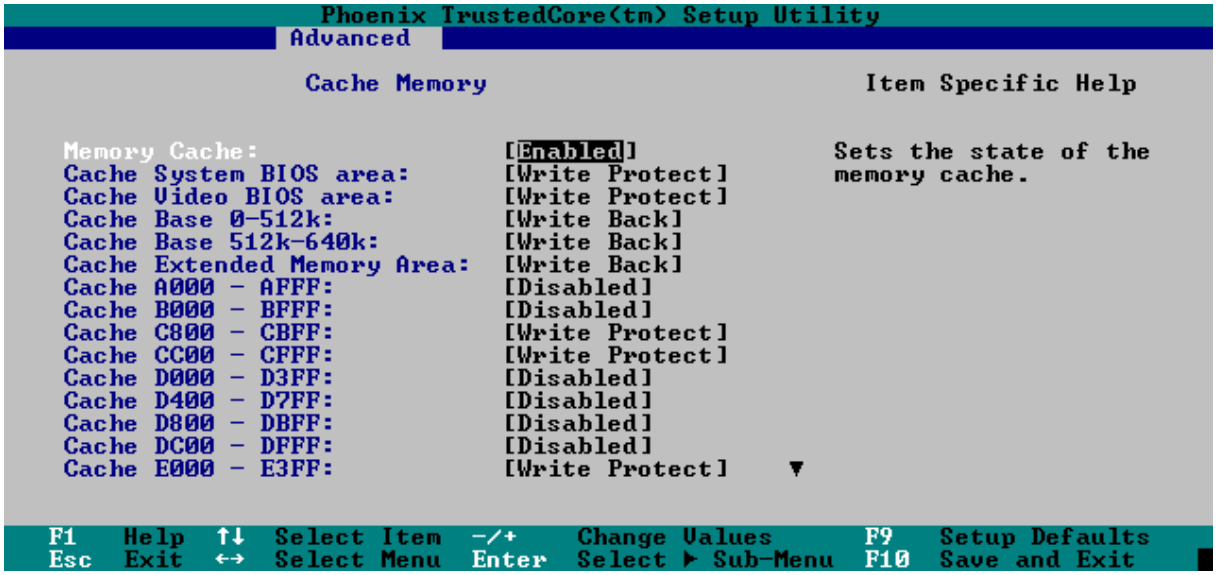
Feature	Option	Description
PNP OS installed	Other Win95 Win98 WinME Win2000 **WinXP**	Select the operating system installed on your system which you will use most commonly.
Reset Configuration Data	**No** Yes	Select 'Yes' if you want to clear the Extended System Configuration Data (ESCD) area.
Large Disk Access Mode	Other **DOS**	UNIX, Novell Netware, or other operating systems, select 'Other'. If you are installing new software and the drive fails, change this selection and try again. Different operating systems require different representations of drive geometries.
Local Bus IDE adapter	Disabled **Primary** Secondary Both	Enable the integrated local bus IDE adapter

11.3.1 Keyboard Features Submenu



Feature	Option	Description
NumLock	Auto **On** Off	Selects Power-on state for NumLock
Key Click	**Disabled** Enabled	Enables Key Click
Keyboard auto-repeat rate	**30/sec** 26.7/sec 21.8/sec 18.5/sec 13.3/sec 10/sec 6/sec 2/sec	Selects key repeat rate
Keyboard auto-repeat delay	¼ sec **½ sec** ¾ sec 1 sec	Selects delay before key repeat

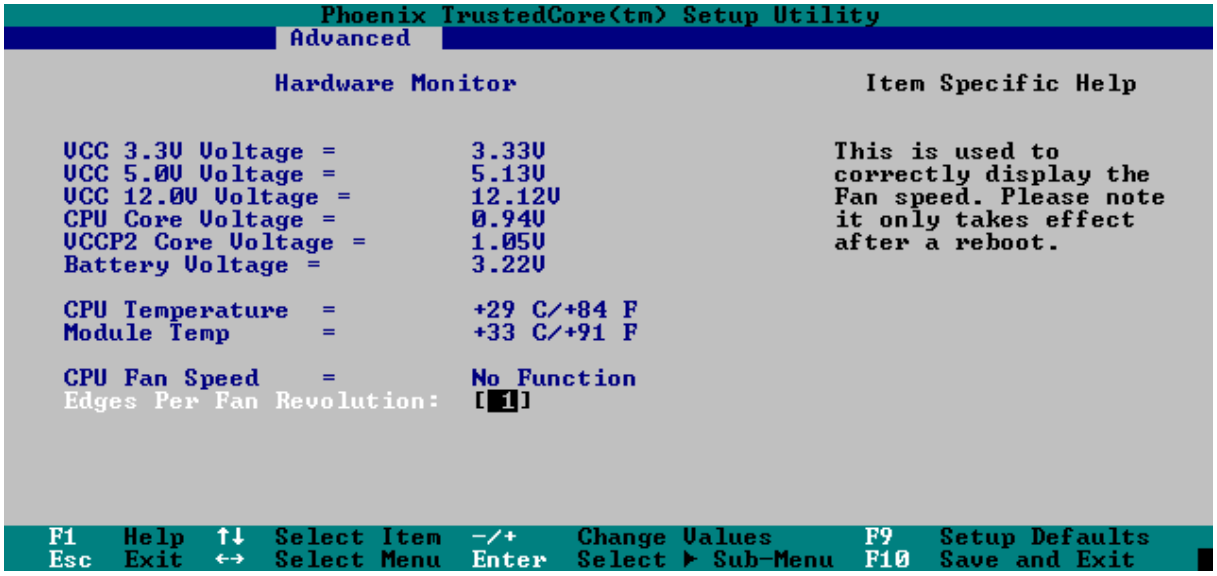
11.3.2 Cache Memory Submenu



Feature	Option	Description
Memory Cache	Disabled **Enabled**	Sets the state of the memory cache
Cache System BIOS area	Uncached **Write Protect**	Controls caching of system BIOS area
Cache Video BIOS area	Uncached **Write Protect**	Controls caching of video BIOS area
Cache Base 0-512k	Uncached Write Through Write Protect **Write Back**	Controls caching of 512k base memory
Cache Base 512k-640k	Uncached Write Through Write Protect **Write Back**	Controls caching of 512k 640k base memory
Cache Extended Memory Area	Uncached Write Through Write Protect **Write Back**	Controls caching of system memory above one megabyte
Cache A000-AFFF	**Disabled** USWC caching Write Through Write Protect Write Back	Disabled – This block is not cached. USWC – Uncached Speculative Write Combined. Write Through – Writes are cached and sent to main memory at once. Write Protect – Writes are ignored. Write Back – Writes are cached but not sent to main memory until necessary
Cache B000-BFFF	**Disabled** USWC caching Write Through Write Protect Write Back	
Cache C800-CBFF	Disabled Write Through **Write Protect** Write Back	Disabled – This block is not cached. Write Through – Writes are cached and sent to main memory at once. Write Protect – Writes are ignored. Write Back – Writes are cached but not sent to main memory until necessary
Cache CC00-CFFF	Disabled Write Through **Write Protect**	

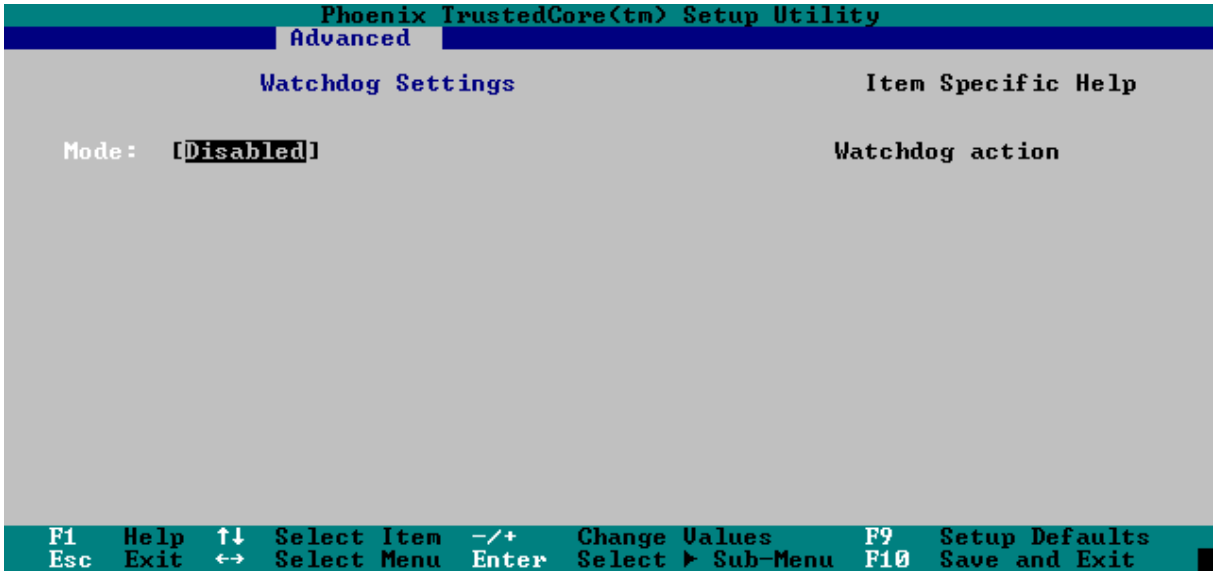
Feature	Option	Description
	Write Back	
Cache D000-D3FF	**Disabled** Write Through Write Protect Write Back	
Cache D400-D7FF	**Disabled** Write Through Write Protect Write Back	
Cache D800-DBFF	**Disabled** Write Through Write Protect Write Back	
Cache DC00-DFFF	**Disabled** Write Through Write Protect Write Back	
Cache E000-E3FF	Disabled Write Through **Write Protect** Write Back	
Cache E400-E7FF	Disabled Write Through **Write Protect** Write Back	
Cache E800-EBFF	Disabled Write Through **Write Protect** Write Back	
Cache EC00-EFFF	Disabled Write Through **Write Protect** Write Back	

11.3.3 Hardware Monitor Submenu



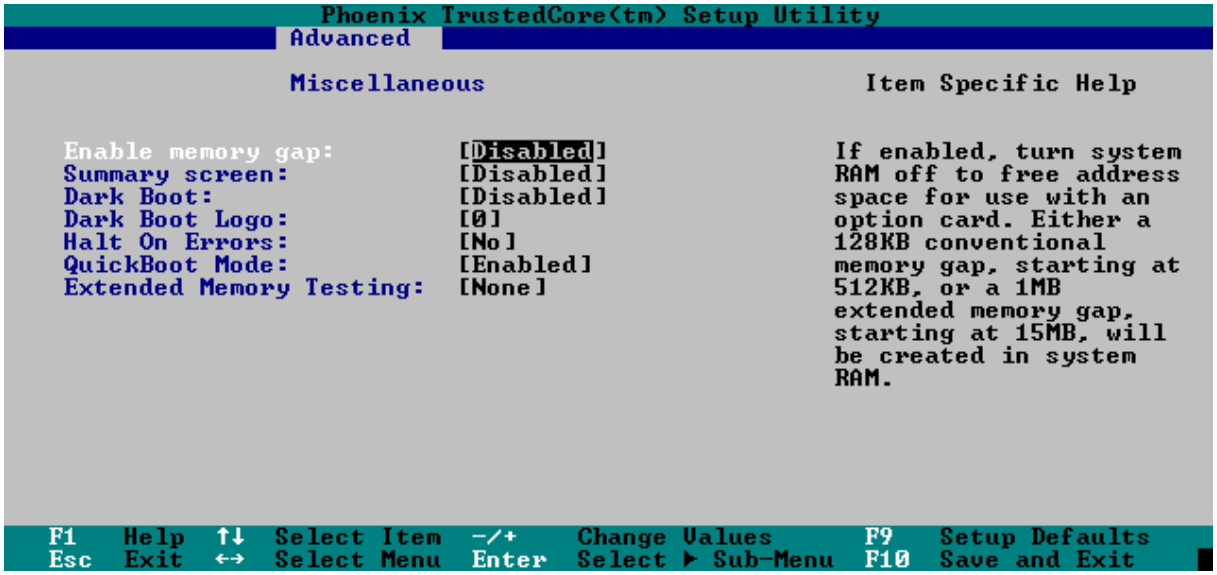
Feature	Option	Description
Edges Per Fan Revolution	0 ... 15	This is used to configure the pulses per revolution for you rfan

11.3.4 Watchdog Settings Submenu



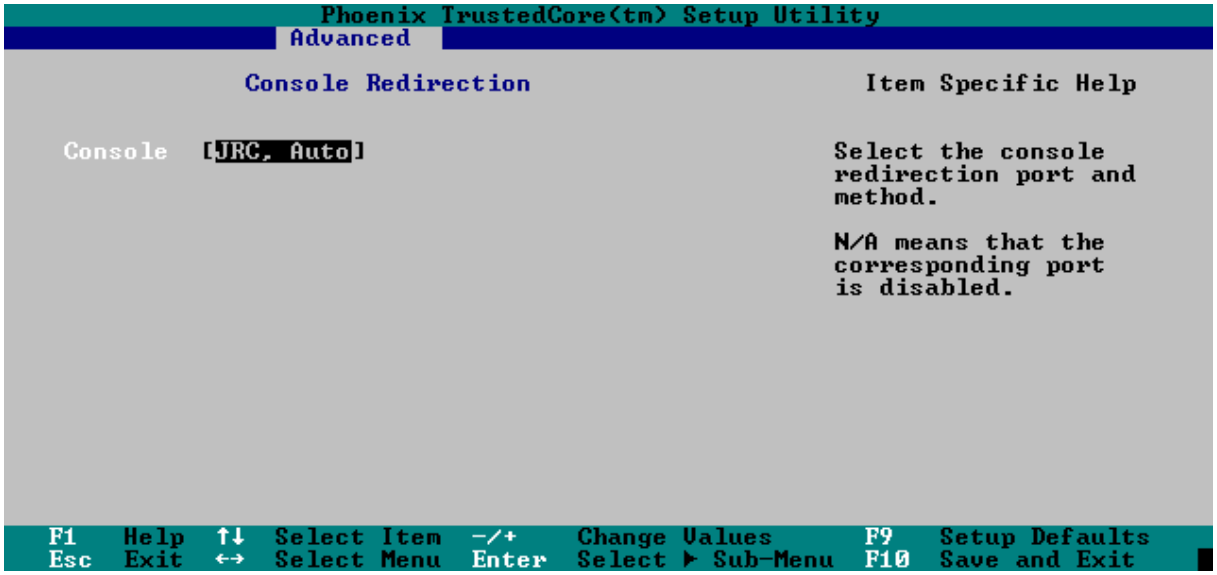
Feature	Option	Description
Mode	**Disabled** Reset NMI	Watchdog action
Timeout	1sec 5sec 10sec **30sec** 1min 5.5min 10.5min 30.5min	Max. trigger periode
Delay	1sec 5sec 10sec **30sec** 1min 5.5min 10.5min 30.5min	Time until watchdog timer starts to count

11.3.5 Miscellaneous Submenu



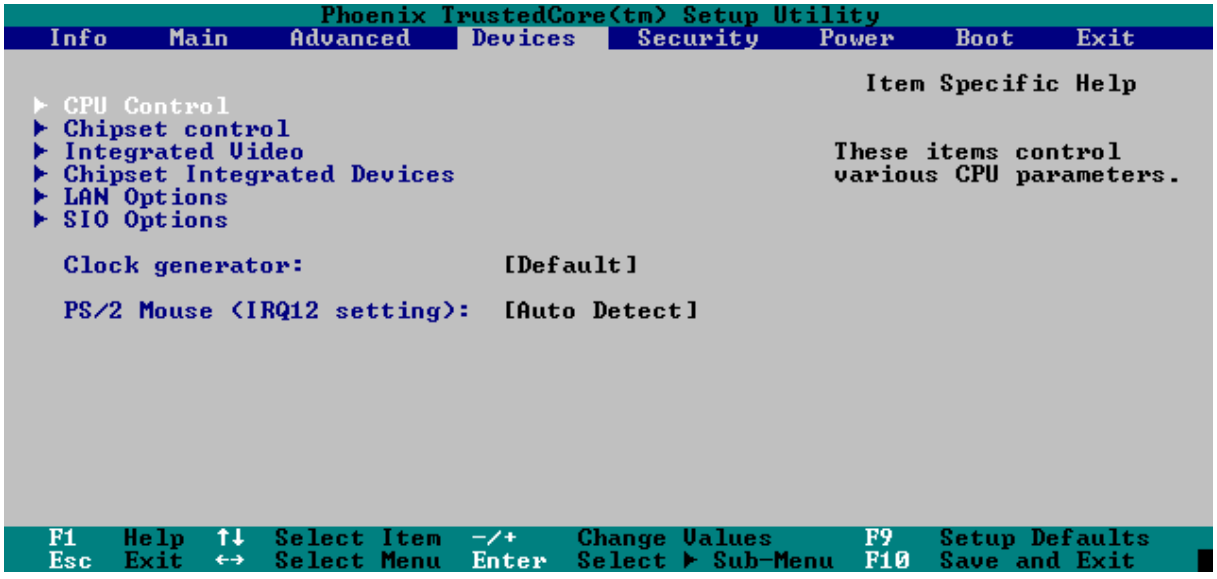
Feature	Option	Description
Enabled memory gap	**Disabled** Extended	If enabled, turn system RAM off to free address space for use with an option card. Either a 128KB conventional memory gap, starting at 512KB, or a 1MB extended memory gap, starting at 15MB, will be created in system RAM.
Summary screen	Disabled **Enabled**	Display system configuration on boot
Dark Boot	**Disabled** Enabled	Prevent diagnostic screen output during boot
Dark Boot Logo	**0** 1	Use -/+ to select the Dark Boot logo 0 – Vendor Logo 1 – Blank screen
Halt On Errors	**No** Yes	Determines if errors cause the system to halt
QuickBoot Mode	Disabled **Enabled**	Allows the system to skip certain tests while booting. This will decrease the time needed to boot the system.
Extended Memory Testing	Normal Just zero it **None**	Determines which type of tests will be performed on extended memory (above 1MB).

11.3.6 Console Redirection Submenu



Feature	Option	Description
Console	Disabled UCR, COM A UCR, COM B **JRC, Auto**	Select the console redirection method
Baud Rate	300 1200 2400 **9600** 19.2k 38.4k 57.6k 115.2k	Enables the specified baud rate
Console Type	VT100 **VT100, 8bit** PC-ANSI PC-ANSI, 7bit VT100+ VT-UTF8 ASCII	Enables the specified console type
Flow Control	**None** XON/XOFF CTS/RTS	Enables Flow Control
Console connection	**Direct** Via modem	Indicate whether the console is connected directly to the system or a modem is used to connect
Continue C.R. after POST	Off **On**	Enables Console Redirection after OS has loaded

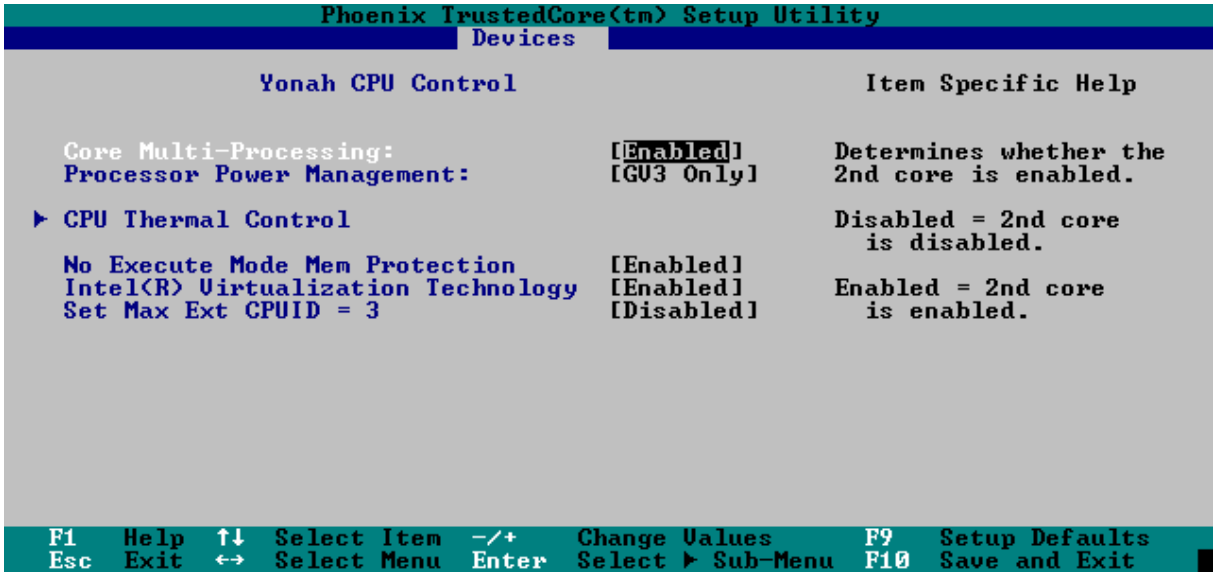
11.4 Devices



Feature	Option	Description
Clock generator	**Default** Program	Controls programming of the clock chip. Default = Uses PowerOn defaults. No chip access via SMBus needed. Program = Allows to change spread spectrum and FSB speed settings.
PS/2 Mouse	Disabled Enabled **Auto Detect**	'Disabled' prevents any installed PS/2 mouse from functioning, but frees up IRQ12. 'Enabled' forces the PS/2 port to be enabled regardless if a mouse is present. 'Auto Detect' will enable the PS/2 mouse only if present. 'OS controlled' only displayed if the OS controls the mouse.

11.4.1 CPU Control

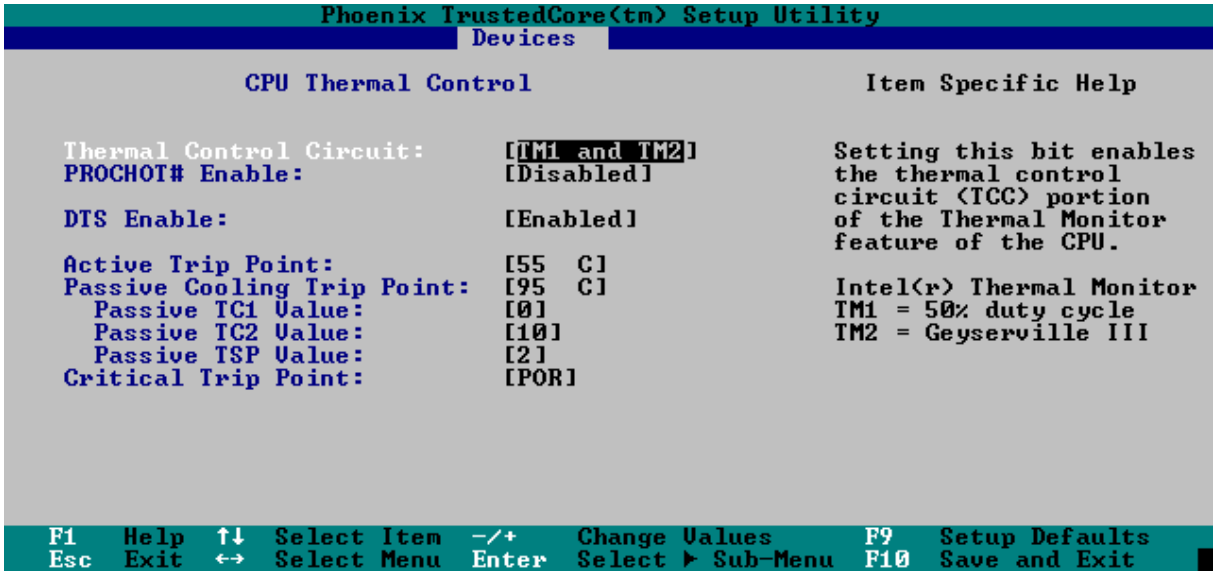
CPU control detects which processor core is used and displays an additional submenu with the detected processor core (yonah, merom, etc.).



Feature	Option	Description
Core Mutli-Processing	**Enabled** Disabled	Disables or enables the second CPU core
Processor Power Management	Disabled **GV3 only** C-States only Enabled	Selects the Processor Power Management desired: Disabled = C-States and GV3 are disabled. GV3 only = C-States are disabled. C-States only = GV3 is disabled. Enabled = C-States and GV3 are enabled
No Execute Mode Mem Protection	Disabled **Enabled**	
Intel® Virtualization Technology	Disabled **Enabled**	When enabled, a VMM can utilize the additional hardware virtualization capabilities provides by this technology
Set Max Ext CPUID = 3	**Disabled** Enabled	Sets Max CPUID extended function value to 3

Note: when a Pentium M C423 is in use, then GV3 is not possible and C-States only is the default setting of Processor Power Management

CPU Thermal Control

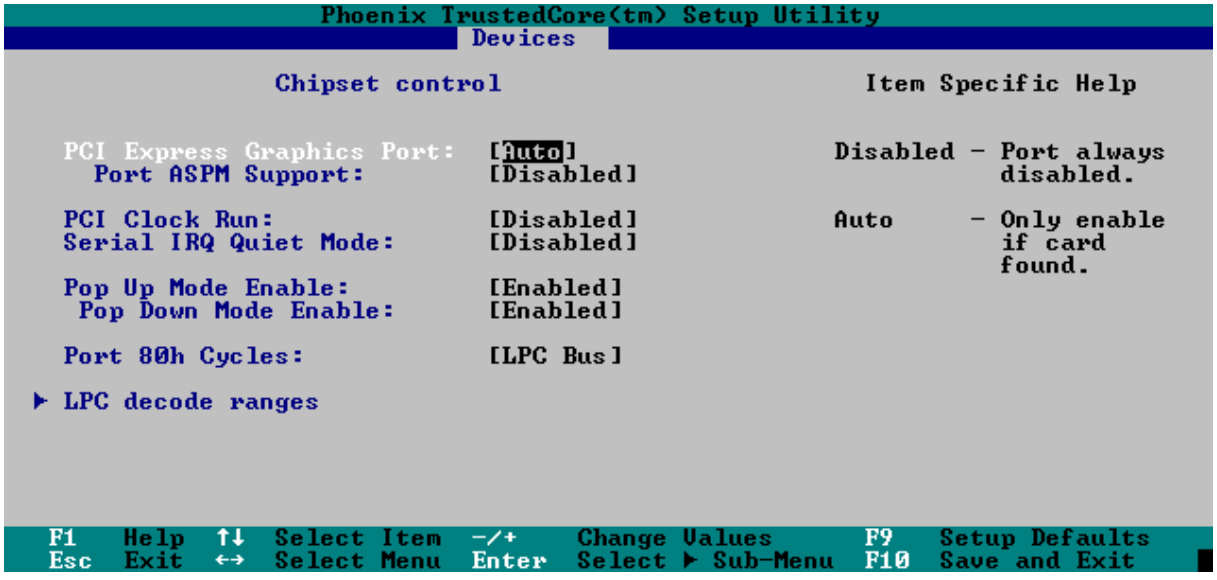


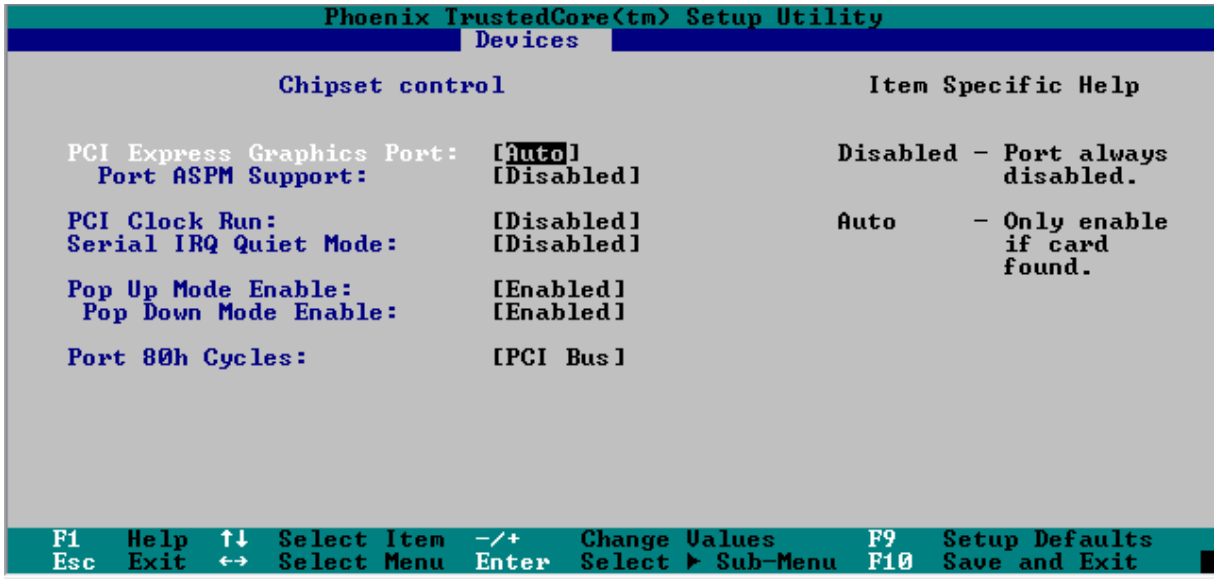
Feature	Option	Description
Thermal Control Circuit	Disabled TM1 TM2 **TM1 and TM2**	Setting this bit enables the thermal control circuit (TCC) portion of the Thermal Monitor feature of the CPU. Intel ® Thermal Monitor TM1 = 50% duty cycle TM2 = Geyserville III
PROCHOT# Enable	**Disabled** Enabled	Enables the processors' PROCHOT# signal. If asserted, TMx circuit will be engaged. PROCHOT# is in addition to the TCC and Enhanced TCC circuitry inside the processor and either may engage TMx
DTS Enable	Disabled **Enabled**	Enables the Yonah DTS to be used for platform Thermal Management
Active Trip Point	Disabled 15 C 23 C 31 C 39 C 47 C **55 C** 63 C 71 C 79C 87 C 95 C 103 C 111 C 119 C	This value controls the temperature of ACPI Active Trip Point – the point in which the OS will turn the CPU fan on
Passive Cooling Trip Point	Disabled 15 C 23 C 31 C 39 C 47 C 55 C 63 C 71 C	This value controls the temperature of ACPI Passive Trip Point – the point in which the OS will begin throttling the CPU

Feature	Option	Description
	79C 87 C **95 C** 103 C 111 C 119 C	
Passive TC1 Value	**0** 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15	This value sets the TC1 value for the ACPI Passive Cooling Formula
Passive TC2 Value	0 1 2 3 4 5 6 7 8 9 **10** 11 12 13 14 15	This value sets the TC2 value for the ACPI Passive Cooling Formula
Passive TSP Value	1 **2** 3 4 5 6 7 8 9 10 11 12 13 14 15	This item sets the TSP value for the ACPI Passive Cooling Formula. It represents the tenth of a second how often the OS will read the temperature when Passive Cooling is Enabled
Critical Trip Point	**POR** 15 C 23 C 31 C 39 C	This value controls the temperature of the ACPI Critical Trip Point – the point in which the OS will shut the system off.

Feature	Option	Description
	47 C	
	55 C	
	63 C	
	71 C	
	79C	
	87 C	
	85 C	
	103 C	
	111 C	
	119 C	
	127 C	

11.5 Chipset Control

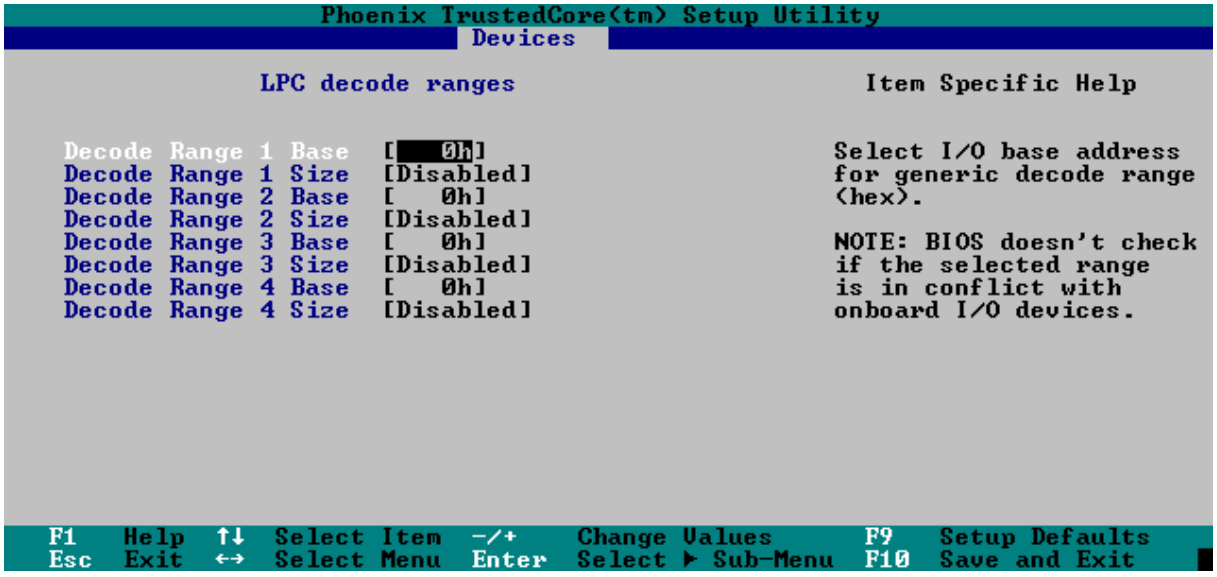




Feature	Option	Description
PCI Express Graphics Port	Disabled **Auto**	Disabled – Port always disabled Auto – Only enable if card found
Port ASPM Support	**Disabled** Auto	Controls ASPM support for the PEG Device. Auto = will set ASPC to the highest common supported ASPM between the Port and Endpoint
PCI Clock Run	**Disabled** Enabled	If Enabled, the CLKRUN# logic will stop the PCI Clocks
Serial IRQ Quiet Mode	**Disabled** Enabled	Enabled: The Serial IRQ will be placed in "Quiet" mode. Disabled: The Serial IRQ will be placed in "Continuous" mode
Pop Up Mode Enable	Disabled **Enabled**	If enabled, ICH will observe a bus master request and it will take the system from a C3/C4 state to a C2 state and auto enable bus masters.

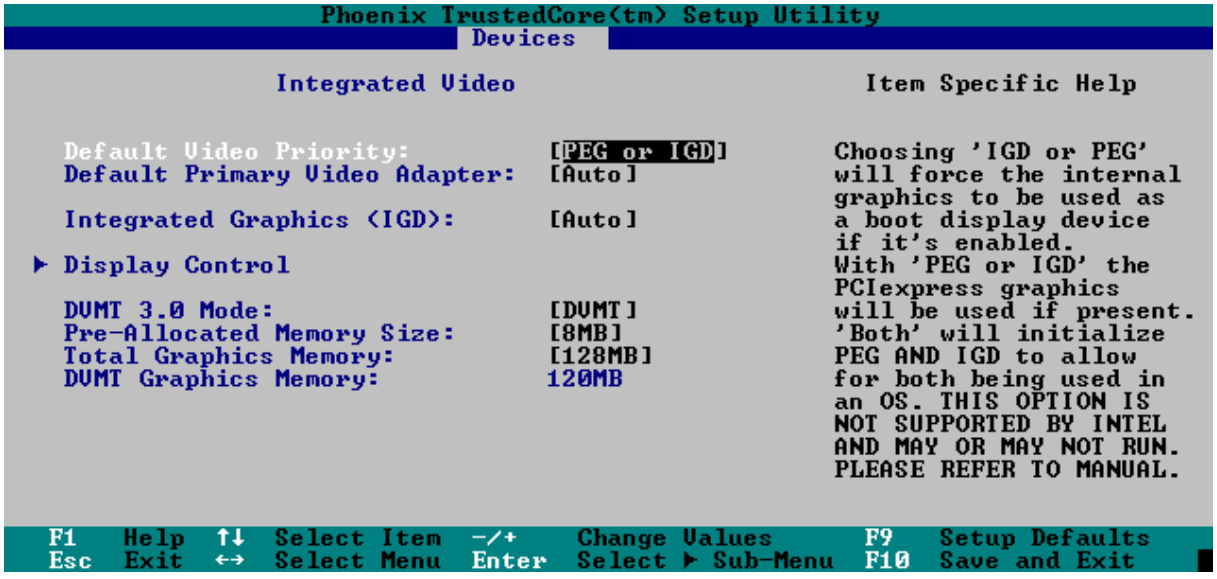
Feature	Option	Description
		If disabled, bus master traffic is a break event and it will return from C3/C4 to C0 based on break events
Pop Down Mode Enable	Disabled **Enabled**	If enabled, ICH will observe a NO bus master request and it can to a previous C3 or C4 state. If disabled, ICH will NOT attempt to automatically return
Port 80h Cycles	LPC Bus **PCI Bus**	Control where the Port 80h cycles are sent

LPC decode Ranges



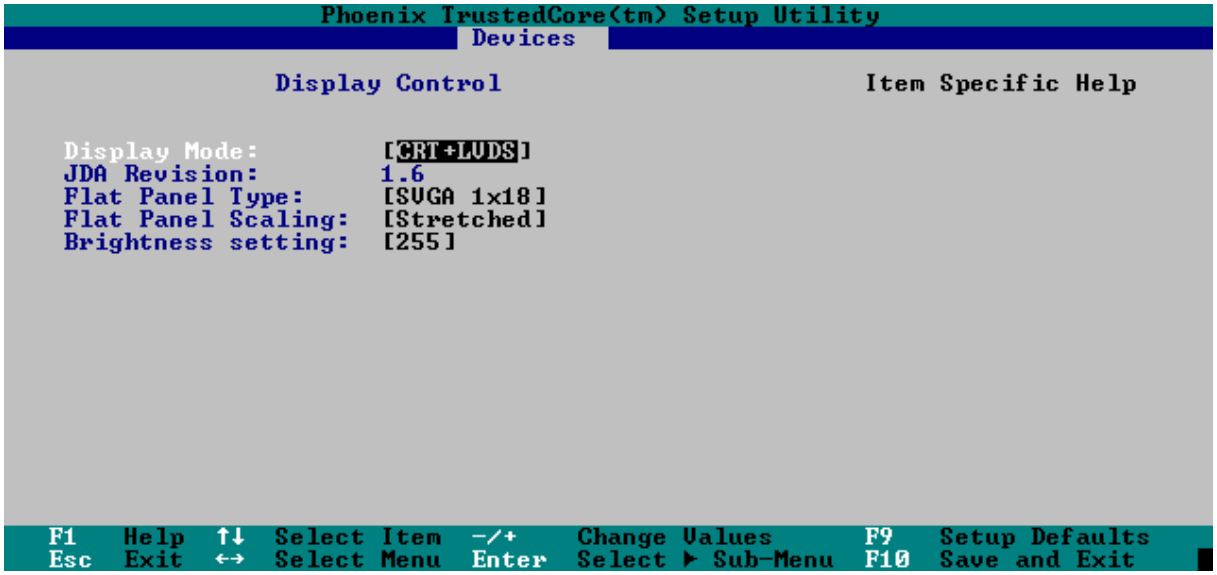
Feature	Option	Description
Decode Range x Base	**0h** - FFFFh	Select I/O base address for generic decode range
Decode Range x Size	**Disabled** 4 8 16 32 64 128 258	Select generic decode range size

11.6 Integrated Video



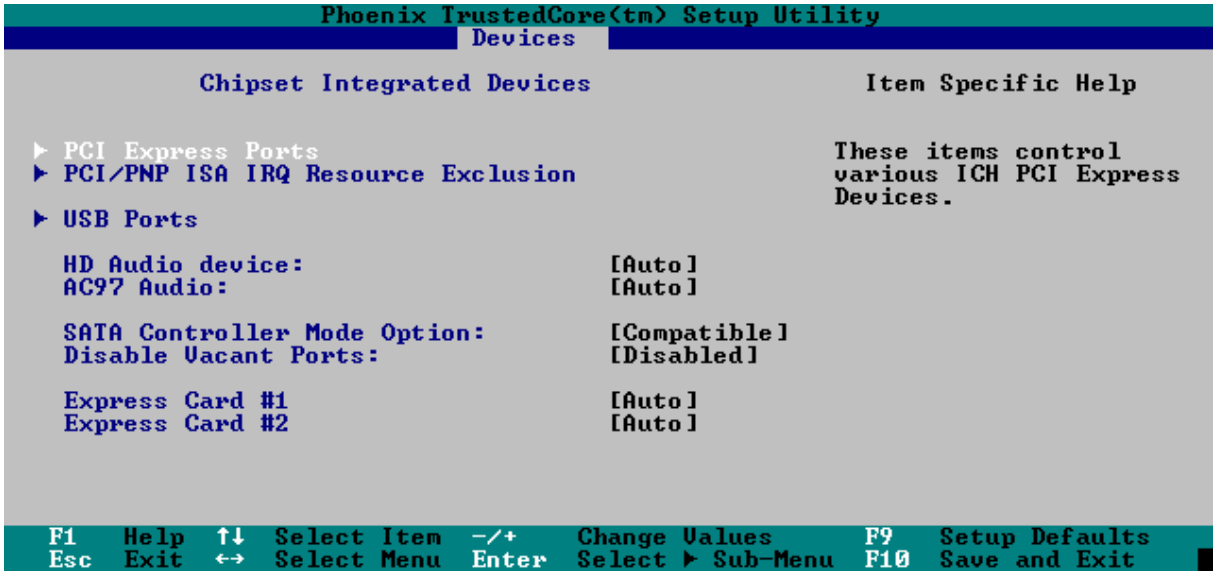
Feature	Option	Description
Default Video Priority	IGD or PEG **PEG or IGD** both	Chossing 'IGD or PEG' will force the internal graphics to be used as a boot display device if it's enabled. With 'PEG or IGD' the PCIexpress graphics will be used if present. 'Both' will initialize PEG AND IGD to allow both being used in an OS. The option 'Both' is not supported by Intel and may not work in all configurations.
Default Primary Video Adapter	IGD **PEG**	This entry allows to select the display device used by the BIOS during POST and as the basic graphics device for the OS. Only devices that are ready to be used are listed here. If 'Auto' is selected, the priority of the primary display device is PEG>PCI>IGD
Integrated Graphics <IGD>	Disabled **Auto**	Enable or Disable the Internal Graphics Device by setting item to the desired value
DVMT 3.0 Mode	Fixed **DVMT** Combo	Select the configuration of the DVMT 3.0 Graphics Memory that Driver will allocate for use by the Internal Graphics Device. 1.Fixed 2. DVMT 3. Combo
Pre-Allocated Memory Size	1MB **8MB**	Select the amount of Pre-Allocated Graphics Memory for use by the Internal Graphics Device
Total Graphics Memory	64MB **128MB** MaxDVMT	Select the amount of Total Graphics Memory – Pre-Allocated + Fixed + DVMT for use by the Internal Graphics Device
DVMT Graphics Memory		Shows the current DVMT Graphics Memory

11.6.1 Display Control



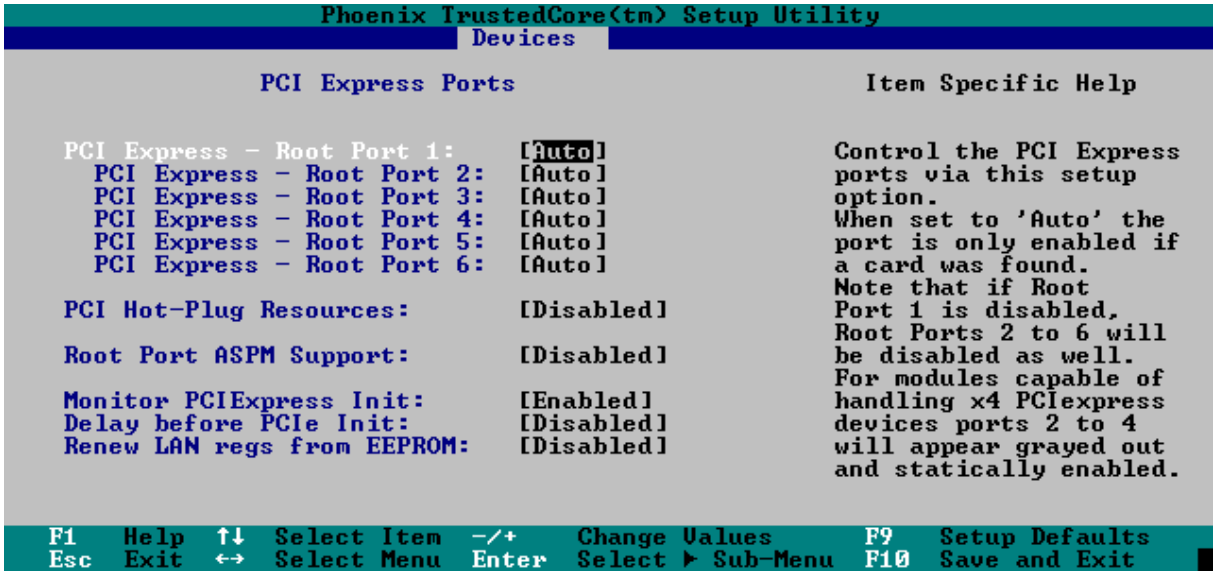
Feature	Option	Description
Display Mode	CRT only TV only LVDS only **CRT+LVDS** LVDS+SDVO	Select the enabled graphics output during POST
JDA Revision		Shows the current revision of JDA
Flat Panel Type	VGA 1x18 SVGA 1x18 XGA 1x18 XGA 1x24 SXGA 2x18 SXGA 2x24 UXGA 2x18 Enter PAID Enter FPID **Auto**	Select [Auto] for JILI or one of the predefined LCD's Use [Enter PAID] or [Enter FPID] to manually enter panel adapter ID or flat panel ID.
Flat Panel Scaling	Centered **Stretched**	
Brightness setting	0 ... **255**	This option allows to set the level of brightness of a connected LCD. Values may range from 0 to 255.

11.7 Chipset Integrated Devices



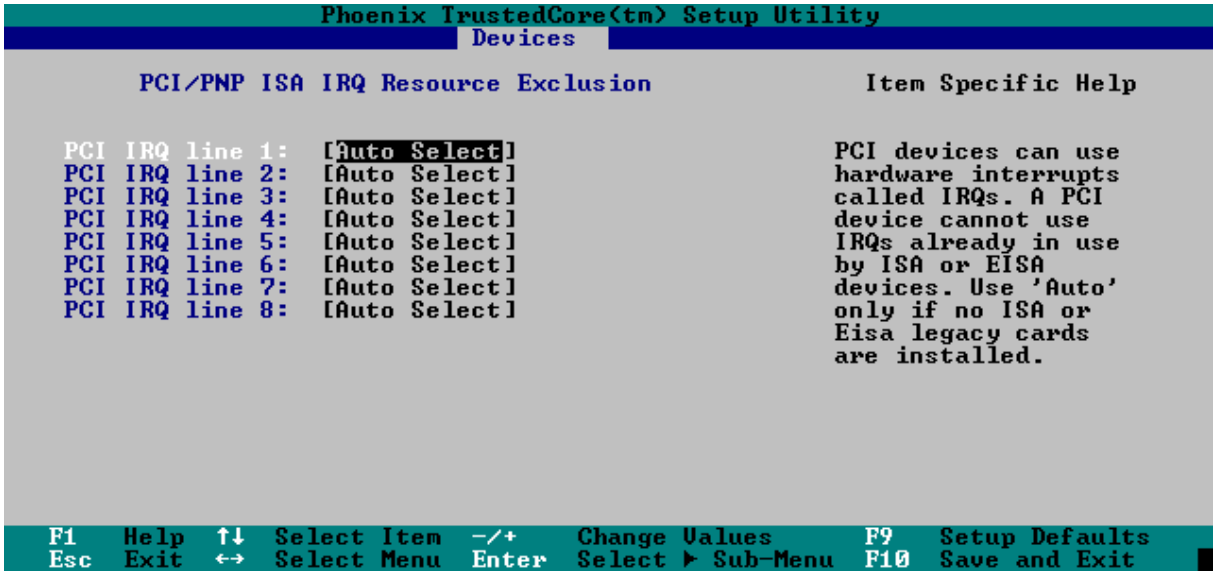
Feature	Option	Description
HD Audio device	Disabled **Auto**	Control Detection of the HD Audio Device. Auto = HD Audio will be enabled if present, disabled otherwise Disabled = HD Audio will be unconditionally disabled, regardless of precense.
AC97 Audio	Disabled **Auto**	Control Detection of the AC97 Audio Device. Auto = AC97 Audio will be enabled if present, disabled otherwise Disabled = AC97 Audio will be unconditionally disabled, regardless of presence.
SATA Controller Mode Option	**Compatible** Enhanced	Compatible mode: SATA and PATA drives are auto-detected and placed in Legacy mode Enhanced (non-AHCI) mode: SATA and PATA drives are auto-detected and placed in their native modes
Disable Vacant Ports	**Disabled** Enabled	Controls automatic disabling of vacant SATA ports
Express Card #1/#2	Disabled **Auto** Enabled	'Auto' enables Express Card slot if card is inserted. 'Enabled' or 'Disabled' permanently enables/disables the slot.

11.7.1 PCI Express Ports



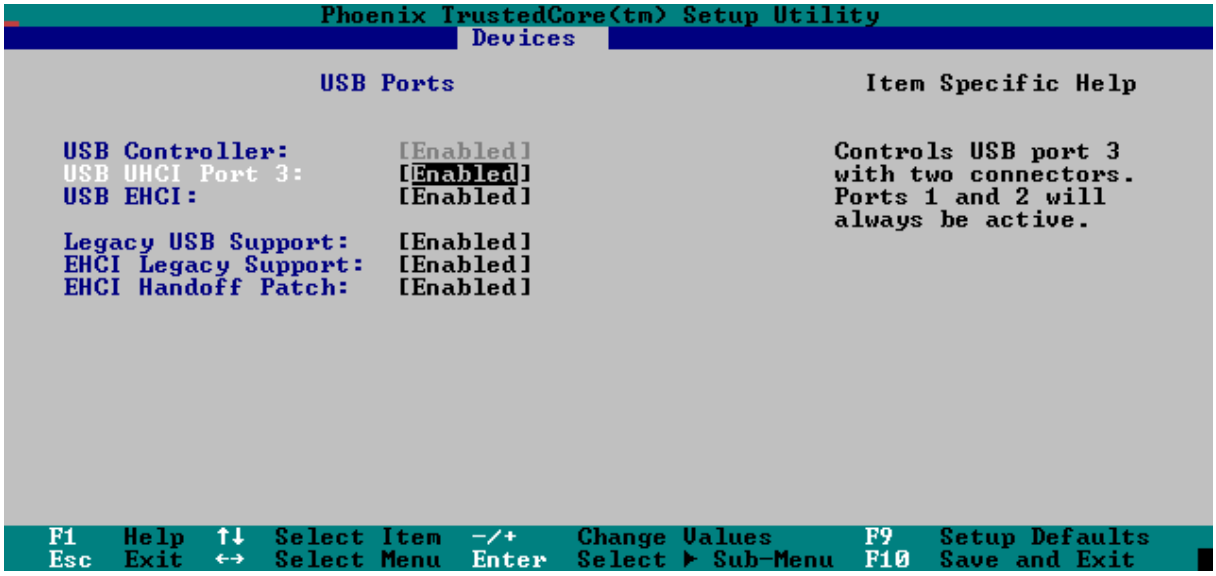
Feature	Option	Description
PCI Express – Root Port 1	Disabled Enabled **Auto**	Control the PCI Express Port via this setup option. Disabled – Port always disabled. Auto – Only enable if card found Note that if Root Port 1 is disabled, Root Ports 2-4 will be disabled as well.
PCI Express – Root Port 2	Disabled Enabled **Auto**	
PCI Express – Root Port 3	Disabled Enabled **Auto**	
PCI Express – Root Port 4	Disabled Enabled **Auto**	
PCI Express – Root Port 5	Disabled Enabled **Auto**	
PCI Express – Root Port 6	Disabled Enabled **Auto**	
PCI Hot-Plug Resources	**Disabled** Enabled	Enabled/Disable Hot-Plug support
Root Port ASPM Support	**Disabled** Auto	Control ASPM support for all the enabled Root Ports. Auto = will set ASPM to the highest common supported ASPM between the Port and Endpoint.
Monitor PCIExpress Init	Disabled **Enabled**	If enabled this control enables the watchdog during PCIexpress init.
Delay before PCIe Init	**Disabled** Enabled	If enabled this control activates a short delay just before initializing PCIexpress devices
Renew LAN regs from EEPROM	**Disabled** Enabled	If enabled the LAN registers are re-read from EEPROM during POST

11.7.2 PCI/PNP ISA IRQ Ressource Exclusion



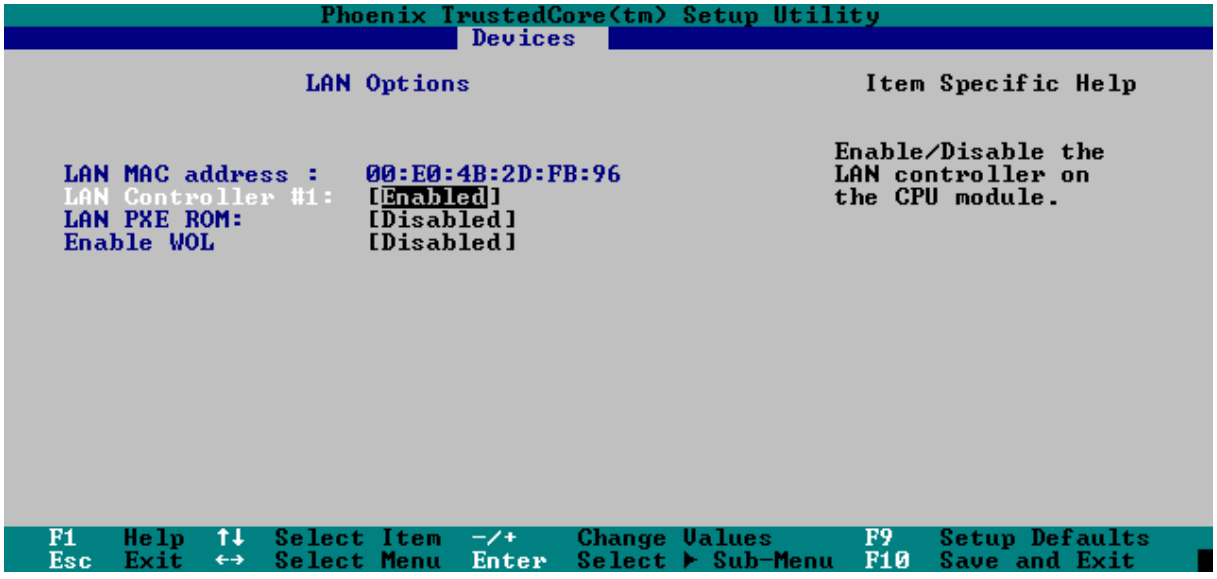
Feature	Option	Description
PCI IRQ line 1 - 8	Disabled **Auto Select** 3 4 5 7 9 10 11 12 14 15	PCI devices can use hardware interrupts called IRQs. A PCI device cannot use IRQs already in use by ISA or EISA devices. Use 'Auto' only if no ISA or Eisa legacy cards are installed.

11.7.3 USB Ports



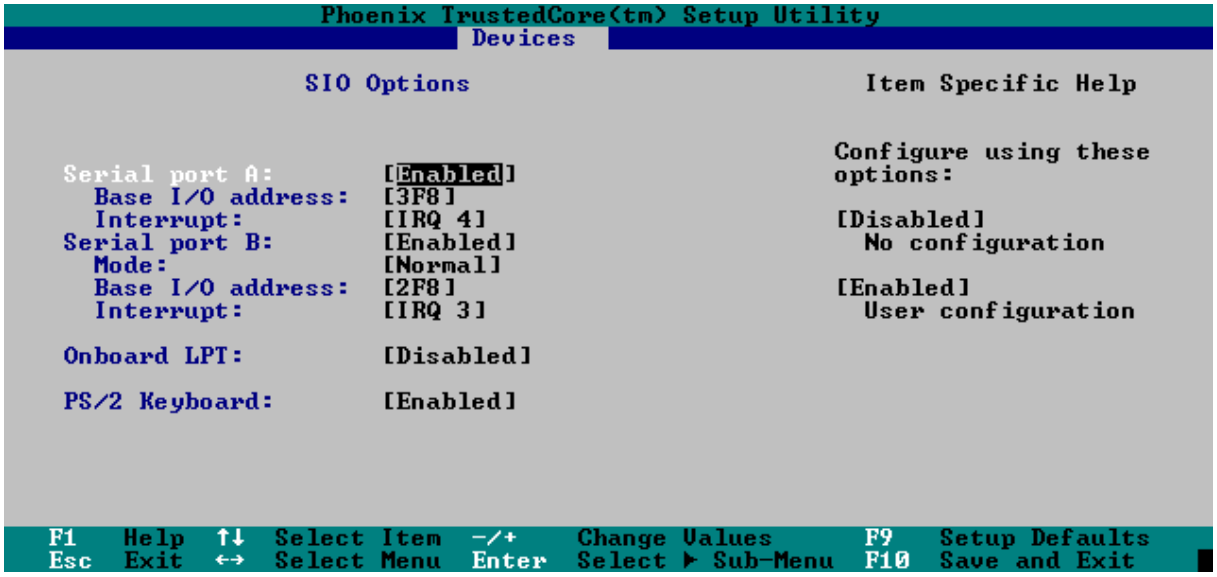
Feature	Option	Description
USB Controller	Disabled **Enabled**	Controls the whole USB controller. If disabled, no USB will be available.
USB UHCI Port 3	Disabled **Enabled**	Controls USB Port 3 with two connectors. Port 1 and 2 will always be active.
USB EHCI	Disabled **Enabled**	Controls USB 2.0 functionality for all the ports set to active state.
Legacy USB Support	Disabled **Enabled**	Enable support for Universal Serial Bus
EHCI Legacy Support	Disabled **Enabled**	This switch enables or disables EHCI support in legacy mode.
EHCI Handoff Patch	Disabled **Enabled**	This patch must be allied if OSes before WinXP SP2 have problems gaining control over USB EHCI ports. It should not be necessary for newer OSes.

11.8 LAN Options



Feature	Option	Description
LAN MAC address		
LAN Controller #1	Disabled **Enabled**	Enable/Disable the LAN controller on the CPU module.
Onboard LAN PXE ROM	**Disabled** Enabled	Enables the remote boot BIOS extension for the onboard LAN controller.
Enable WOL	**Disabled** Enabled	Enables the LAN device to wake the system from a sleep state (wake-on-LAN).

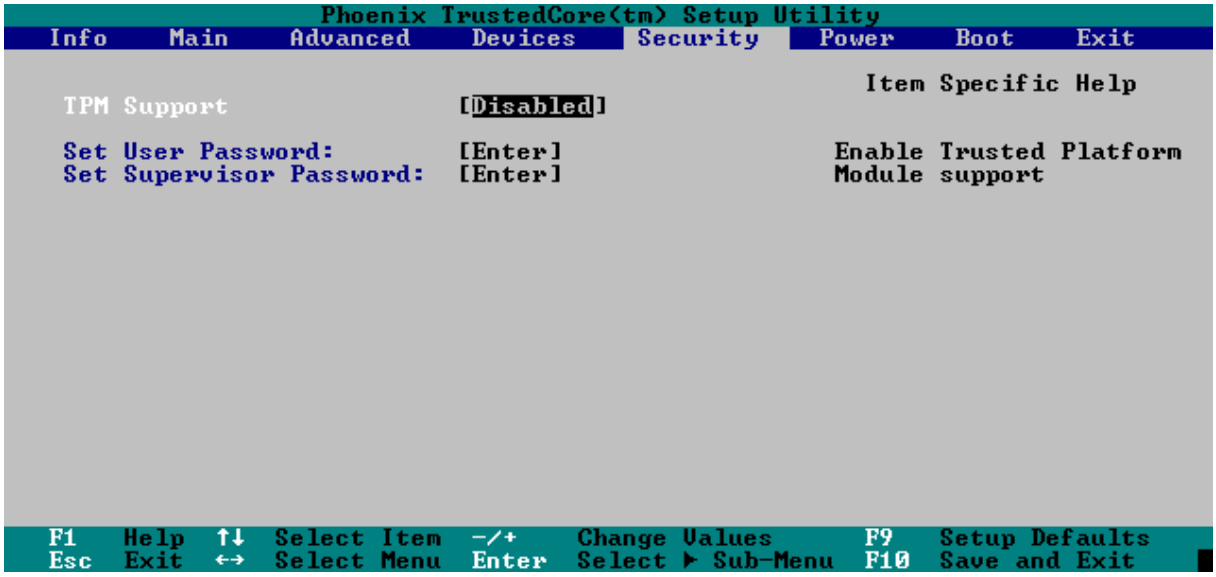
11.9 SIO Options



Feature	Option	Description
Serial port A	Disabled **Enabled** Auto	Configure using these options: [Disabled] No Configuration [Enabled] User Configuration [Auto] BIOS or OS chooses configuration
Base I/O address	**3F8** 2F8 3E8 2E8	Set the base I/O address for serial port A
Interrupt	IRQ 3 **IRQ 4**	Set the interrupt for serial port A
Serial port B	Disabled **Enabled** Auto	Configure using these options: [Disabled] No Configuration [Enabled] User Configuration [Auto] BIOS or OS chooses configuration
Mode	**Normal** IR ASK-IR	Set the mode for serial port B
Base I/O address	3F8 **2F8** 3E8 2E8	Set the base I/O address for serial port B
Interrupt	**IRQ 3** IRQ 4	Set the interrupt for serial port B
Onboard LPT	Disabled Enabled **Auto**	Configures the onboard LPT controller [Disabled] No Configuration [Enabled] User Configuration [Auto] BIOS or OS chooses configuration
Mode	Output only Bi-directional EPP **ECP**	Set the mode for the parallel port using options Output only Bi-directional EPP ECP
Base I/O address	**378** 278	Set the base I/O address for the parallel port

Feature	Option	Description
	3BC	
Interrupt	IRQ 5 **IRQ 7**	Set the interrupt for the parallel port
DMA channel	DMA 1 **DMA 3**	Set the DMA channel for the parallel port
PS/2 Keyboard	Disabled **Enabled**	Enables or disables PS/2 Keyboard

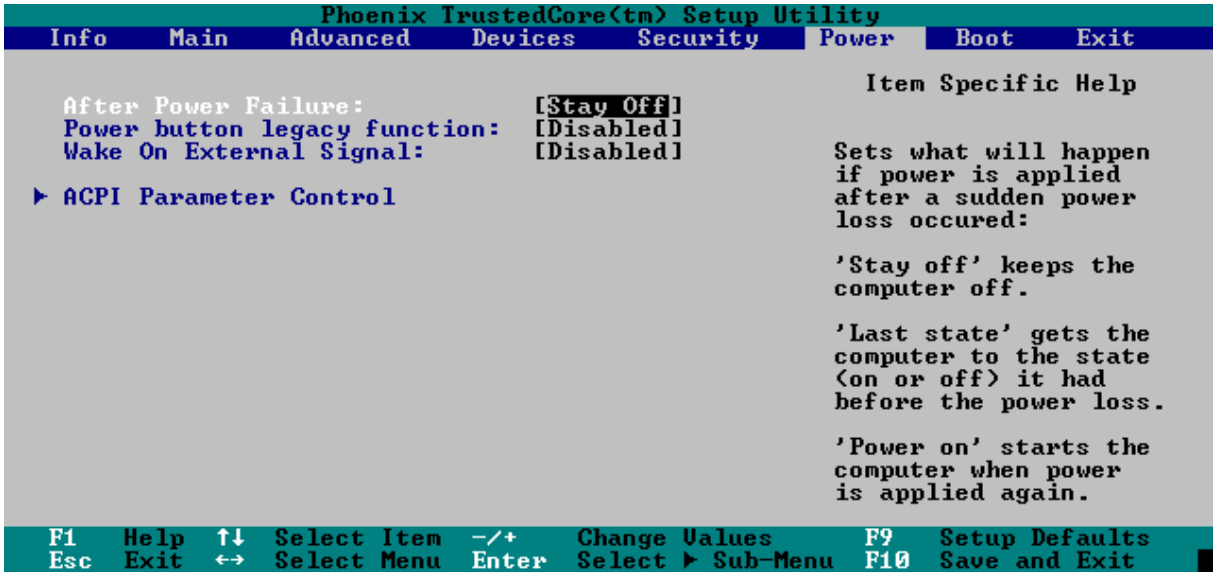
11.10 Security



Feature	Option	Description
TPM Support	**Disabled** Enabled	Enable Trusted Platform Module support
Set User Password		User Password to control access to the system at boot
Set Supervisor Password		Supervisor Password to control acces to the BIOS setup

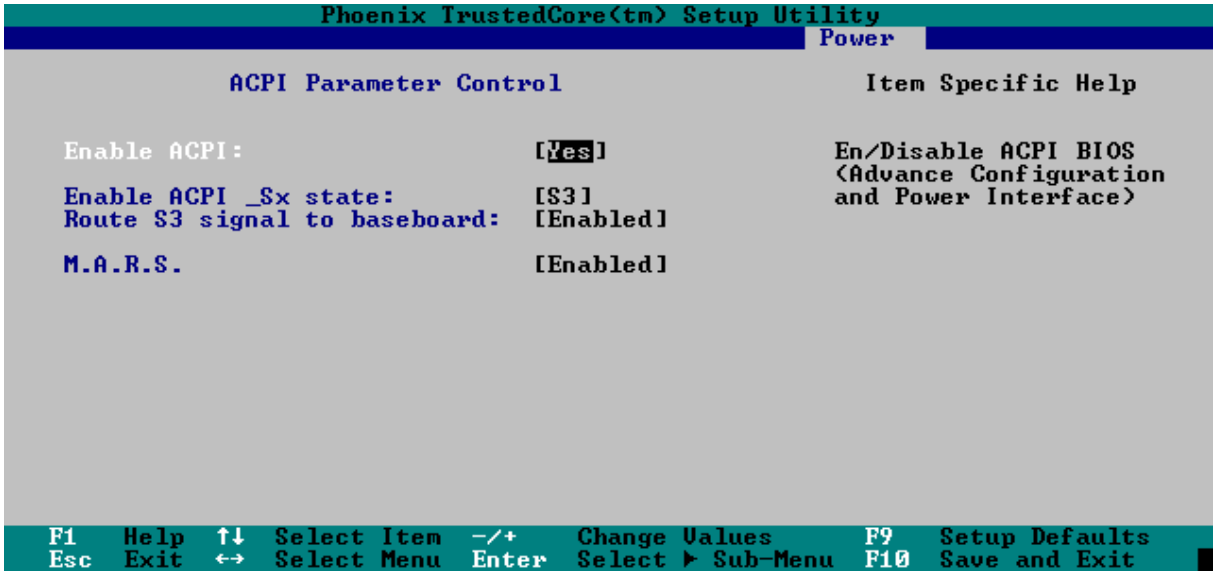
Note: This menu only appears, when a TPM device is available on the board

11.11 Power



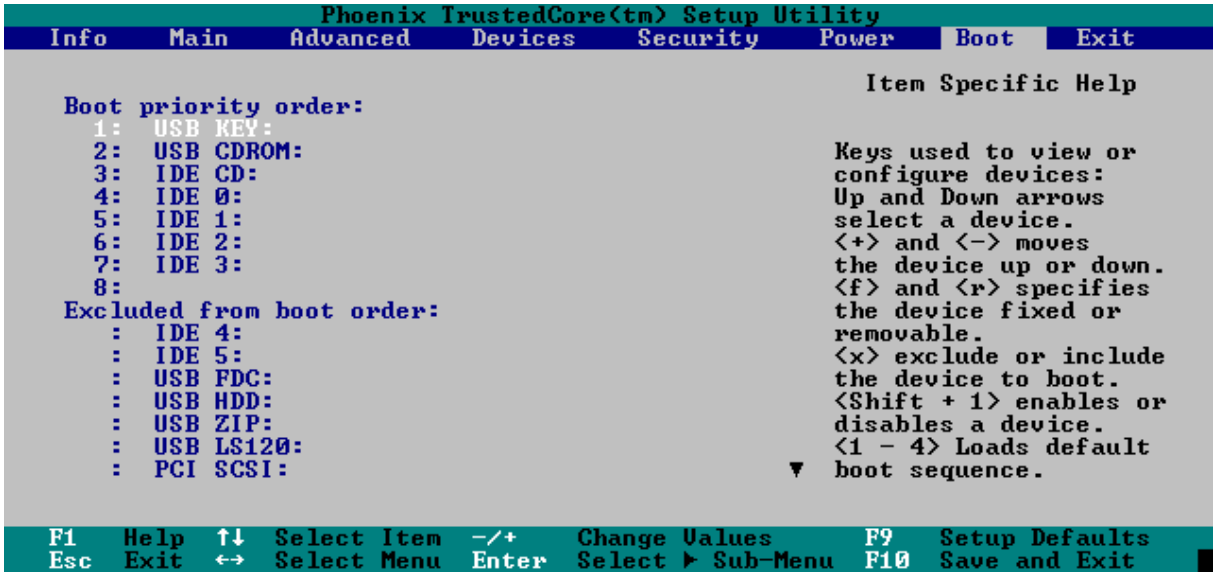
Feature	Option	Description
After Power Failure	**Stay Off** Last State Power On	Sets the mode of operation if an AC/Power Loss occurs. The two modes are: Enabled restores the previous power state before loss occurred, Disabled keep the power off until the power button is pressed. The Disabled choice turns off Resume on Modem Ring.
Power button legacy function	**Disabled** Enabled	This switch dis- and enables power button functions during POST and DOS
Wake On External Signal	**Disabled** Enabled	This option allows to enable or disable external wake-up via COM Express line WAKE1#

11.11.1 ACPI Parameter Control



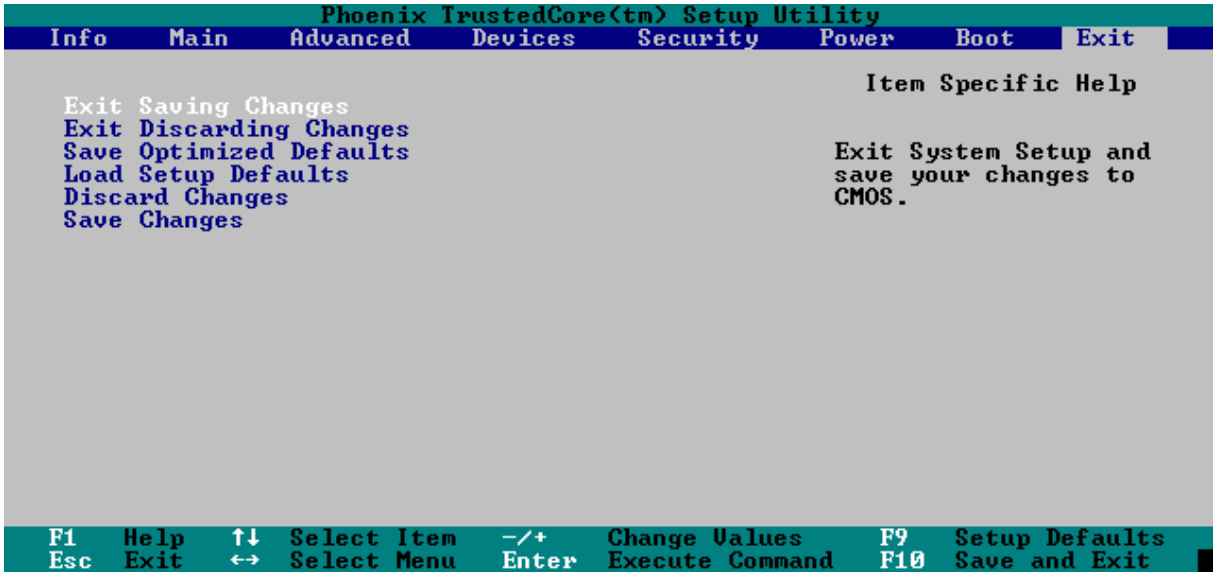
Feature	Option	Description
Enable ACPI	No **Yes**	En/Disable ACPI BIOS (Advance Configuration and Power Interface)
Enable ACPI _Sx state	None S1 **S3** S1+S3	This option allows to selectively enable Sx standby states for ACPI OS. Choosing 'Nono' will force the OS to have only S1, S4 and S5 states.
Route S3 signal to baseboard	Disabled **Enabled**	If S3_SUS is not routed to the baseboard then switching off main power is prevented. This will achieve shorter recovery time but higher power consumption. Please be sure your board supports the appropriate S3 state when making this choice
M.A.R.S.	**Disabled** Enabled	Enable/Disable support for the Kontron M.A.R.S. Smart Battery system. if enabled, the Smart Battery system will appear as an ACPI device and allow an ACPI aware OS to display and handle battery related information.

11.12 Boot



Feature	Option	Descpription
Boot priority order	1:USB Key 2:USB CDROM 3:IDE CD 4:IDE 0 5:IDE 1 6:IDE 2 7:IDE 3 8:	Keys used to view or configure devices: Up and Down arrows select a device. <+> and <-> moves the device up or down. <f> and <r> specifies the device fixed or removable. <x> exclude or include the device to boot. <Shift + 1> enables or disables a device. <1 – 4> Loads default boot sequence.
Excluded from boot order	IDE 4 IDE5 USB FDC USB HDD USB ZIP USB LS120 PCI SCSI	

11.13 Exit



Feature		Description
Exit Saving Changes		Exit System Setup and save your changes to CMOS.
Exit Discarding Changes		Exit utility without saving Setup data to CMOS.
Load Optimized Defaults		Load customer specific default values
Save Optimized Defaults		Save customer specific default values
Load Setup Defaults		Load default values for all SETUP items
Discard Changes		Load previous values from CMOS for all SETUP items
Save Changes		Save Setup Data to CMOS