Modular Computers®

CPCI Backplane Manual

PRODUCT DOCUMENTATION

PD10

CP6-BP8-H110

Reference ID: 24229 PD10
Revision: 01
Issued: March 01, 2002

The product described in this manual is in compliance with all applied CE standards.

Revision History

Manual/Product Title:	CPCI Backplane Manual: Product Documentation: CP6-BP8-H110
Reference ID:	24229 PD10

Rev. Index	Brief Description of Changes	Date of Issue
01	Initial Issue	Mar. 01, 2002

Imprint

Modular Computers ®

DISCLAIMER:

PEP Modular Computers GmbH rejects any liability for the correctness and completeness of this manual as well as its suitability for any particular purpose.

This manual was realized by: **TPD/Engineering, PEP Modular Computers GmbH**.

1. Introduction

The specific product description provided with this product documentation is part of the PEP's CPCI Backplane manual. For further information, in particular regarding general details as well as safety and warranty statements, refer to the CPCI Backplane Manual, ID 24229.

2. CP6-BP8-H110 DIN Type M Backplane with H.110 Connectivity

The main features of the 6U, 8-slot, DIN type M powered telephony backplane CP6-BP8-H110 are described in the following table:

Table 1: Distinctive Features of Backplane CP6-BP8-H110

Feature	Specification
Form Factor	6U
Size	222.51*262.05 mm
Number of Slots	8
Bus Resolution	P1/P2 on all slots: 64 bits
Bus Frequency	33MHz
Rear I/O Connectivity	P3 and P5 on all slots: general purpose P4 on slots 2 to 8: H110
Hot-Swap Capability	Yes
Power Supply Connector	DIN type M; ATX standard
Redundant Power Supply	Yes
Flexible Grounding Option	Yes
Fan Connector	Yes
MSD Connector	Yes
Power LED	Yes
PS-ON Connector	Yes
Reset Function Connector	—

3. Board Layout

Figure 1: CP6-BP8-H110 Board Layout (Front)

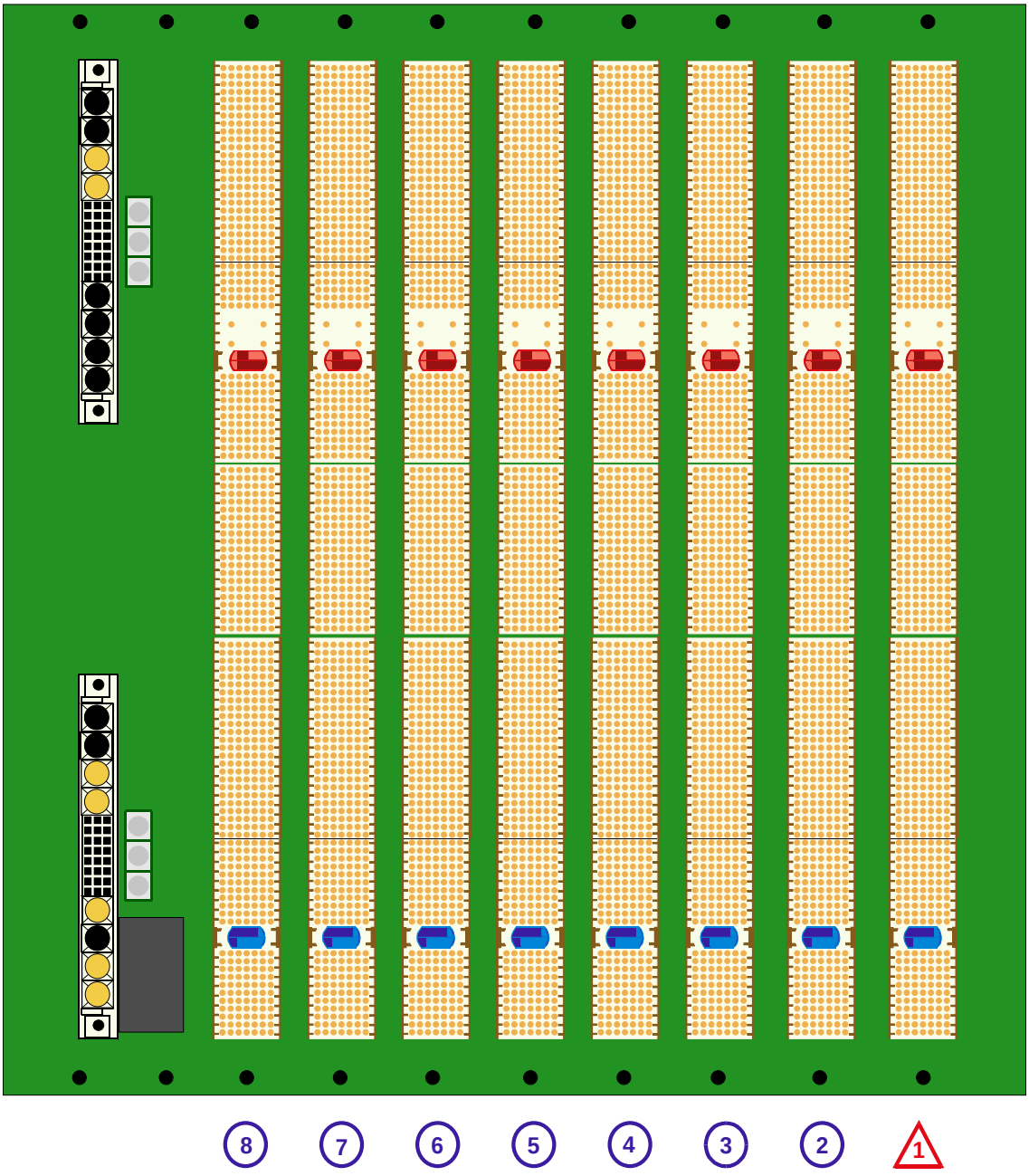
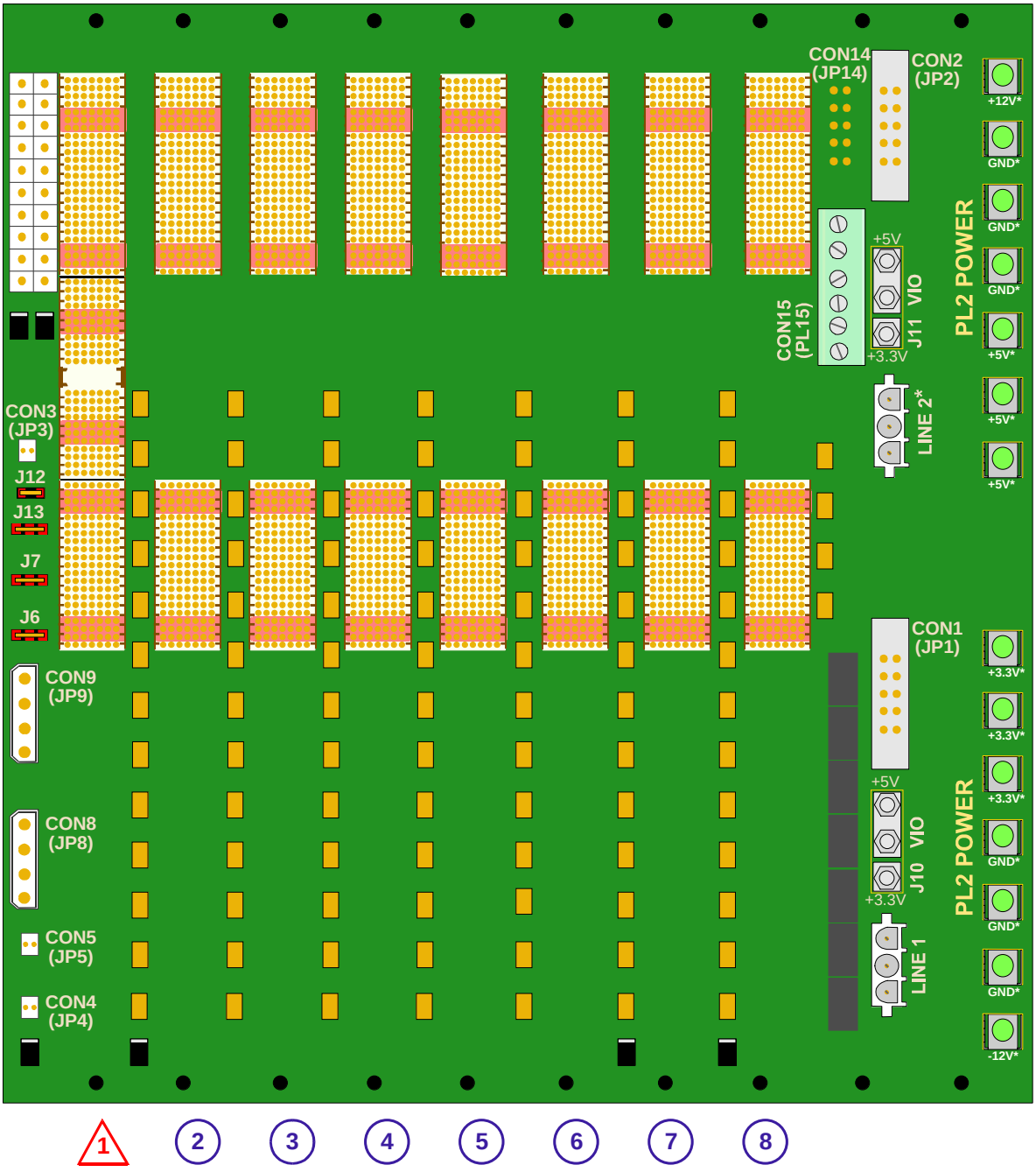


Figure 2: CP6-BP8-H110 Board Layout (Reverse)



Components marked with an asterisk (*) are optionally available.

4. Signalling Environment

4.1 V(I/O) Setting

For accommodating 3U and 6U power supplies there are two blocks of three high-current terminals (designated as V(I/O)) for connecting V(I/O) to either the +5V or +3.3V power supply. V(I/O) must be connected either to the +5V or the +3.3V input power. It is the responsibility of the system integrator to ensure that the required signalling voltage is implemented and that the backplane P1 connector coding corresponds to the implemented signalling voltage.

Warning!

Using both 3.3V and 5V boards within the same backplane segment may result in damage to your equipment. Please note that the presence of only one 5V board determines a 5V signalling environment. The default setting is 5V.

4.2 P1 Connector Coding for V(I/O)

The CompactPCI Specification foresees coding of the P1 connector to correspond to the signalling environment of the PCI bus. For this reason, only boards with universal or the corresponding coding can be physically inserted into the backplane. PEP's factory default setting for V(I/O) is +5V and male, 1567 code, brilliant blue coding keys are used.

Warning!

Using boards with an inadequate signalling voltage may result in damage to your equipment. Therefore, when changing the signalling environment from 5V to 3.3V or vice versa, it is mandatory that proper coding keys are used (refer to chapter 3 of the CPCI Backplane Manual, ID 24229, for details).

5. Interfaces

5.1 Line Connector

The power supply to the backplane is connected by means of the 3-pole Mate-N-Lok connector marked ”LINE1” on the reverse side of the backplane.

Figure 3: Orientation and Pinouts of CP6-BP8-H110 Connector LINE1

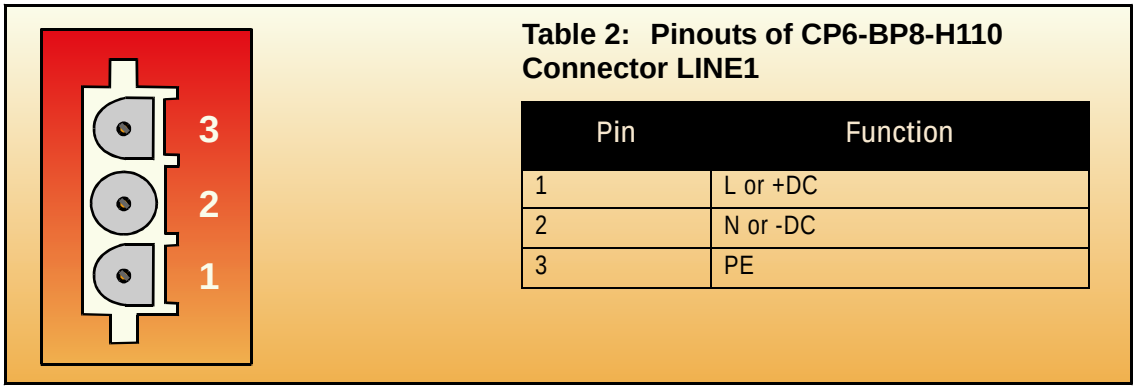


Table 2: Pinouts of CP6-BP8-H110 Connector LINE1

Pin	Function
1	L or +DC
2	N or -DC
3	PE

5.2 ATX Power Supply Connector

The main input power voltage is fed directly to the ATX power supply unit without any throughput via a backplane power supply connector. The power supply unit’s V1 ... V4 output power is distributed to the backplane by means of the 20-contact, male, Molex Mini-Fit Junior Connector ”ATX”.

Figure 4: Orientation and Pinouts of CP6-BP8-H110 ATX Connector

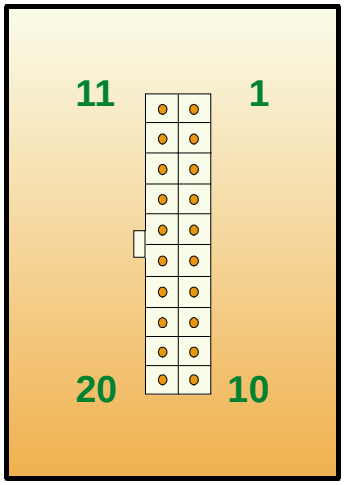


Table 3: ATX Connector Pinouts

Pin	Function	Pin	Function
1	+3.3V	11	+3.3V
2	+3.3V	12	-12V
3	GND	13	GND
4	+5V	14	PS_ON#
5	GND	15	GND
6	+5V	16	GND
7	GND	17	GND
8	PWR_OK	18	-5V
9	+5 VSB	19	+5V
10	+12V	20	+5V

5.3 Power Supply Connector

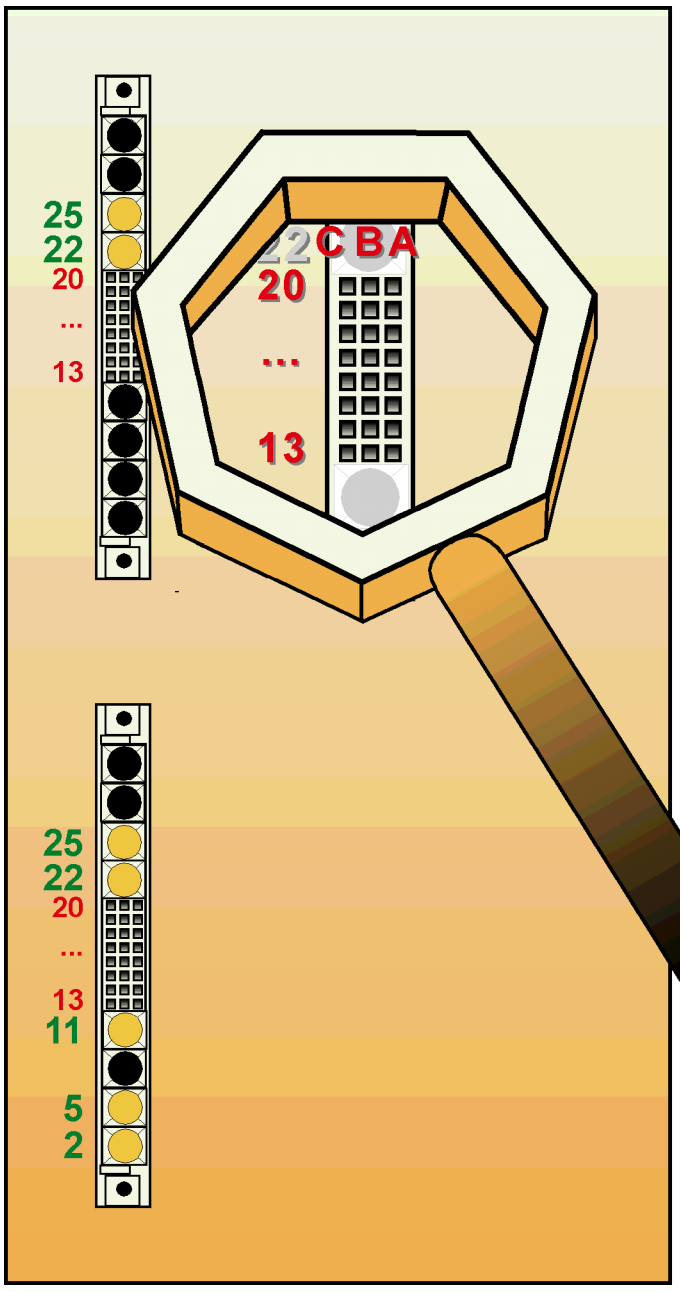


Figure 5: Orientation and Pinouts of CP6-BP8-H110 DIN Type M Power Supply Connector

The V_{EU} and V_{US} input voltages to the power supply unit and the V_{o1}...V_{o4} output voltages from the power supply unit to the backplane are connected via a 32-pole DIN type M female power supply connector.

Warning!

System integrators must ensure that only power supplies which comply with the pinout as provided in Table 4 are used with this connector!

Pins 2, 5, 28, and 31 do not comply with the CompactPCI Power Interface Specification.

Table 4: DIN Type M Upper and Lower Connector Pinouts

Pin	Function	Pin	Function
2	L or +DC*	B.17	+3.3V
5	N or -DC*	B.18	+3.3V
8	No Pin Loaded	B.19	+12V
11	PE*	B.20	-12V
A.13	Spare	C.13	EN#
A.14	INH#	C.14	DEG#
A.15	Current Share	C.15	FAL#
A.16	5V Sense -	C.16	+3.3V
A.17	5V Sense +	C.17	+3.3V
A.18	+3.3V	C.18	+3.3V
A.19	+12V	C.19	+12V
A.20	-12V	C.20	-12V
B.13	+3.3V	22	+5V
B.14	+3.3V	25	GND
B.15	+3.3V	28	No Pin Loaded * **
B.16	+3.3V	31	No Pin Loaded * **

** No pin loaded at upper DIN M24/8 power supply connector;*
*** No pin loaded at lower DIN M24/8 power supply connector*

5.4 Faston/M4 Terminals

In addition to ATX and DIN type M power connectors, this backplane can be provided with Faston/M4 type power terminals for use with non-pluggable power supplies. See Figure 2 for the location of each terminal.

5.5 Telecommunications Power Supply Connector

The 6-pole terminal block PL15 provides connection of the power supply circuits -SELVbat, VRG and -Vbat.

Figure 6: Orientation and Pinouts of CP6-BP8-H110 Terminal Block PL15

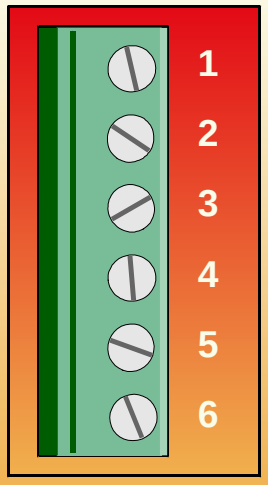


Table 5: Pinouts of CP6-BP8-H110 Terminal Block PL15

Pin	Function
1	-SELVbat
2	SELVbatRtn
3	VRG
4	VRGRtn
5	-VBat
6	VBatRtn

Note...

For details concerning the telecommunication connector pinouts please refer to the specifications of the boards connected to the H.110 bus.

5.6 Fan Connectors

The backplane is equipped with two lockable Molex male connectors, JP4 and JP5, for the connection of fans to the 12V power supply of the bus.

Figure 7: Orientation and Pinouts of CP6-BP8-H110 Connectors JP4 and JP5

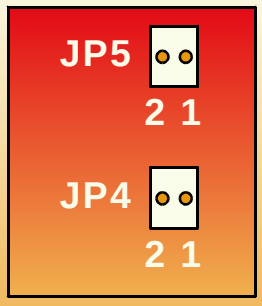


Table 6: Pinouts of CP6-BP8-H110 Connectors JP4 and JP5

Pin	Function
1	GND
2	+12V

5.7 MSD Connectors

Two 4-pole Molex male connectors, JP8 and JP9, are equipped on the backplane for the connection of mass storage devices (drives) to the +5V/+12V power supply of the bus.

Figure 8: Orientation and Pinouts of CP6-BP8-H110 Connectors JP8 and JP9

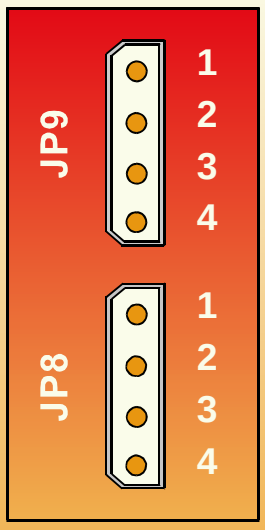


Table 7: Pinouts of CP6-BP8-H110 Connectors JP8 and JP9

Pin	Function
1	+12V
2	GND
3	GND
4	+5V

5.8 Power LED Connector

The 3-pole 2.54 mm pin-row male connector JP6 offers the possibility of connecting a ”Power ON/OFF” LED. The connector pinouts are identical to those of PC connectors customary in trade. Voltage is supplied by the +5V line.

Note...

By default, the power supply line is equipped with a resistor that is serially connected to the LED. Such a resistor is necessary to protect the LED from possible overcurrents.

Figure 9: Orientation and Pinouts of CP6-BP8-H110 Connector JP6

Table 8: Pinouts of CP6-BP8-H110 Connector JP6

Pin	Function
1	GND
2	N/C
3	+5V

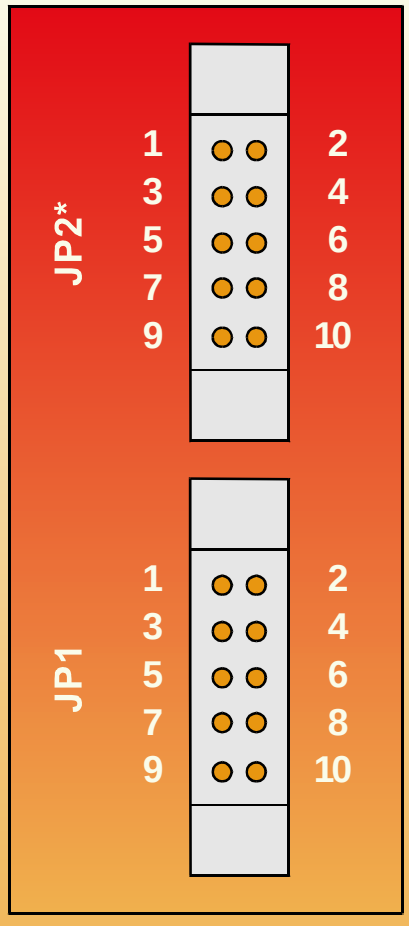
5.9 Auxiliary Signal Connectors

The connection of the auxiliary signals is accomplished by means of the two 10-pole LPV female connectors JP1 and JP2.

Note...

When using an ATX power supply unit its auxiliary signals must be connected to the auxiliary signals of the PCI bus.

Figure 10:Orientation and Pinouts of CP6-BP8-H110 Connectors JP1 und JP2



**This connector is available optionally.*

Table 9: Pinouts of CP6-BP8-H110 Connectors JP1 und JP2

JP1		JP2	
Pin	Function	Pin	Function
1	GND	1	GND
2	EN#1[1]	2	EN#2
3	GND	3	GND
4	INH#1	4	INH#2[3]
5	DEG#1[2,3]	5	DEG#2[3]
6	FAL#1[2,3]	6	FAL#2[3]
7	GND	7	GND
8	PRST#1[3]	8	PRST#2[3]
9	GND[4]	9	GND[4]
10	+5V[4]	10	+5V[4]

Legend:

[1] ATX power supply unit: The signal PS-ON (ATXPWR.14) is connected to EN#1 via the jumper BR1 normally closed.

[2] ATX power supply unit: The signal PS-OK (ATXPWR.8) can be connected via the 3-pole jumper JP7 either to FAL#1 or DEG#1 (see also section "Jumper Setting").

[3] Also in system slot.

[4] Also sense down.

Note...

Inserting a 0-ohm resistor at the location marked on the board with EN#1 the signals EN#1 of the power supply unit can be connected permanently with GND. Thus, enabling the power supply unit can be forced by default.

5.10 Power Supply Remote Enabling

The Molex male connector JP3 has a double function. It can be used as a power supply remote enable connector or, if bridged, as a wire jumper. If used as a connector, JP3 offers the possibility of remote ON/OFF via an external power supply enable switch.

Figure 11: Orientation an Pinouts of CP6-BP8-H110 Connector JP3

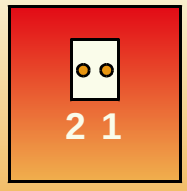


Table 10:Pinouts of CP6-BP8-H110 Connector JP3

Pin	Function
1	GND
2	PS_ON#

If JP3 is used as a wire jumper, the remote ON/OFF commuting is accomplished by closing JP3. No external power supply enable switch is required in this case.

5.11 Shelf Enumeration Assignment

The 10-pole double pinrow connector JP14 is used to assign a shelf enumeration address to indicate the location (shelf) of the backplane within a system of CompactPCI sub-systems. The address is 5-bits binary coded where SGA0 is the least significant bit, and it is implemented by either jumpering the associated pins to create a logic 0 or by not jumpering to create a logic 1.

Figure 12: Orientation an Pinouts of CP6-BP8-H110 Connector JP14

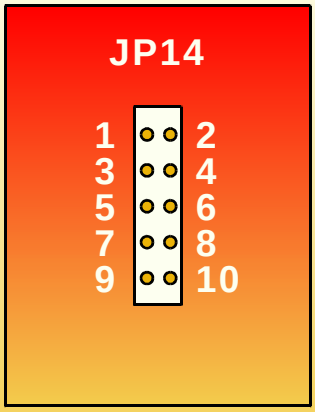


Table 11:Pinouts of CP6-BP8-H110 Connector JP14

Pin	Function	Pin	Function
1	SGA0	2	GND
3	SGA1	4	GND
5	SGA2	6	GND
7	SGA3	8	GND
9	SGA4	10	GND

6. Jumper Settings

The CP6-BP8-H110 backplane is provided with the following jumpers. The function of these jumpers can be described as follows:

- External power supply enabling (BR1, JP3) with 0-ohm resistor EN#1 open;
- Select the power supply status signal to be routed to the H.110 bus (JP7).

The jumper settings are described in the following tables:

Table 12:Settings of CP6-BP8-H110 Jumpers BR1 and JP3

Function	BR1	JP3
Not supported	Open	Open
	Open	Closed
Power supply OFF	*Closed*	*Open*
Power supply ON	Closed	Closed

Default settings in italics.

The control signal to enable power supply is available additionally on connector JP1 (pin 2).

Table 13: Settings of CP6-BP8-H110 Jumper JP7

JP7	Function
1-2	FAL# routed to H.110 bus
1-3	DEG# routed to H.110 bus
Jumper not set	*No routing to H.110 bus*

Default settings in italics.

7. CompactPCI as a Telecom Platform

The integration of computers and telecommunications has enabled a wide range of new communication applications and has fueled an enormous growth in communications markets. A key element in the development of computer-based communications equipment has been the addition of an auxiliary telecom bus to existing computer systems. Most manufacturers of high-capacity computer-based telecommunications equipment have incorporated such a telecom bus in their systems. Typically these buses transport and switch nx64 kBaud low-latency communications traffic between boards within the computer, independent of the computer's I/O and memory buses.

The Telecom Interest Sub-Committee (TISC) of PICMG defined the capabilities and utility of the CompactPCI 6U-based system achitecture to support the application needs of the computer telephony (CT) industry. Key features include the H.110 backplane TDM bus which incorporates the ECTF´s (**Enterprise Computer Telephony Forum**) H.100 bus and hot swap, rear panel analog and digital PSTN connections, telco power and ground as well as physical keying of boards.

The collaborative effort of TISC has resulted in a rugged industrial chassis with well-established mechanical specifications, extremely robust metric connectors and provisions for special telecom voltages, busses and I/O connectors on the backplane. In short, CompactPCI provides all of the advantages of a hot swap industrial computer chassis while retaining compatibility with all desktop software.

The objective of the H.100/H.110 CT Bus specification is to provide a single telecom bus for the entire industry. To facilitate its adoption, the H.100 CT Bus specification was initially targeted at PCI form-factor boards. The H.110 CT Bus specification, is targeted at CompactPCI form factor products. The H.110 specification is functionally identical to the H.100 specification. However, some of the features in H.100 relating to high availability realize their full utility only in the hot swap CompactPCI environment. There are electrical differences between H.100 and H.110 due to the differences between a ribbon cable and a backplane implementation.

Finally the H.110 CT Bus has been designed with more capacity than any of the previously deployed buses, so as to support the next generation of high capacity servers. At the same time, CT Bus includes well-defined subsets so that economical low-end systems can be built involving as few as two boards.

For detailed information on CT Bus systems please refer to the ECTF H.110 Hardware Compatibility Specification for the CT Bus, Revision 1.0. Additional useful information relevant to computer-based telecommunications in the CompactPCI environment can be found in the PICMG CT Specification, edition 2.5, and in the PICMG Hot Swap Specification, edition 2.1, release 1.0.

For further information on the H.110 coding keys refer to chapter 3.5 of the CPCI Backplane manual, ID 24229.

This page was intentionally left blank.