ePCI-100

Celeron – Pentium III SBC with D V I

Technical Reference Manual
Version 1.3, February 2003

Note: The latest releases of the Technical Reference Manuals are available at:
ftp://ftp.kontron.ca/support/Product_manuals/

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ePCI-100 – Technical Reference Manual

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ADDITIONAL COMMENTS

FCC Compliance Statement
Warning

Changes or modifications to this unit not expressly approved by the party responsible for the compliance could void the user's authority to operate this equipment.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his or her own expense.

European Statement

Warning

This is a class B product. If not installed in a properly shielded enclosure, and used in accordance with the instruction manual, this product may cause radio interference in which case the user may be required to take adequate measures at his or her own expense.

Safety Standard

UL Recognized Component, File # E186339 Vol. 1 Section 2

Care and handling precautions for Lithium batteries

- Do not short circuit
- Do not heat or incinerate
- Do not charge
- Do not deform or disassemble
- Do not apply solder directly
- Do not mix different types or partially used batteries together
- Always observe proper polarities

READ ME FIRST

Your computer board has a standard non-rechargeable lithium battery. To preserve the battery lifetime, **the battery enable jumper is removed when you receive the board.**

EXERCISE CAUTION WHILE REPLACING LITHIUM BATTERY

WARNING

Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type of battery recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

ATTENTION

Il y a danger d'explosion s'il y a remplacement incorrect de la batterie.

Remplacer uniquement avec une batterie du même type ou d'un type équivalent recommandé par le fabricant. Mettre au rebut les batteries usagées conformément aux instructions du fabricant.

ACHTUNG

Explosionsgefahr bei falschem Batteriewechsel. Verwenden Sie nur die empfohlenen Batterietypen des Herstellers. Entsorgen Sie die verbrauchten Batterien laut Gebrauchsanweisung des Herstellers.

ATENCION

Hay un peligro de explosion sido la pila no ha si bien remplazada. Remplace la pila con el mismo tipo o con aquellas recomendadas por el fabricante. Para desacerce de las pilas usadas, siga las instructiones del fabricante.

POWERING-UP THE BOARD

If you should encounter a problem, verify the following items:

Make sure that all connectors are properly connected.

Check your boot diskette.

If the board still does not start up properly, you should try booting your system with the ePCI-100 installed in the system, a monitor and a mouse connected to the board. This is the minimum required to verify the board's operation.

If you still are not able to verify your board, please refer to the emergency Procedure in the Appendix Section.

If you still are not able to get your board up and running, contact our Technical Support department for assistance (see Appendix G, Getting Help).

ADAPTER CABLES

While adapter cables are provided from various sources, the pinout is often different. The direct crimp design offered by Kontron allows the simplest cable assembly. All cables are available from Kontron Sales Department.

UNPACKING AND SAFETY PRECAUTIONS

Static Electricity

Since static electricity can cause damage to electronic devices, the following precautions should be taken:

1. Keep the board in its anti-static package, until you are ready to install it.
2. Always touch a grounded surface or wear a grounding wrist strap before removing the board from its package; this will discharge any static electricity that may have built up in your body.
3. Handle the board by the edges.

Storage Environment

Electronic boards are sensitive devices. Do not handle or store devices near strong electrostatic, electromagnetic, magnetic or radioactive fields.

Power Supply

Before any installation or setup, ensure that the board is unplugged from power sources or subsystems.

Unpacking

Follow these recommendations while unpacking:

1. After opening the box, save it and the packing material for possible future shipment.
2. Remove the board from its anti-static wrapping and place it on a grounded surface.
3. Inspect the board for damage. If there is any damage or missing items, notify Kontron immediately.

When unpacking you will find:

1. One ePCI-100 SBC.
2. One Quick Reference sheet.
3. One DVI to VGA adapter.
4. One CDROM containing drivers.
5. One Cable Kit.

1 PRODUCT OVERVIEW

2 BOARD FEATURES

3 INSTALLING THE BOARD

APPENDICES

PART 1

1 PRODUCT OVERVIEW

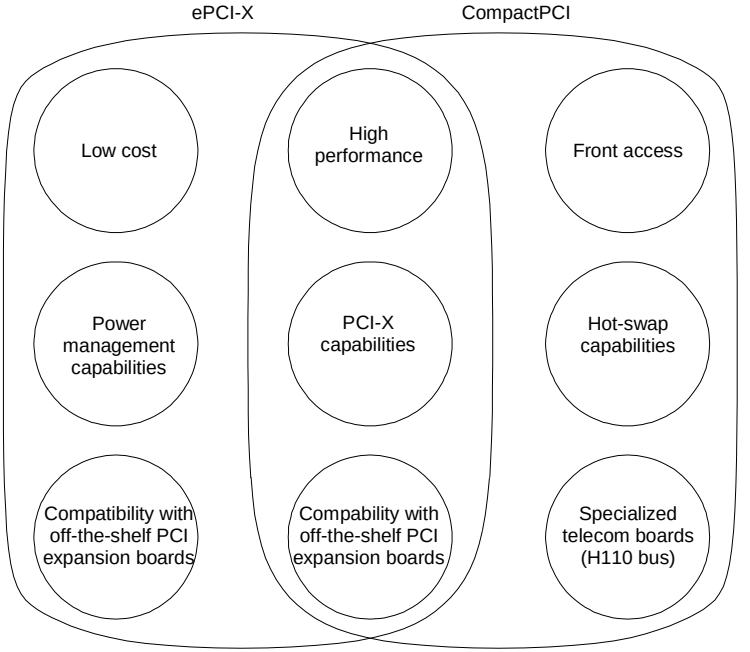
1. INTRODUCTION
2. ePCI-100 SBC TECHNICAL SPECIFICATIONS
3. POWER REQUIREMENTS

1.1 Introduction

The ePCI-100 (Embedded PCI) is a state-of-the-art LOW POWER PCI half-size Intel 82810E based Single Board Computer and is an addition to the current VIPer product line. It is a major change to the VIPer family since this board supports PCI only rather than ISA bus expansion. This board addresses the embedded board market as a high-performance engine with PCI Mezzanine expansion support and connectivity of digital displays using a DVI (PanelLink®) interface.

As bandwidth-intensive applications continue to increase, Kontron's ePCI-100 offers the latest in processing power with an Intel® Pentium® III processor at 866MHz clock speed which is integrated into a single slot, low profile SBC to meet the critical requirements for more power in less space. Other essential features include up to 512MB of SDRAM, two 10Base-T/100BaseTx Ethernet interfaces, two USB ports, and CPU/Board monitoring. The ePCI-100 is capable of supporting a comprehensive range of OSs, including Windows® NT 4.0/98/2000, QNX™, Linux, and FreeBSD.

The purpose of the ePCI-100 is to provide an upgrade path for ISA enclosure and fill the market gap between motherboards and CompactPCI systems. CompactPCI is a reliable board but there are still a lot of applications where the cPCI is not the right solution, i.e., cost sensitive application and applications requiring standard PCI expansion boards or power management capabilities.



ePCI-X and CompactPCI Comparison

On the expansion boards side, most functions are now available with a PCI interface. PCI front-end chips, FPGA, cores, and even CPLD free softcores are available to make custom high-performance specialized expansion boards as well as very simple I/O expansion boards.

The need for the ISA bus is fading away even in the most traditional sectors.

1.2 ePCI-100 SBC Technical Specifications

FEATURES	DESCRIPTIONS
CPU	Celeron® processor – Low-Power 566, and 733 MHz (bus speed at 66MHz) Pentium III processor - 600/700/850MHz (bus speed at 100MHz) Pentium III processor - 733/866MHz (bus speed at 133MHz) Note: Will feature higher speeds when CPU available
Chipset	Intel 82810E
Cache	128KB Instruction / Data CPU-internal Level 1 256KB Advanced Transfer Cache (64-bit wide on-die full speed Level 2 pipelined burst)
Data Path	64-bit on CPU and video memory; 32-bit on local PCI
Memory	Two 144-pin SDRAM SODIMM supports (long/1.25", short/1") memory configurations up to 512MB Standard 3.3V single-sided or double-sided SODIMMs (requires PC100 SDRAM)
Bus Interfaces	Front Side Bus 66MHz/100MHz/133MHz determined by CPU PCI Bus, 32-bit 33MHz SMBus

ePCI-100 SBC Technical Specifications (continued)

FEATURES	DESCRIPTION
Flash Memory	4KB Serial EEPROM for user configuration Silicon Serial ID TAG for unique board identification accessible via software
Video	Integrated 2D/3D 64-bit CRT video controller with DVI output CRT resolutions up to 1600x1200x64K colors, non-interlaced No direct flat panel support (must go through DVI connector) Compatible with CGA, EGA, Hercules, MDA, VGA, SVGA, XGA, and SXGA
Clock/Calendar	Real-time clock with (replaceable) battery backup 256-byte CMOS RAM
I/O	**Super I/O Controller :** LPC47B27X **USB Port** : Two (Version 1.1) **Serial Ports** : Two (COM1: RS-232, COM2: Configurable as RS-232/422/485) **Parallel port** : One bi-directional with all IEEE 1284 protocols supported, BIOS selectable IRQs and addressing **Floppy Disk** : Support for one drive (360KB to 2.88MB) **EIDE** : Two Enhanced IDE interfaces; support for two IDE drives (master/slave configuration); PIO Mode 0-4 and Ultra DMA/66 **Ethernet** : Two Intel 82559ER Ethernet controllers, PCI10/100Base-TX ports **Multifunction** : PS/2 mouse, AT and PS/2 standard keyboard, speaker, reset switch and hard disk/Power LEDs **CompactFlash™ Module**: Optional bootable CompactFlash™ disk interfaces to secondary EIDE channel, user upgradeable, master/slave

ePCI-100 SBC Technical Specifications (continued)

FEATURES	**DESCRIPTIONS**
BIOS Features	Phoenix BIOS in Firmware Hub with recovery code. Save CMOS in Flash option and Boot from LAN capability. CC000-E0000 address blocking; PnP tables Setup console redirection to serial port (VT100 mode) with CMOS setup access Software enable/disable of onboard Ethernet; hardware enable/disable of onboard video Diskless, keyboardless, and videoless operation extensions Programmable I/O wait states Advanced security feature for floppy and HDD; DMI & HDD S.M.A.R.T. support Intelligent System Monitoring (chassis intrusion and advanced thermal management such as resume, overheat alarm and auto slow down) Green support
Supervisory	Dual-stage software programmable Watchdog timer drives NMI on first stage and system reset on second stage Time out from 31ms to 4:22 min Programmable CPU temperature monitor alarm Board temperature sensor Power failure and voltage monitoring/low battery detector Hardware system monitor for system voltages, temperature, fan speed, and “cover open” discrete input, accessible via on-board SMBus LEDs: IDE activity(debug LED), Ethernet activity and link status Voltage monitoring of 5V, 3.3V , 12V, VBAT and Vcore voltage rails System monitor connector to provide board health status, and to monitor external fan and system fault discrete inputs.
OS Compatibility	Windows® 98/2000, Windows® NT 4.0, QNX™, Linux, and FreeBSD
Form Factor (Standard ePCI)	122 x 185 x 50.8 mm (4.8” x 7.3” x 2”) at CPU fan.

ePCI-100 SBC Technical Specifications (continued)

FEATURES	DESCRIPTIONS
Environmental	**Operating** / **Storage and Transit** Temp. 0-55°/32-131°F (w/ 150LFM airflow) / -40° to +70° / -40° to 158°F **When using a CompactFlash disk, must not exceed 50°C (0-50°C/32-122°F)** Humidity 5% to 95% @ 40°C/104°F non-condensing / 5% to 95% @ 40°C/104°F non-condensing Altitude 4,572m / 15,000ft / 15,240m / 50,000ft Shock 5G, each axis Vibration 1.5G, each axis
Reliability	MTBF: > 75,000 hours 55°C/131°F (MIL-HDBK-217F) Unique silicon serial number accessible via software USB, keyboard and mouse voltage protected by self-resetting fuses 2 year limited warranty
Safety	Designed to meet or exceed UL 1950; CSA C22.2 No 950; EN 60950; IEC950
EMI/EMC	FCC 47 CFR Part 15/CISPR22, Class B; CE Mark to EN55022/EN50082

1.3 Power requirements

The power requirements for the ePCI-100 are specified as follows:

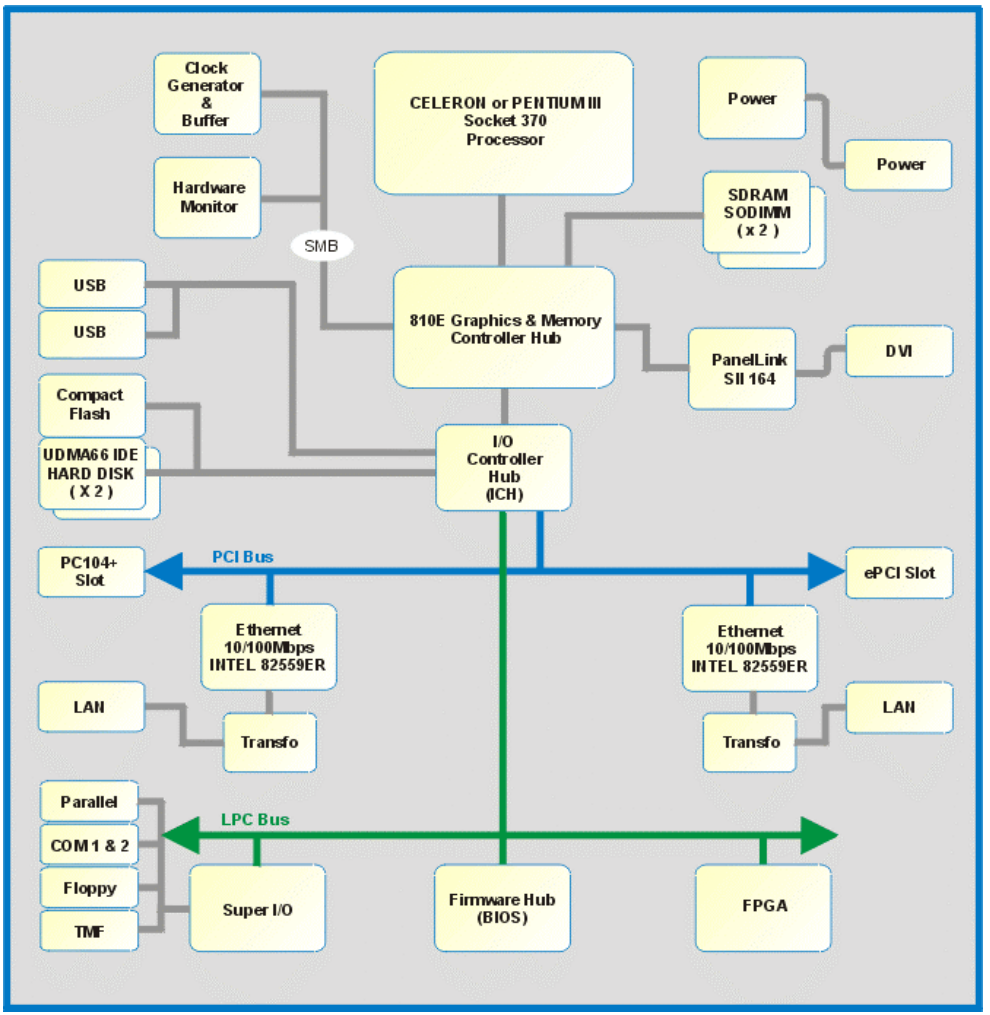
		CELERON 733	PENTIUM 850	
OS	**Supply Voltage**	**Current (amps)**	**Current (amps)**	**Remarks**
DOS	VCC5	2.47	3.02	All tests done with two banks of SODIMM (512MB RAM)
	VCC3.3	2.80	2.90	
	+12V	0.14	0.14	
WIN98	VCC5	0.42	0.42	
	VCC3.3	2.36	2.54	
	+12V	0.14	0.14	
Kpower	VCC5	4.36	5.34	
	VCC3	2.30	2.36	
	+12V	0.14	0.14	

PART 2

2 BOARD FEATURES

1. BLOCK DIAGRAM
2. SYSTEM CORE
3. MEMORY
4. BATTERY
5. SUPERVISORY FEATURES
6. POWER SUPPLY
7. I/O DEVICES
8. STORAGE

2.1 Block Diagram



2.2 System Core

2.2.1 Processors

Celeron® and Pentium® III Processors

The ePCI-100 may be equipped with one of the following Intel processors:
Celeron ranging speed from 566 to 733MHz,
Pentium III ranging speed from 600 to 866MHz

Related Jumpers

None

BIOS Settings

None

CAUTION
Since CPUs are very sensitive components, particular attention should be given while installing a processor on the board.

Improper installation may damage the board and/or the CPU.

Before changing or installing a processor on your board, **you must contact our Technical Support** for the installation procedure (see Appendix G, Getting Help).

2.2.2 Chipset

The ePCI-100 uses the Intel's 82810E Chipset. Here are the main highlights:

Highly integrated chipset

Integrated 2D/3D video engine

Integrated RAMDAC

Support Celeron® or Pentium® III

66MHz up to 133MHz host bus

Memory

PC100 SDRAM interface

Up to 512MB on two SO-DIMMs

Support 32MB/64MB/128MB/256MB/512 technology

USB

Support 2 USB ports

Firmware Hub

1MBytes Firmware Hub (Flash BIOS) on LPC bus

Super IO

Super IO on LPC bus

Flat Panel

Support Panel Link (DVI) Flat Panel via DVO port

The Intel® 82810E Chipset architecture also enables a new security and manageability infrastructure through the Firmware Hub component. It also removes the requirements for the ISA expansion bus that was traditionally integrated into the I/O subsystem of PCIsets

The Intel 82810E Chipset contains three core components

The Graphics and Memory Controller Hub (GMCH)
The I/O Controller Hub (ICH)
The Firmware Hub (FWH) also referred as BIOS

The GMCH integrates a 66/100/133 MHz bus controller, integrated 2D/3D graphics accelerator, 100MHz SDRAM controller and a high-speed hub interface for communication with the ICH. The ICH integrates an Ultra ATA/33 or Ultra ATA/66 (ICH) controller, USB host controller, LPC interface controller, FWH interface controller, PCI interface controller, and a hub interface for communication with the GMCH.

2.2.2.1 The GMCH

The GMCH provides the interconnect between the SDRAM and the rest of the system logic:

- 421 MINI BGA
- Integrated Graphics controller
- 230MHz RAMDAC
- Support for Intel® Celeron™ or Pentium® III processors with a 66MHz, 100MHz or 133MHz system bus
- 100MHz SDRAM interface supporting up to 512MB SDRAM
- Downstream hub interface for access to the ICH
- TVout/Flat Panel Display support (DVI)

2.2.2.2 The Controller Hub (ICH)

The I/0 Controller Hub provides the I/O subsystem with access to the rest of the system:

241 Mini BGA
Upstream hub interface for access to the GMCH
PCI 2.2 interface
Bus Master IDE controller – supports two Ultra DMA/66 IDE (ICH)
USB controller
SMBus controller
FWH interface
LPC interface
Integrated System Management Controller
IRQ controller

2.2.2.3 The Firmware Hub (FWH)

The FWH component is a key element to enabling a new security and manageability infrastructure for the PC platform. The device operates under the FWH interface and protocol. The hardware features of this device include:

An integrated hardware Random Number Generator (RNG)
Register-based locking
Hardware-based locking
Main BIOS

2.3 Memory

2.3.1 SDRAM System Memory

The ePCI-100 supports two industry standard 144-pin SODIMMs (Small Outline Dual Inline Memory Module) sockets for memory configuration from 32MB to 512MB of Synchronous DRAM.
The memory characteristics must conform to the following:

- 1.25 inch height (long) or 1 inch height (short), 144-pin SODIMM
- Standard 3V
- 64-bit modules, single-sided or double-sided
- Unbuffered 100MHz SDRAM
- Serial Presence Detect (SPD) EEPROM.

For the latest list of tested DIMMs devices please consult our FTP site at :

ftp://ftp.kontron.ca/Support/Product_Memory_AVL_Approved%20Vendor%20List/

2.3.2 SODIMM Installation

> **NOTE**
> If a Mezzanine card is installed, it must be removed before installing SODIMMs.

To install the SODIMMs in the sockets, proceed as follows:
With the board flat on the table, turn it so that the faceplate is facing you.
Hold the module vertically so that the bottom connector key is at right. Install the SODIMM into the socket. The keys of the socket will ensure a correct mating.
Press firmly on the top edge of the memory module to engage it into the socket. The module is fully inserted when the retaining clips snap into notches located at each end of the module.
To remove the SODIMMs from the sockets, press simultaneously on the retaining clips located on each side of the socket. Once the module has snapped out, pull gently on it.

WARNING

Since static electricity can cause damage to electronic devices, the following precautions should be taken:
Keep the board in its anti-static package, until you are ready to install it.
Touch a grounded surface or wear a grounding wrist strap before removing the board from its package; this will discharge any static electricity that may have built up in your body.
Handle the board by the edges.

2.4 Battery

An onboard 3.6V lithium battery is provided to backup BIOS setup values and the real time clock (RTC).
When replacing, the battery must be connected as follows:

NOTE

The board is shipped with W7 (on board enable/disable battery jumper) not installed. Please install this jumper prior to run the ePCI-100.
Running the board without installing W7 will cause a CMOS memory error.

WARNING

Danger of explosion if battery is incorrectly replaced
Replace only with the same or equivalent type of battery recommended by the manufacturer. Dispose of used batteries according to the instructions of the manufacturer.

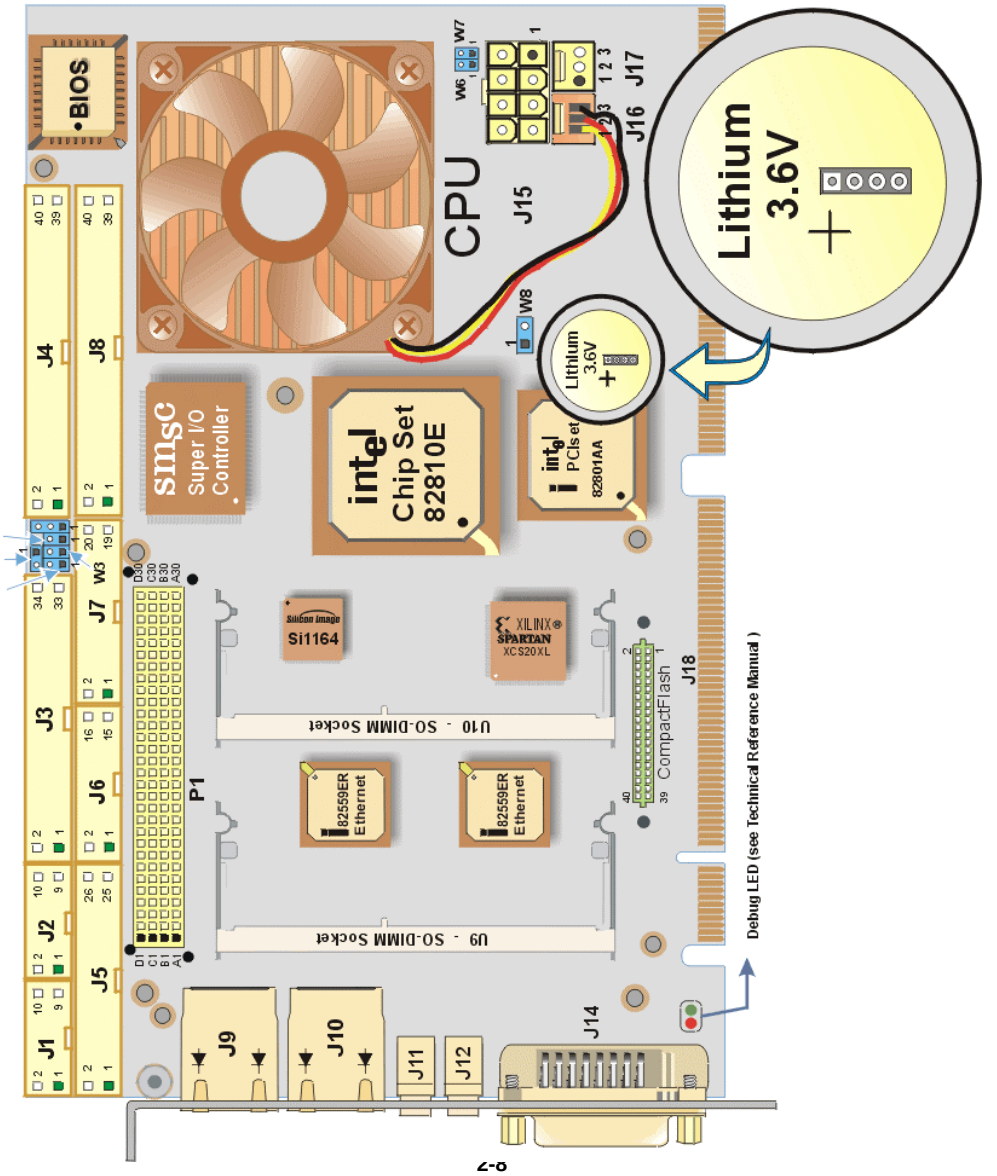
Prior to first powering the board, the battery must be connected using the W7 Battery jumper.

The battery specifications are as follows: 3.6V Lithium battery, 0.37A/h

Related Jumpers	
W 6	Battery connection
Related Connectors	
BT1	Polarized battery holder

2.4.1 Installation

Connect the battery to the BT1 header. The positive terminal of the battery holder is located at the bottom center.



2.5 Supervisory Features

The ePCI-100 provides a set of programmable I/O registers to setup the ICH (I/O addresses 4030h to 4037h) and the XILINX FPGA (I/O addresses programmable at 190h-197h, using the Phoenix Chipset Features Setup).
Only register bits needed to program the power fail detection and watchdog functions are described below.

2.5.1 Power Fail Monitoring

The status of the power failure detector can be read from one bit of the system register located at the address 191h Bit 0. The detection conforms to the following conditions (* = active low signal):
The board always monitors the 3.3V power supply. When it drops below 3.3v±5% (typical), the system is reset.

The board monitors the onboard battery. When the battery is in a low condition (below 2.9V typical). An interrupt handler can then service the interrupt. If you choose not to generate a SMI, you can use an algorithm to detect a low-battery condition and respond accordingly.
For more information, contact the Technical Support department (see Appendix G)

2.5.2 Watchdog

The function of a watchdog is to reset the CPU board if the processor is not able to generate a trigger for longer than the watchdog time-out period. This feature is useful in embedded systems where human supervision is not required or impossible.

The ePCI-100 provides a two-stage digital watchdog with software programmable time-out period.

Following a reset of any source, the watchdog is disabled. The watchdog can be enabled by software.

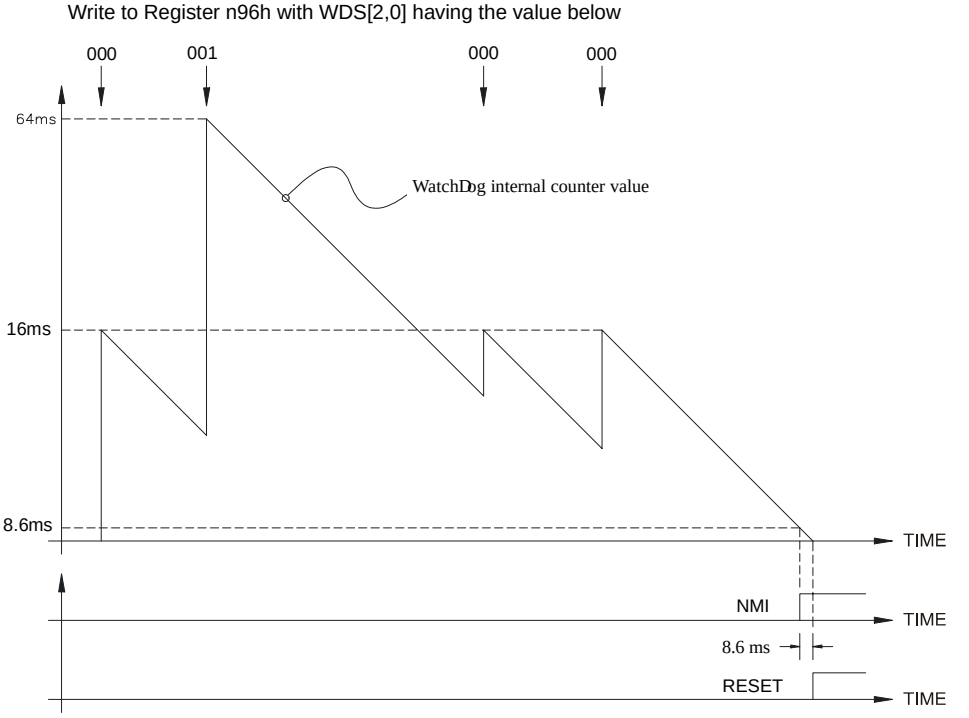
Dual Stage Watchdog

Enabling the Programmable Watchdog
To enable the programmable watchdog, first unlock the enable bit by clearing the lock bit in register 192h (bit 2), then set the bit WDEN (bit 7) in register 196h and relock it by setting the lock bit in register 192 (bit 2). The following is an example in C language:

```
#define TekReg 0x190                    // define base address (0x190)
void ArmWatchdog(void)
{
outp(TekReg+2,  inp(TekReg+2) & 0xFB);          // unlock watchdog enable bit
outp(TekReg+6,  inp(TekReg+6) | 0xF0);          // enable and trigger at max time-out
outp(TekReg+2,  inp(TekReg+2) | 0x04);          // lock watchdog enable bit
}
```

Triggering the Programmable Watchdog
To trigger the programmable watchdog, the processor writes to register 196h. The action of writing to the register is the trigger and the value written to the register tells the watchdog the current time-out to use (see register 196h description). For a fixed time-out, the software simply writes a constant in register 196h.

A variable refresh is possible as shown below:



The programmable watchdog can be viewed as a decrementing counter that is initialized by a write to register 196h. The processor must initialize the counter to prevent it from reaching count 0 (timeout).
The following C language procedure can be used to trigger the programmable watchdog.

```
#define TekReg 0x190                    // define base address (0x190)
void TrigWatchdog(timeout)      // select timeout at runtime: 0x80 = 0.016s,
// 0x90 = 0.065s, 0xA0 = 0.261s, ...
{
  outp(TekReg+6,(inp(TekReg+6) & 0x0F) | (timeout & 0xF0));
}
```

Time-out

The programmable watchdog has two stages: the first stage has a variable time-out while the second stage has a fixed one.

The first stage time-out is chosen at runtime from eight preset values (see table below). The first stage time-out generates an NMI interrupt (if enabled in register 196h, bit 7). An appropriate NMI handler must be written, otherwise this will be treated as a parity error by the default BIOS NMI handler; see register 196h description for a suggestion on how to do this.
The second stage times-out 8.6ms ±10% (depending on the temperature) after the first one and generates a master reset.

WDD[2..0]	NMI(T)	RESET(T)
000	0.016S	NMI(T)+ 8mS
001	0.064S	NMI(T)+ 8mS
010	0.256S	NMI(T)+ 8mS
011	1.024S	NMI(T)+ 8mS
100	~4S	NMI(T)+ 8mS
101	~16S	NMI(T)+ 8mS
110	~65S	NMI(T)+ 8mS
111	~4:22Min	NMI(T)+ 8mS

A reset from the programmable watchdog is latched for reset source identification.
The ePCI-100 is equipped with a circuit that can inform the user of the cause for the last system reset. The reset can be caused by the user pushing the push-button reset or the system reset can be caused by the watch dog timer elapsing. Bit D7 in register 191h is high if the last system reset was caused by the push-button reset. Bit D5 of register 191h is high if the watchdog timer elapsing caused the last system reset. These bits can be cleared by writing a “0” to bit D0 at 192h.

2.5.3 Thermal Management

Two temperature sensors are provided to supervise the thermal environment. One is used to monitor the CPU die temperature.

The temperature is controlled according to two temperature levels, the Low temperature limit, which indicates normal operating conditions, and the High temperature limit, which indicates an overheating condition.

The temperature management consists in reducing the CPU clock speed (throttling) when the temperature goes over the high limit (overheating condition) and suspending the throttling operation as soon as the temperature returns under the low temperature limit (normal condition).

The clock speed may be throttled due to CPU overheating caused by the system cooling failure. In such a case, the temperature control is triggered as soon as the temperature reaches the high temperature limit of the die.

The ambient temperature of the CPU generally raises up due to an augmentation of the temperature in the casing. In that case, the clock speed will be slowed down as soon as the ambient temperature reaches the high ambient temperature value.

Thermal management operations are controlled by the ICH, and settings are provided through the BIOS setup program interface.

2.6 Power Supply

When used as a stand-alone system, the ePCI-100 must be powered through the J15 Power connector. When installed on a backplane, the power is drawn to the power lines connected to the PCI fingers of the edge connectors.

Related Jumpers

None

BIOS Settings

See Power Management options described in Section 4.1.2.7 Power Menu Selection

2.6.1 Power Management

Power Management features are supported at the BIOS level. All Power Management options are described in the BIOS section.

Signal Path

The ePCI Power Management supporting voltage extension to the external Power Supply are available on the J15 connector.

Related Jumpers

None

BIOS Settings

Section 4.1.2.7.2 Hardware Monitor Inputs and 4.1.2.7.3 Hardware Monitor Controls.

2.7 I/O Devices

2.7.1 Ethernet Interface

The Ethernet controller is electrically connected to the PCI bus. It supports 10Base-T and 100Base-TX operations: 10Mbps and 100Mbps network speeds are automatically detected and switched.

Signal Path

The Ethernet interfaces are available through the connectors J9 and J10.

Related Jumpers

None.

BIOS Settings

Section 4.1.2.5 Advanced Menu Selection, Advanced Chipset Control, Onboard Ethernet Controller, Enable or Disable.

See also Boot 4.1.2.7.4 Boot Menu Selection, Network Boot.

2.7.1.1 Boot from LAN

The Boot from LAN capability is supported. To enable the option, use the BIOS Setup program (Boot Menu Selection).

2.7.1.2 Drivers

A CDROM is included with the ePCI-100. It contains network drivers for most common operating systems.

2.7.2 PS/2 Keyboard - PS/2 Mouse Interface

The onboard keyboard controller is 8042 software compatible. PS/2 keyboard and mouse signals are available through an output that supports direct connection to the interface.

Signal Path

PS/2 keyboard and PS/2 mouse signals are available through the Multifunction connector J6.

Related Jumpers

None

BIOS Settings

None

2.7.2.1 I/O Connections

Standard AT keyboard PS2 MOUSE, speaker port, reset and power buttons, and hard disk LED signals are available on the J6 Multifunction connector.

2.7.3 Parallel Port

The ePCI-100 features one IEEE-1854 multi-mode parallel port. It is compatible with Standard Mode IBM PC/XT, PC/AT, and PS/2 compatible bi-directional parallel port, Enhanced Parallel Port (EPP), and Enhanced Capabilities Port (ECP).

Signal Path
The Parallel Port interface is available through an onboard connector J5.
Related Jumpers
None
BIOS Settings
Section4.1.2.5 Advanced Menu Selection, I/O Device Configuration, Parallel Port (Enabled, Disabled, Auto or OS Controlled).

Section 4.1.2.5, I/O Device Configuration, Parallel Port Mode, (Output only, Bi-directional EPP and ECP.

The differences between Standard, EPP, and ECP modes appear in the signal assignation of the pins on the connector. Differences are described as follows:

Pin Number (J5)	Standard Mode	EPP Mode	ECP Mode
A15	SLCT	-	SLCT
B15	PE	-	PERROR[1], ACKREVERS[2]
C15	BUSY	WAIT	BUSY[1], PERIPHACK[2]
D15	ACK#	INTR#	ACK#
E16	SLCTIN#	ADDRSTRB#	SLCTIN#
B17	INIT#	-	INIT#[1], REVERSERQST#[2]
D17	ERR#	-	FAULT#[1],PERIPHRQST#[2]
A18	ALF	DATASTB	ALF[1], HOSTACK[2]
E17	D0	D0	D0
C17	D1	D1	D1
A17	D2	D2	D2
D16	D3	D3	D3
C16	D4	D4	D4
B16	D5	D5	D5
A16	D6	D6	D6
E15	D7	D7	D7

[1] Compatible mode
[2] High Speed Mode

NOTE
To operate in EPP or ECP mode, ensure the peripheral is designed to work in this mode and the BIOS setup is configured to support it.

2.7.3.1 Standard Mode

The Standard mode is unidirectional. It is supported to maintain the compatibility with the IBM PC standard.

2.7.3.2 EPP Mode

The EPP (Enhanced Parallel Port) mode consists of a hardware independent method of accessing a parallel port configured as EPP. It provides support for single I/O cycle as well as the high performance block I/O transfers. The EPP mode always uses the most optimum method for I/O transfers. For example, if the hardware supports it, EPP mode will perform 32-bit I/O block transfers.
EPP mode assumes that the parallel port can be used to connect more than one peripheral device using multiplexor or daisy chain configurations.
A multiplexor is an external device that permits up to eight parallel port devices to share a single parallel port.
A daisy chain device has two ports: input and output. The input port is connected either to the host parallel port or the daisy chain device in front of it. The output is used to connect the next peripheral device to the daisy chain. The last device, however, can be one without daisy chain support.

2.7.3.3 ECP Mode

ECP (Extended Capabilities Port) works the same as EPP mode, but it will take precedence over the EPP mode when addressing multiple logical devices in a single physical product. While the EPP mode may intermix read and write operations without any overhead or protocol handshaking, the ECP mode negotiates data transfers using a request from the host and an acknowledgment from the peripheral.

> **NOTE**
>
> For more information on the ECP protocol, please refer to the Extended Capabilities Port Protocol and ISA Interface Standard (available from Microsoft Corporation) or contact our Technical Support department (See appendix G).

2.7.4 Serial Ports

Two full function serial ports are provided on the board for asynchronous serial communications. They are 16C550 high-speed UART compatible and support 16-byte FIFO buffers for transfer rates from 50bps to 115Kbps.

Each serial port is specified as follows:

Designation	Communication Mode	Output Path
Serial Port 1	RS-232	J2
Serial Port 2	RS-232, RS-422 or RS-485	J1

UART registers are individually addressable and fully programmable.

2.7.4.1 Serial Port 1

Serial Port 1 is buffered directly for RS-232 operation. Signals include the complete signal set for handshaking, modem control, interrupt generation, and data transfer. When assigned as COM1, the port is 100% compatible with the IBM-AT serial port in RS-232 mode.
We can enable com1 in standard RS-232 mode or null modem mode with W2.

Signal Path

Serial Port 1 signal is available through J2 10-pin header.

Related Jumpers

W2

2.7.4.2 Serial Port 2

The serial port 2 is buffered directly for RS-232, RS-422 or RS-485 operations and is 16C550 PC-Compatible. The interface includes the complete signal set for handshaking, modem control, interrupt generation, and data transfer.
The serial port 2 is 100% compatible with the IBM-AT serial port.

Signal Path
Serial Port 2 signals are only available through J1-pin header.
Related Jumpers
NoneW1,W3

2.7.4.2.1 RS-232 Protocol:

When configured for RS-232 operation mode, the Serial Port 2 is 100% compatible with the IBM-AT serial port signals.

2.7.4.2.2 RS-422 Protocol:

The RS-422 protocol (Full Duplex) uses both RX and TX lines simultaneously during a communication session.

> **CAUTION**
>
> In RS-422 mode, W1 and W3 jumper caps must be installed to connect the 120-ohm line termination resistors (See Section 3.1 Setting Jumpers).

2.7.4.2.3 RS-485 Protocol:

The RS-485 protocol (Full Duplex) also uses differential signals during a communication session. It differs from the RS-422 mode as it offers the ability to transmit and receive over the same pair of wires, and allows the sharing of the communication line by multiple stations. This configuration (also known as Party Line) allows only one system to take control of the communication line at the time.
In RS-485 mode, the RX lines are used as the transceiver lines, and the RTS signal is used to control the direction of the RS-485 buffer.
When set for RS-485 mode in the BIOS, upon power-up or reset, the transceiver is by default in receiver mode to prevent unwanted perturbation on the line. Party line operation mode requires termination resistors to be installed at both ends of the network.

2.7.5 USB Interfaces

Signals for two USB ports are available through connectors J11 and J12 located on the faceplate.
USB is becoming the new essential peripheral interface. The USB strengths are as follows: capability to daisy chain as many as 127 devices per interface, fast bi-directional, isochronous/asynchronous interface, 12Mbps transfer rate, and standardization of peripheral interfaces into a single format.

Signal Paths
None
Related Jumpers
None

USB supports Plug and Play and hot swapping operations (OS level). These user-friendly features allow USB devices to be automatically attached, configured and detached, without reboot or running setup.
The ePCI-100 board fully supports the standard universal host controller interface (UHCI) and uses standard software drivers that are UHCI-compatible.

2.7.6 Video Interface

The high-performance video capability of the board is based on Accelerated Graphics Port (AGP) technology. The video controller with its high performance 2D/3D 64-bit video engine integrated into the chipset supports CRT displays with resolution of up to 1280x1024 16Mcolors.

Signal Path
VGA interface signals are available on J14, DVI analog/digital connector, located on the bracket of the board.
Related Jumpers
None

2.7.6.1 Supported Display Resolution and Colors

The maximum video resolution and performance depend directly on the drivers running with your software application. Resolution and number of color specification are listed below:

Resolution	Number of Colors
640x480, 800x600, 1024x768, 1280x1024, 1600x1200	16M(24 bits)

2.7.6.2 2D/3D Graphics Engine

The 2D/3D graphics engine is an advanced 64-bit three-operand engine that accelerates BitBLTs as line draws, polygon draw, and polygon fill. The 2D/3D graphics engine also performs video and bitmap scaling, and data overlay.

2.8 Storage

2.8.1 CompactFlash Interface

The ePCI-100 board supports an IDE compatible flash disk by using a CompactFlash carrier module connected to the Kontron's mezzanine (T069). CompactFlash (C-Flash) disks are the resident industry-standard ATA/IDE subsystem for application, data, image, and audio storage. They have the same functionality and capabilities as intelligent disk drives, but with the advantages of being very compact, rugged (typical M.T.B.F. is 1,000,000 hours) and low power. The ePCI-100 supports all CompactFlash sizes presently available and future sizes when available.
The C-Flash disk connects on the ePCI-100 via the onboard Flash Disk connector located at J18.

Related Jumpers
W6 to set the CompactFlash disk as master or slave (Located on the CompactFlash disk).

BIOS Settings
Section, Primary Master or Primary Slave, Auto.

The CompactFlash disk connects directly on the secondary EIDE interface. It must be configured the same way as a standard hard disk using the BIOS setup program (Autodetect function).
To setup the CompactFlash disk for Master or Slave configuration, use the CompactFlash jumper (W6).
To locate and install this jumper, please refer to Section 3.1 Setting Jumpers.

NOTES
Since CompactFlash devices use the ATA/IDE interface, no specific flash disk driver is required for various operating systems.

When using a CompactFlash disk, the operating temperature must not exceed 50°C/122°F.
When using a CompactFlash Disk and a hard disk drive on the secondary EIDE channel (J8):

a. The ATA66 HDD mode is not available on J8.
b. Use a cable (part # 150-050) in order to get proper detection.

2.8.2 Enhanced IDE Interfaces

The ePCI-100 board features two channels Bus Master PCI EIDE dedicated to Primary IDE logical interface. The channel supports up to four IDE devices (including CD-ROMs, hard disks, CompactFlash) with independent timings, in Master/Slave combination.

Signal Paths
The primary IDE interface is available on J4,J8 and at the Compact Flash connector J18.
Related Jumpers
None
BIOS Settings
Section 4.1.2.4 Main Menu Selection, Primary Master or Primary Slave.

Section 4.1.2.5, Advanced Menu Selection, Local Bus IDE Adapter, Primary or Secondary or Both or Disabled.

See also Section 4.1.2.5, Advanced Menu Selection, I/O Device Configuration, Large Disk Access Mode.

The IDE interface supports PIO mode 4 transfers up to 14MB/sec and Bus Master IDE transfer up to 66MB/sec (Ultra-DMA 66). It does not consume any ISA DMA resources and integrates 16x32-bit buffers for optimal transfers.

CAUTION
When connecting IDE devices to the Primary IDE interface, Master and Slave devices must be shared in respect of the device allocation on both the CompactFlash and hard disk drives.
Two Master devices (or two Slave devices) must not be installed on the same interface at the same time.

2.8.3 Floppy Disk Interface

The onboard floppy disk controller is IBM PC XT/AT compatible. It handles 3.5" and 5.25", low and high density disks. Up to two drives are supported in any combination.

Signal Paths
The Floppy Disk Controller interface is available through the J3 connector.
Related Jumpers
None.
BIOS Settings
Section 4.1.2.7.4 Boot Menu Selection, Removable Devices, Legacy Legacy Floppy Drives. Select the type of floppy installed.

Section Section4.1.2.5 Advanced Menu Selection, I/O Device Configuration, Floppy Disk Controller (Enabled, Disabled, Auto or OS Controlled).

PART 3

3 INSTALLING THE BOARD

1. SETTING JUMPERS
2. REGISTER'S DESCRIPTION
3. ONBOARD INTERCONNECTIVITY
4. USING THE EPCI-100 INTO A SYSTEM

3.1 Setting Jumpers

Seven jumpers are provided to setup the board. Their functions are summarized below:

3.2 Register's Description

3.2.1 0x190 Uart 2 Mode and Watchdog Control

Address	FPGA	D7	D6	D5	D4	D3	D2	D1	D0
0x190	READ	EN_LAN1	EN_LAN2	NU	RS485	RS232	ST	NU	
	WRITE								

EN_LAN1	*Enable/disable LAN 1*
EN_LAN2	*Enable/disable LAN 2.*
RS485	*Enable uart2 RS422 & 485 operation.*
RS232	*Enable uart2 RS232 operation.*
ST1	*Enable RTS2 to be used as 485TX ENABLE when in 485 mode.*

The serial port 2 mode can be controlled by setting 3 bits. Here are the possibilities.

Mode	Bit RS485	Bit RS232	Bit ST1
RS232	0	1	X
RS422	1	0	0
RS485	1	0	1
Power-up	0	0	0

3.2.2 0x191 History and Monitor Status

Address	FPGA	D7	D6	D5	D4	D3	D2	D1	D0
0x191	READ	PBRST	WDO1	WDO	CPUFLT	VT100	NU		PFO
	WRITE	NU				NU			

PFO	*Read the external power fail flag.*
VT100	*VT100 Flag (low enable VT100 mode)*
CPUFLT	*When low, signal a CPU thermal alarm to the outside world on the monitor connector.*
WDO	*When high, indicate that the last system reset was caused by watchdog time out.*
WDO1	*When low indicate that watchdog stage-1 timed out.*
PBRST	*When high, indicate that a system reset was caused by push button reset switch.*

3.2.3 0x192 Multimedia and Digital Watchdog Control, History Status

Address	FPGA	D7	D6	D5	D4	D3	D2	D1	D0
0x192	READ	NU					WD_LOCK	NU	CLRHIS
	WRITE								

CLRHIS	*When low, clear all history bits.*
WD_LOCK	*When high, lock the state of the enable bit for the digital watchdog.*

3.2.4 0x193 Monitoring Status and I/O Access

Address	FPGA	D7	D6	D5	D4	D3	D2	D1	D0
0x193	READ	APPFLT	NU	DATA_M	CLK_M	IDCHIP	NU	I2C_CLK	I2C_DATA
	WRITE								

I2C_DATA	*I^2C data.*
I2C_CLK	*I^2C Clock.*
IDCHIP	*One-wire clock/data for silicon ID chip.*
CLK_M	*Clock for monitoring connector. (Another I^2C Channel)*
DATA_M	*Data for monitoring connector. (Another I^2C Channel)*
APPFLT	*When low, signal an application fault to the outside world on the monitor connector. Clear on read.*

3.2.5 0x194 Uart 3 PnP Configuration

Address	FPGA	D7	D6	D5	D4	D3	D2	D1	D0
0x194	READ	NU							
	WRITE								

3.2.6 0x195 Uart 4 PnP Configuration

Address	FPGA	D7	D6	D5	D4	D3	D2	D1	D0
0x195	READ	NU						NU	
	WRITE							RED_L	GREEN_L

GREEN_L	*GREEN LED (write 1 at end of BIOS execution)*
RED_L	*RED LED (write 1 at end of BIOS execution)*

3.2.7 0x196 Digital Watchdog

Address	FPGA	D7	D6	D5	D4	D3	D2	D1	D0
0x196	READ	WDEN	WDD2	WDD1	WDD0	NU			
	WRITE								

WDD[2..0]	*Duration of digital watch dog.*
WDEN	*Enable/disable digital watchdog. (default disable)*

The digital watchdog duration can be controlled in the following way.

WDD[2..0]	NMI(T)	RESET(T)
000	0.016S	NMI(T)+ 8mS
001	0.064S	NMI(T)+ 8mS
010	0.256S	NMI(T)+ 8mS
011	1.024S	NMI(T)+ 8mS
100	~4S	NMI(T)+ 8mS
101	~16S	NMI(T)+ 8mS
110	~4:05Min	NMI(T)+ 8mS
111	~4:22Min	NMI(T)+ 8mS

3.2.8 0x197 NMI Control

Address	FPGA	D7	D6	D5	D4	D3	D2	D1	D0
0x197	READ	BATFEN	BATFLT	FANFEN	FANFLT	EXTFEN	EXTFLT	WDNMIEN	WDNMI
	WRITE		NU		NU		NU		NU

WDNMI	*When high, signal NMI from watchdog timeout.*
WDNMIEN	*Enable NMI generation from digital watchdog.*
EXTFLT	*When high, signal NMI from external source on monitor connector. Clear or read.*
EXTFEN	*Enable NMI generation from external source.*
FANFLT	*When high, signal NMI from external fan motion detector on monitor connector. Clear on read.*
FANFEN	*Enable NMI generation from fan fault on monitor connector.*
BATFLT	*When high, signal NMI from local RTC battery monitor. Clear on read.*
BATFEN	*Enable NMI generation for bat fault.*

3.2.9 Register BITs Description (Summary)

Address	FPGA	D7	D6	D5	D4	D3	D2	D1	D0
0x190	READ	EN_LAN1	EN_LAN2	NU	RS485	RS232	ST1	NU	NU
	WRITE								
0x191	READ	PBRST	WDO1	WDO	CPUFLT	VT100	NU		PFO
	WRITE	NU				NU			NU
0x192	READ	NU					WD_LOCK	NU	CLRHIS
	WRITE								
0x193	READ	APPFLT	NU	SMBCLK	SMBDATA	IDCHIP	NU	I2C_CLK	I2C_DATA
	WRITE								
0x194	READ	NU							
	WRITE								
0x195	READ	NU						NU	
	WRITE							RED_L	GREEN_L
0x196	READ	WDEN	WDD2	WDD1	WDD0	NU			
	WRITE								
0x197	READ	BATFEN	BATFLT	FANFEN	FANFLT	EXTFEN	EXTFLT	WDNMIEN	WDNMI
	WRITE		NU		NU		NU		NU

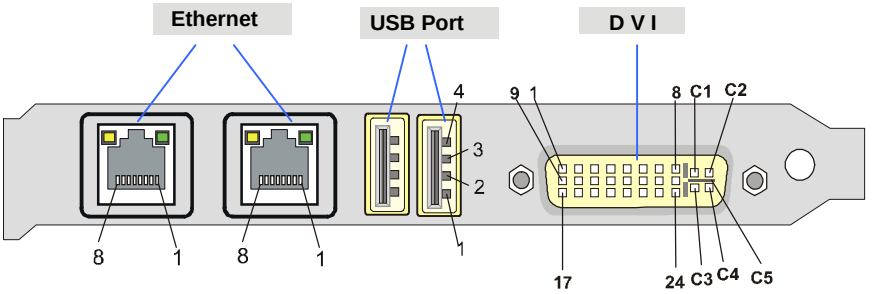
0x198 - 0x19F	R E S E R V E D

3.3 Onboard Interconnectivity

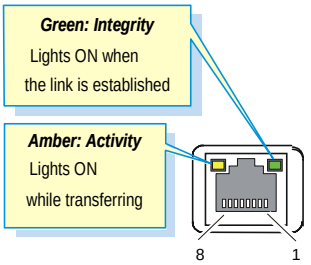
3.3.1 Onboard Connectors and Headers

Description	Connector's description	
Serial Port 1	J2	2 x 10-pin onboard connectors
Serial Port 2	J1	2 x 10-pin onboard connectors
Floppy	J3	1 x 34-pin onboard connector
EIDE (Primary/Secondary)	J4 / J8	2 x 40-pin onboard connectors
Parallel port	J5	1 x 26-pin onboard connector
Multifunction	J6	1 x 16-pin onboard connector for keyboard, PS/2 mouse, reset switch input, speaker, hard disks activity, and power led
Hardware monitor	J7	1 x 20-pin onboard connector for hardware monitoring
Ethernet	J9 / J10	2 x RJ-45 connectors with built-in activity and link indicators
USB 0 / USB 1	J11 / J12	2 x USB connectors (on the faceplate)
DVI	J14	1 x Female DVI-I analog/digital connector
External power	J15	1 x 6-pin onboard connector with 3.3V, 5V, and 12V
CPU Fan	J16	1 x 3-pin lock header
Fan Header	J17	1 x 3-pin lock header. The +12V DC CPU fan power supply is provided through this header as well as a speed sense input for the fan
CompactFlash disk	J18	1 x 40-pin board to board connector
SODIMM Socket	U9 / U10	2 x 144-pin SODIMMs, up to 512MB of SDRAM
PC/104+	P1	1 x standard 120-pin onboard connector
Battery	BT1	CMOS backup battery connector

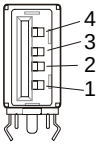
3.3.2 Front Plate Connectors and Indicators



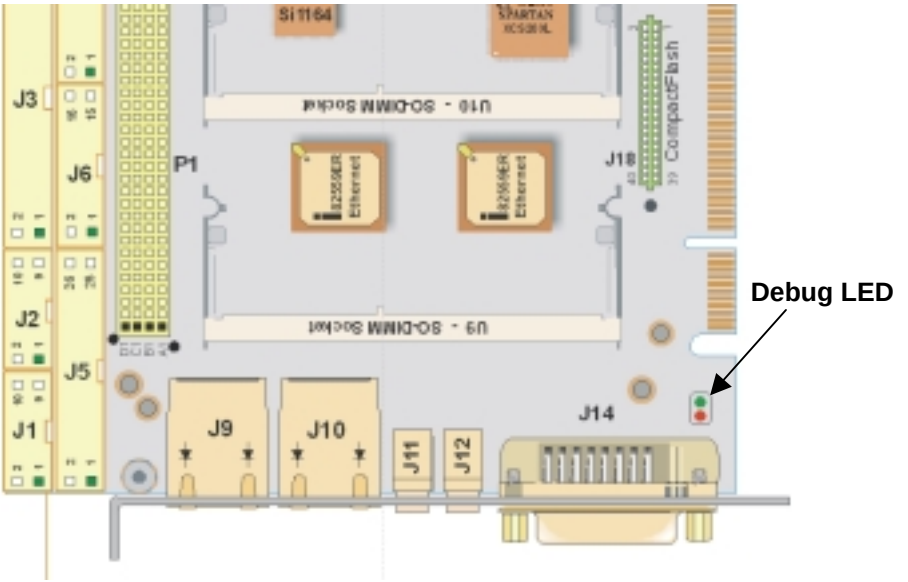
Ethernet Connector



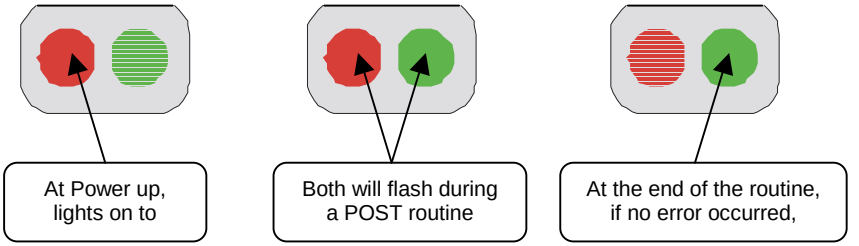
USB connector



3.3.3 Debug LED

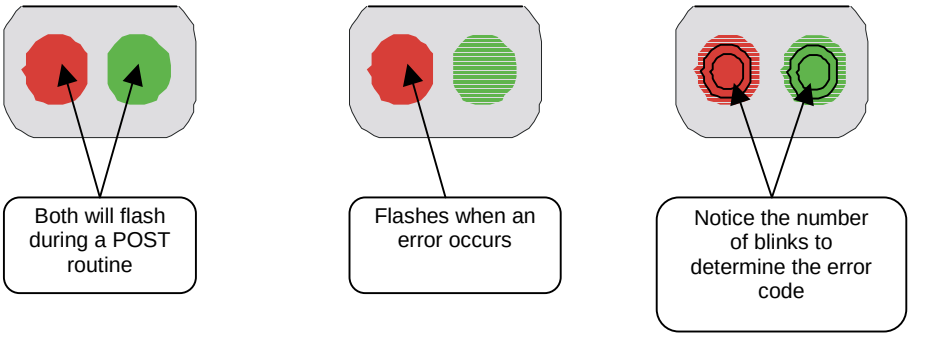


The following figure indicates the sequence that the debug LED will perform from the beginning of a power up until it reaches the end of a POST routine.



At the beginning of each POST routine, the debug LED lights YELLOW (both LEDs light on). If the BIOS detects an error condition, it halts POST after issuing an error post debug code and the LED will light RED indicating an error.

Soon afterward, the debug LED will flash RED then GREEN. Notice the number of time it flashes RED and GREEN and use these counts during troubleshooting to establish at what point the system failed and what routine was being performed.



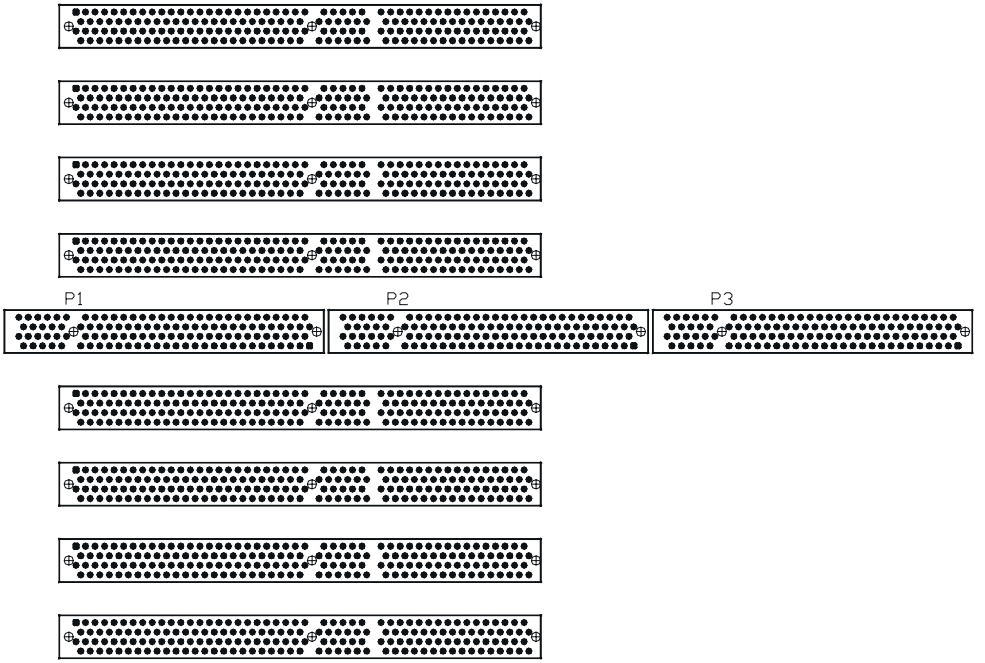
A list of the checkpoint codes (in hexadecimal) written at the start of each test and the debug LED codes issued for terminal errors is available in APPENDIX E.

3.4 Using the ePCI-100 into a System

3.4.1 The ePCI-X System

The ePCI-100 can be installed into an ePCI-X (Embedded PCI-X) system composed of a backplane and a removable CPU board called the System Host Board (SHB).

The backplane that can accept the ePCI-100 may have one or two PCI bus(ses). Each bus can have up to four, 0.8" spaced, PCI slots (more if PCI-to-PCI bridges are used). The SHB slot is in the middle of the backplane.



Dual-Bus Backplane Example (top view)

Components on the SHB are on the same side of the board as they are on PCI expansion boards. The SHB slot uses low cost and widely available standard PCI connectors.

3.4.2 SHBs and Backplanes Interoperability

If using a single-bus SHB in a dual-bus backplane does not sense, using a dual-bus SHB in a single-bus backplane can make some.

For this reason, extra signals were added for the SHB to sense the number of busses of the backplane (0, 1, or 2). The SHB can then disable any unused circuitry.

Backplane with SHBs can have 32 or 64-bit busses and all combinations are valid. For example, a SHB with a 32-bit bus can operate in a 64-bit backplane and 64-bit expansion boards will be able to do peer-to-peer 64-bit transfers.

3.4.3 Compatibility

An ePCI-X backplane is fully compliant to PCI-2.2, PCI-X addendum and ATX 1.0 specifications.

PART 4

4 SOFTWARE SETUPS

1. BIOS SETUP PROGRAM
2. BOOT UTILITIES
3. VT100 MODE

NOTE **UPDATING OR RESTORING THE BIOS IN FLASH**

(see the Kontron FTP site and select the “support” section)

4.1 BIOS Setup Program

All relevant information for operating the board and connected peripherals is stored in the CMOS memory. A battery-backed up memory holds this information when the board is powered off, the BIOS Setup program is required to make changes to the setup.

NOTES

Make sure you setup the BIOS Setup software prior to installing your operating system and your drivers.

For systems that need the BIOS to first attempt to boot from LAN, follow these steps:

1. Set the “Network Boot” or “Landesk Service Agent II” as the first boot service in the BIOS setup (Boot Menu Selection, Boot First Menu).

2. Follow the complete procedure in the Boot from LAN utility CDROM.

4.1.1 Accessing the BIOS Setup Program

The system BIOS (Basic Input Output System) provides an interface between the operating system and the hardware of the ePCI-100 peripheral processor. The ePCI-100 uses the Phoenix Setup program, a setup utility in flash memory that is accessed by pressing the DELETE key at the appropriate time during system boot. This utility is used to set configuration data in CMOS RAM.

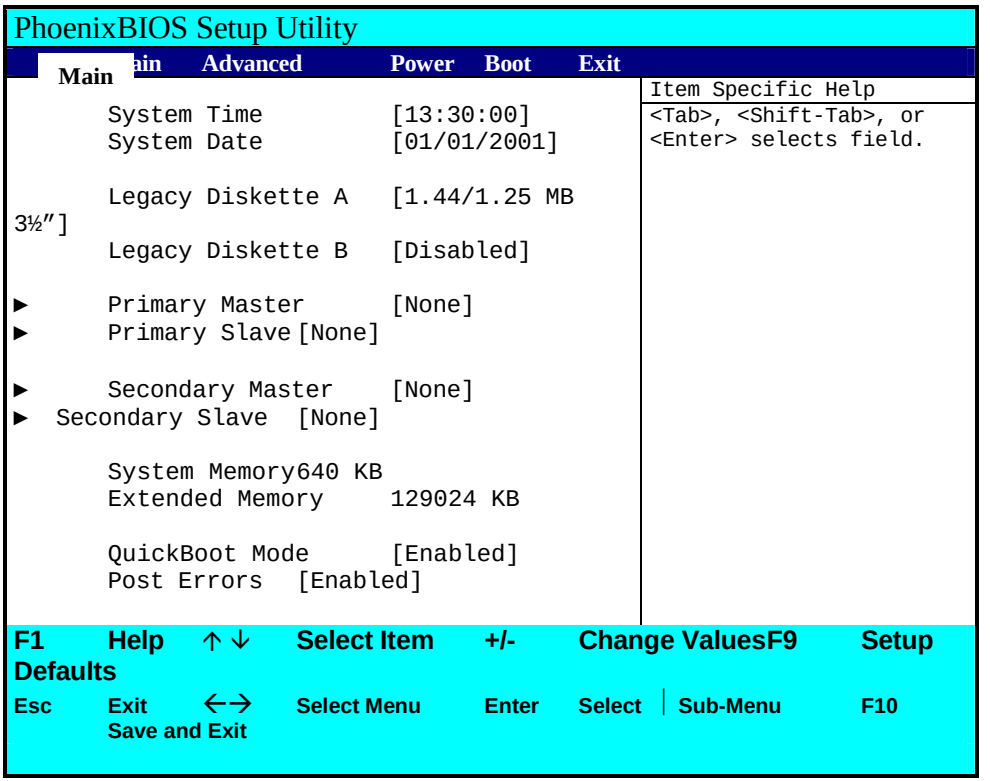
> **CAUTION**
>
> Before modifying CMOS setup parameters, ensure that the W7 battery selection jumper is installed to enable the CMOS battery backup (please refer to Section 3.1 Setting Jumpers

To run the Phoenix Setup program incorporated in the ROM BIOS:

- Turn on or reboot the system.
- When you get the following message, hit <F2> key to enter SETUP

  PhoenixBIOS 4.0 Release 6.0
  Copyright 1985-1999 Phoenix Technologies Ltd.
  All Rights Reserved
  KONTRON T8002 BIOS Version 1.0

The main menu of the Phoenix BIOS CMOS Setup Utility appears on the screen.



Whenever you are not sure about a certain setting, you may refer to the list of default values. The list of defaults is provided in the event that a value has been changed and one wishes to set this option to its original value. Loading the SETUP defaults will affect all the options in this screen (or all parameters if defaults are loaded from the Main Menu) and will reset options previously altered.

The BIOS Default values provide **optimum performance** settings for all devices and system features.

CAUTION

These parameters have been provided to give control over the system. However, the values for these options should be changed only if the user has a full understanding of the timing relationships involved.

4.1.2 The Menu Bar

The Menu Bar at the top of the window lists these selections:

Menu selection	Description
Main	Use this menu for basic system configuration
Advanced	Use this menu to set the Advanced Features available on your system's chipset.
Console Redirection	Use this menu to set the VT100 mode
Power	Use this menu to configure Power Management features
Boot	Use this menu to determine the booting device.
Exit	Exits the current menu.

Use the left and right ← and → arrows keys to make a selection.

4.1.2.1 The Legend Bar

Use the keys listed in the legend bar on the bottom to make your selections or exit the current menu. The chart on the following page describes the legend keys and their alternates:

Key	Function
<F1> or <Alt-H>	General Help windows (see below)
<Esc>	Exit this menu.
← → arrow keys	Select a different menu
<Tab> or <Shift-Tab>	Cycle cursor up and down
<Home> or <End>	Move cursor to top or bottom of window.
<PgUp> or <PgDn>	Move cursor to top or bottom of window.
<F5> or <->	Select the Previous Value for the field.
<F6> or <+> or <Space>	Select the Next Value for the field.
<F9>	Load the Default Configuration values for this menu
<F10>	Save and exit.
<Enter>	Execute Command or Select the Sub menu

To select an item, use the arrow keys to move the cursor to the field your want. Then use the plus-and-minus value keys to select a value for that field. To save values commands in the Exit Menu save the values currently displayed in all the menus.
To display a sub-menu, use the arrow keys to move the cursor to the sub menu your want. Then press <Enter>. A pointer ( ) marks all sub menus.

4.1.2.2 The Field Help Window

The help window on the right side of each menu displays the help text for the currently selected field. It updates as you move the cursor to each field.

4.1.2.3 The General Help Windows

Pressing <F1> or <Alt-H> on any menu brings up the General Help window that describes the legend keys and their alternates:

General Help

Setup changes system behavior by modifying the BIOS configuration. Selecting incorrect values may cause system boot failure; load Setup Default values to recover.
<Up/Down> arrows select fields in current menu.
<PgUp/PgDn> moves to previous/next page on scrollable menus.
<Home/End> moves to top/bottom item of current menu.
Within a field, <F5> or <-> selects next lower value and <F6>, <+>, or <Space> selects next higher value.
<Left/Right> arrows select menus on menu bar.
<Enter> displays more options for items marked with .
<F9> loads factory installed Setup Default values.
<F10> saves current settings and exists Setup.
<Esc> or <Alt-X> exits Setup; in sub-menus, pressing these keys returns to the previous menu.
<F1> or <Alt-H> displays General Help (this screen).

[Continue]

The scroll bar on the right of any windows indicates that there is more than one page of information in the windows. Use <PgUp> and <PgDn> to display all the pages. Pressing <Home> and <End> displays the first and last page. Pressing <Enter> displays each page and then exits the window.

4.1.2.4 Main Menu Selection

You can make the following selections on the Main Menu itself. Use the sub menus for other selections.

Feature	Options		Description
System Time	HH:MM:SS		Set the system time.
System Date	MM/DD/YYYY		Set the system date.
Legacy Diskette A: Legacy Diskette B:	Disabled 360Kb 5.1/4” 1.2MB, 5.1/4”< 720 Kb 3 1/2” 1.44/.125 MB 3 1/2” 2.88 MB 3 ½		Select the type of floppy disk drive installed in your system. **Note :** 1.25MB 3 1/2” references a 1024 byte/sector Japanese media format. The 1.25MB, 3 1/2 diskette requires a 3-Mode floppy-disk drive.
Primary Master	Type	None	None No booting device installed.
		CD-ROM	CD-ROM CD-ROM drive installed.
			Multi-Sector Transfers Any selection except Disabled determines the number of sectors transferred per block. Standard is 1 sector per block. **LBA Mode Control** Enabling LBA causes Logical Block Addressing to be used in place of Cylinders, heads, and Sectors. **32 Bit I/O** Enables 32-bit communication between CPU and IDE card. Requires PCI or local bus. **Transfer Mode** Selects the method for transferring the data between the hard disk and system memory. The Setup menu only lists those options supported by the drive and platform. **Ultra DMA Mode** Select the Ultra DMA mode used for moving data to/from the drive. Autotype the drive to select the optimum transfer mode.
		ATAPI Removable	Choices are same as CD-ROM

Main Menu Selection (continued)

Feature	Options		Description
Primary Master (Continued)	Type (continued	IDE Removable	Choices are same as CD-ROM
		USER)	**Cylinders** Set the number of cylinders **Heads** Set the number of heads. Choices are 1 to 16 **Sectors** Set the number of sectors per track **Maximum Capacity** Maximum capacity is displayed according to the cylinders, heads and sectors selected. **Multi-Sector Transfers** Specify the number of sectors per block for multiple sector transfers. "MAX" refers to the size the disk returns when queried. **LBA Mode Control** Enabling LBA cause Logical Block Addressing to be used in place of Cylinders Heads and Sectors **32 Bit I/O** This setting enables or disables 32 bit IDE data transfers. **Transfer Mode** Select the method for moving data to/from the drive. Autotype the drive to select the optimum transfer mode. **Ultra DMA Mode** Select the Ultra DMA mode used for moving data to/from the drive Autotype the drive to select the optimum transfer mode.
		Auto	BIOS autodetects the hard disk installed
Primary Slave	Type	None CD-ROM ATAPI Removable IDE Removable User Auto	Same description as Primary Master
Secondary Master	Type	None CD-ROM ATAPI Removable IDE Removable User Auto	Same description as Primary Master

Main Menu Selection (continued)

Secondary Slave	Type	None CD-ROM ATAPI Removable IDE Removable User Auto	Same description as Primary Master
System Memory	*640KB*		Displays the amount of conventional memory detected during boot up
Extended Memory	*It depends on the memory installed*		Displays the amount of extended memory detected during boot up
QuickBoot Mode	Enabled Disabled		Allows the system to skip certain tests while booting. This will decrease the time needed to boot the system.
POST Errors	Enabled Disabled		Pauses and displays SETUP entry or resume boot prompt if error occurs on boot. If disabled, system always attempts to boot.

4.1.2.5 Advanced Menu Selection

You can make the following selections on the Advanced Menu. Use the sub-menus for other selections.

Feature	Options	Description
Installed O/S	Other Win95 Win98/Win2000	Other : Non PnP or ACPI OS. Win95 : PnP OS. Win98/Win2000 : ACPI OS. Select the operating system installed on your system that you will use most commonly. **Note :** An incorrect setting can cause some operating systems to display unexpected behavior.
Reset Configuration Data	No Yes	Select "Yes" if you want to clear the Extended System Configuration Data (ESCD) area.
Cache Memory	Memory Cache [Enabled / Disabled]	Sets the state of the memory cache.
	Cache System BIOS area	Controls caching of system B0S area. Choices are: **uncached, Write Protect**
	Cache Video BIOS area	Controls caching of video BIOS area.Choices are: **uncached, Write Protect**
	Cache Base 0-512K	Controls caching of 512k base memory Choices are : **uncached, Write Through, Write Protect, and Write Back**
	Cache Base 512K-640K	Controls caching of 512k-640k base memory Choices are : **uncached, Write Through, Write Protect, and Write Back.**
	Cache Extended Memory Area	Controls caching of system memory Choices are: **uncached, Write Through, Write Protect, and Write Back.**
	Cache A000-AFFF	Set the type of caching. Following choices are available : **Disabled** : This block is not cached. **USWC Caching** :Uncached Speculative Write Combined. **Write Through:** Writes are cached and sent to main memory at once. **Write Protect:** Writes are ignored. **Write Back:** Writes are cached, but not sent to main memory until necessary. Set the type of caching. Following choices are available :Disabled, Write Through, Write Protect, and Write Back
	Cache B000-BFFF	Same as above
	Cache C800-CBFF	Set the type of caching. Following choices are available: **Disabled, Write Through, Write Protect, and Write Back**

Advanced Menu Selection (continued)

Feature	Options	Description
Cache Memory	Cache CC00-CFFF	Same as above
	Cache D000-D3FF	
	Cache D400-D7FF	
	Cache D800-DBFF	
	Cache DC00-DFFF	
	Cache E000-E3FF	
	Cache E400- E7FF	
	Cache E800-EBFF	
	Cache EC00- EFFF	
I/O Device Configuration	Serial Port A	Configure serial port A using options: **Disabled :** No configuration **Enabled :** User configuration When Enabled, set the base I/O address for serial port A. Choices are : **3F8, 2F8, 3E8, 2E8** Choices for IRQs are: **IRQ 3** and **IRQ 4** **Auto :** BIOS or OS chooses configuration **OS Controlled :** Displayed when controlled by OS.
	Serial Port B	Same as above
	Mode	Set the mode of rserial port B. Choices are : RS-232, RS-422, and RS-485.
	Parallel port	Configure parallel port using options : **Disabled :** No configuration **Enabled :** User configuration When enabled, set the Base I/O address. Choices are: **378, 278** and **3BC.** Choices for IRQs are: **IRQ5** and **IRQ7.** **Auto:** BIOS or OS chooses configuration **OS Controlled:** Displayed when controlled by OS
	Mode	**Mode** Set the mode for the parallel port using options: **Output only, Bi-directional EPP** and **ECP**

Advanced Menu Selection (continued)

Feature	Options	Description
I/O Device Configuration (continued)	Floppy disk controller	Configure the floppy disk controller by using these options : **Disabled :** No configuration **Enabled:** User configuration **Auto:** BIOS or OS chooses configuration **OS Controlled :** Displayed when controlled by OS**.**
	Base I/O address	Set the base I/O address for the floppy disk controller using options : **Primary** or **Secondary**
Large Disk Access Mode	Other DOS	If you are using UNIX, Novell Netware or other operating systems, select "**Other**". If you are installing new software and the drive fails, change this selection and try again. Different operating systems require different representations of drive geometries.
Local Bus IDE Adapter	Disabled Primary Secondary Both	Enable the integrated local bus IDE adapter

Advanced Menu Selection (continued)

Feature	Options	Description
Advanced Chipset Control	Video boot type	Select “Onboard Video” to enable the onboard video controller as the boot display device. Select either 512K or 1MB of System Memory to be allocated to the onboard video controller. Select “Disable Onboard Video” to disable the onboard video controller. No System Memory will be allocated for video.
	Enable memory gap	If enabled, turn system RAM off to free address space for use with an option card. Either a 128KB conventional memory gap, starting at 512KB, or a 1MB extended memory gap, starting at 15MB, will be created in system RAM.
	Enable CD hole	If enabled, turn system RAM off to free address space for use with an option card. A 16KB CD hole, starting at 880KB (DC000h) will be created in system memory space.
	Frequency Ratio	Select the internal frequency multiplier of the CPU. Choices are 2x, 4x, 3x, 5x, 2.5x, 4.5x, 3.5x, 5.5x, 6x, 8x, 7x, 6.5x, 1.5x, 7.5x, and 2x.
	Legacy USB Support	Enables/Disables support for Legacy Universal Serial Bus.
	Onboard Ethernet 1 Controller	Enables/Disables onboard Ethernet Controller.
	Onboard Ethernet 2 Controller	Enables/Disables onboard Ethernet Controller.
	Save CMOS in FLASH	Enable/Disable Save CMOS in FLASH.
	CPU Clock Spread Spectrum	Enables/Disables Spread Spectrum.

4.1.2.6 Console Redirection Menu Selection

Feature	Options	Description
Com Port Address	COM A, COM B	If enabled, it will use the port.
Baud Rate	600, 1200, 2400, 4800, 9600, 19.2K, 38.4K, 115.2K	Enables the specified baud rate
Console Type	PC ANSI, VT100	Enables the specified console type
Flow Control	No Flow Control, XON/XOFF, CTS/RTS	Enables Flow Control
Console connection	Direct,, Via modem	Indicate whether the console is connected directly to the system or a modem is used to connect
Console Redirection After POST	On, Off	Enables Console redirection after OS has loaded

4.1.2.7 Power Menu Selection

Feature	Options	Description
Power Savings	Disabled	To turn off power management, choose Disabled.
	Customized	To alter these settings, choose Customized
	Maximum Power Savings	Maximum Power Savings conserves the greatest amount of system power .
	Maximum Performance	Maximum Performance conserves power but allows greatest system performance
Standby Timeout	Off 2 Minutes 4 Minutes 6 Minutes 8 Minutes 12 Minutes 16 Minutes	Amount of time the system needs to be in Idle Mode before entering the Standby Mode. Standby Mode turns off various devices in the system, including the screen, until you start using the computer again .
Auto Suspend Timeout	Off 5 Minutes 10 Minutes 15 Minutes 20 Minutes 30 Minutes 40 Minutes 60 Minutes	Amount of time the system needs to be in Standby before entering the SUSPEND Mode.
Resume On Time	Off On	Enabled wakes the system up at a specific time
Resume Time	[00:00:00]	Specify the time when the system is to wake up. <Tab>, <Shift-Tab>, or <Enter> selects field
Resume on Modem Ring	Off On	Enabled wakes the system up when an incoming call is detected on your modem.
Intelligent System Monitor	**This is a Sub-Menu, see section 4.1.2.7.1**	

4.1.2.7.1 Intelligent System Monitor

You can make the following selections on the Intelligent System Monitoring Sub-Menu. Use the sub menus for other selections.

Feature	Options	Description
Intelligent System Monitoring	Disabled Enabled	Enables/Disables the Intelligent System Monitor device. When enabled, the system will monitor some system states such as temperature and power supplies.
Interrupt Generation	Disabled Enabled	Enables/Disables the generation of interrupts when an event occurs. This must be set to DISABLED when programs such as LANDesk® are loaded onto the system.
Chassis Intrusion	Disabled Enabled	Enables/Disables the detection of chassis intrusion.
Secured Chassis	Disabled Enabled	Controls the SECURE CHASSIS feature. If set to ENABLED and a chassis intrusion is detected, the user is required to enter SETUP and set the option "Reset chassis intrusion" to "Yes", before the system is allowed to complete the boot.
Reset Chassis Intrusion	No Yes	Selecting "Yes" will reset the chassis intrusion circuitry on the next boot.
Beep codes for non-thermal events	Disabled Enabled	Produces beep codes when the Intelligent System Monitoring events occur for either the chassis, the fan or the voltages. Codes are as follows: One long beep plus: 2 short beeps for chassis intrusion 3 short beeps for fan events 4 short beeps for voltage events This alarm may not be supported by the operating system.
Thermal Audio Alarm	Disabled Enabled	When the Thermal Management option and this option are enabled, a continuous audible alarm is sounded when the temperature specified in the Overheat Alarm options is reached. This alarm may not be supported by the operating system.
Hardware Monitor Inputs	**This is a Sub-Menu, see section 4.1.2.5.1.1**	
Hardware Monitor Controls	**This is a Sub-Menu, see section 4.1.2.5.1.**	

4.1.2.7.2 Hardware Monitor Inputs

Feature	Options	Description
MB Temperature	**Displays a Status and limit set in other menu.**	
CPU Temperature		
VCORE Voltage		
+3.3V Voltage		
+5V Voltage		
+2.5V Voltage		
VTT Voltage		
Vbat Voltage		
+12V Voltage		
-12V Voltage		
CPU Fan (RPM)		
System Fan (RPM)		
External Fan 1 (RPM)		
External Fan 2 (RPM)		
External Fan 3 (RPM)		
External Fan 4 (RPM)		
External Fan 5 (RPM)		
External Fan 6 (RPM)		

4.1.2.7.3 Hardware Monitor Controls

Feature	Options	Description
CPU Temperature Interrupt	Enabled Disabled	This option enables Temperature events handling.
Resume Alarm (ºC)	10ºC to 70ºC with step of 4ºC	Full speed (Normal mode) will be resumed when the temperature comes down to the selected temperature.
Overheat Alarm (ºC)	30ºC to 90ºC with step of 4ºC	The CPU will be slowed down (Doze mode) When it reaches the selected temperature.
VCORE Voltage Interrupt	Enabled **DISABLED**	**THIS OPTION ENABLES VOLTAGE EVENTS HANDLING.**
+3.3V Voltage Interrupt	Enabled **DISABLED**	**THIS OPTION ENABLES VOLTAGE EVENTS HANDLING.**
+5V Voltage Interrupt	Enabled Disabled	This option enables Voltage events handling.
+2.5V Voltage Interrupt	Enabled Disabled	This option enables Voltage events handling.
VTT Voltage Interrupt	Enabled Disabled	This option enables Voltage events handling.
Vbat Voltage Interrupt	Enabled Disabled	This option enables Voltage events handling.
+12V Voltage Interrupt	Enabled Disabled	This option enables Voltage events handling.
-12V Voltage Interrupt	Enabled Disabled	This option enables Voltage events handling.
CPU Fan Interrupt	Enabled **DISABLED**	**THIS OPTION ENABLES TEMPERATURE EVENTS HANDLING.**
System Fan Interrupt	Enabled **DISABLED**	**THIS OPTION ENABLES TEMPERATURE EVENTS HANDLING.**
External Fan 1 Interrupt	Enabled **DISABLED**	**THIS OPTION ENABLES TEMPERATURE EVENTS HANDLING.**
External Fan 2 Interrupt	Enabled **DISABLED**	**THIS OPTION ENABLES TEMPERATURE EVENTS HANDLING.**
External Fan 3 Interrupt	Enabled **DISABLED**	**THIS OPTION ENABLES TEMPERATURE EVENTS HANDLING.**
External Fan 4 Interrupt	Enabled **DISABLED**	**THIS OPTION ENABLES TEMPERATURE EVENTS HANDLING.**
External Fan 5 Interrupt	Enabled **DISABLED**	**THIS OPTION ENABLES TEMPERATURE EVENTS HANDLING.**
External Fan 6 Interrupt	Enabled **DISABLED**	**THIS OPTION ENABLES TEMPERATURE EVENTS HANDLING.**

4.1.2.7.4 Boot Menu Selection

Feature	Options	Description
	Removable Devices Legacy Floppy Drives Hard Drive Bootable Add-in Cards ***** ATAPI CD-ROM Drive Network Boot	Keys used to view or configure devices: **<Enter>** expands or collapses devices with a **+** or **–** **<Ctrl+Enter>** expands all **<Shift + 1>** enables or disables a device **<+>** or **<->** moves the device up or down **<n>** May move removable device between Hard Disk or Removable Disk **<d>** Remove a device that is not installed. ***** Note : The hard drives and SCSI drives detected will be listed in this section and the first drive in the list will be the boot drive.

4.1.2.8 Exit Menu Selection

Feature	Options	Description
	Exit Saving Changes	Exit System Setup and save your changes to CMOS.
	Exit Discarding Changes	Exit utility without saving Setup data to CMOS.
	Load Setup Defaults	Load default values for all SETUP items.
	Discard Changes	Load previous values from CMOS for all SETUP items.
	Saves Changes	Save Setup Data to CMOS.

4.2 Boot Utilities

Phoenix Boot Utilities are : Phoenix QuietBoot™
Phoenix MultiBoot™

Phoenix QuietBoot displays a graphic illustration rather than the traditional POST messages while keeping you informed of diagnostic problems.

Phoenix MultiBoot is a boot screen that displays a selection of boot devices from which you can boot your operating system.

4.2.1 Phoenix QuietBoot

Right after you turn on or reset the computer, Phoenix QuietBoot displays the QuietBoot Screen, a graphic illustration created by the computer manufacturer instead of the text-based POST screen, which displays a number of PC diagnostic messages.

To exit the QuietBoot screen and run Setup, display the MultiBoot menu, or simply display the PC diagnostic messages, you can simply press one of the hot keys described below.

The QuietBoot Screen stays up until just before the operating system loads unless:

You press <ESC> to display the POST screen.
You press <F2> to enter Setup.
POST issues an error message.
The BIOS or an option ROM requests keyboard input.

The following explains each of these situations.

4.2.1.1 Press <ESC>

Pressing <ESC> switches the POST screen and takes one of two actions:

If MultiBoot is installed, the boot process continues with the text-based POST screen until the end of POST, and then displays the BootFirst Menu, with these options:
Load the operating system from a boot device of your choice.
Enter Setup.
Exit the Boot First Menu (with <ESC>) and load the operating system from the boot devices in the order specified in Setup.
If MultiBoot is not installed, the boot process continues as usual.

4.2.1.2 Press <F2>

Pressing <F2> at any time during POST switches to the POST screen (if not already displayed) and enter Setup.

4.2.1.3 POST Error

Whenever POST detects a non-fatal error, QuietBoot switches to the POST screen and displays the errors. It then displays this message:

Press <F1> to resume, <F2> to Setup

Press <F1> to continue with the boot. Press <F2> if you want to correct the error in Setup.

Keyboard Input Request

If the BIOS or an Option ROM (add-on card) requests keyboard input, QuietBoot switches over to the POST screen and the Option ROM displays prompts for entering the information. POST continues from there with the regular POST screen.

4.2.1.4 Phoenix MultiBoot™

Phoenix MultiBoot expands your boot options by letting you choose your boot device, which could be a hard disk, floppy disk, or CDROM. You can select your boot device in Setup, or you can choose a different device each time you boot during POST by selecting your boot device in **The Boot First Menu**.
MultiBoot consist of :

The Setup Boot Menu
The Boot First Menu

4.3 VT100 Mode

The VT100 operating mode allows remote setups of the board. This configuration requires a remote terminal that must be connected to the board through a serial communication link.

4.3.1 Requirements

The terminal should emulate a VT100 or ANSI terminal. Terminal emulation programs such as Telix© or Procom© can also be used.

4.3.2 Setup & Configuration

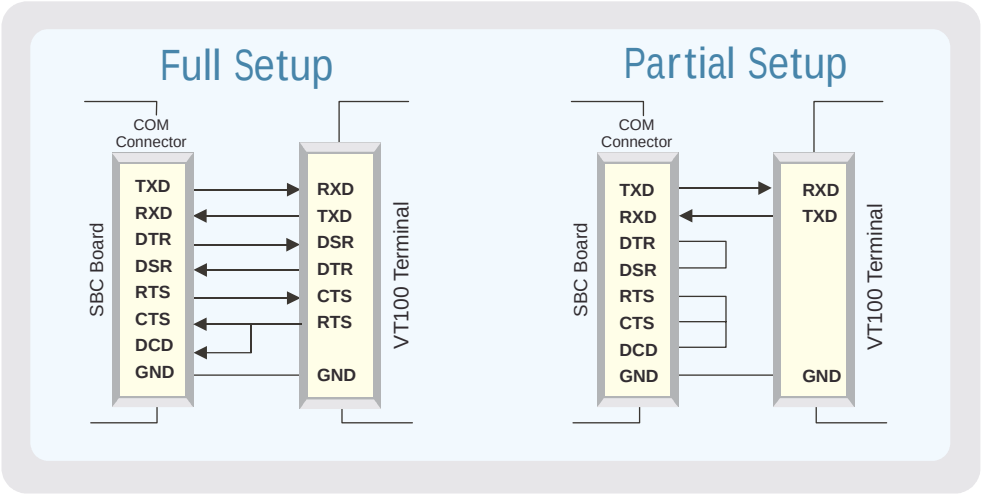
Follow these steps to set up the VT100 mode:

1. Connect a monitor and a keyboard to your board and turn on the power
2. Enter into the CMOS Setup program in the "BIOS Feature Setup"
3. Select the VT100 mode and the appropriate COM port and save your setup
4. Connect the communications cable as shown in the next page

NOTE

If you do not require a full cable for your terminal, you can set up a partial cable by using only the TXD and RXD lines. To ignore control lines simply loop them back as shown in VT100 Partial Setup cable diagram.

5. Configure your terminal to communicate using the same parameters as in CMOS Setup
6. Install the VT100 jumper and reboot the board (see section 3.1Setting Jumpers)
7. Use the remote keyboard and display to setup the BIOS
8. Save the setup, exit, and disconnect the remote computer from the board to operate in stand-alone configuration.



Running Without a Terminal

The board can boot up without a screen or terminal attached. If the speed is set to Auto and no terminal is connected, the speed is set to 115,200 bps.

Furthermore, you can run without any console at all by simply not enabling VT100 Mode and by disabling the onboard video.

PART 5

APPENDICES

A. MEMORY & I/O MAPS

B. INTERRUPT LINES

C. BOARD DIAGRAMS

D. CONNECTOR PINOUTS

E. BIOS SETUP ERROR CODES

F. BIOS UPDATE & EMERGENCY PROCEDURE

G. GETTING HELP & RMA

A. MEMORY & I/O MAPS

A.1 MEMORY MAPPING

Address	Function
00000-9FFFF	0-640 KB DRAM
A0000-BFFFF	Video DRAM
C0000-CBFFF	Video BIOS
CC000-DFFFF	Optional ROM (Free)
	LAN BIOS around 30KB if activated, address may vary
	SCSI BIOS 18KB at runtime, 2KB if no device, address may vary
E0000-FFFFF	System BIOS
100000-Top of DRAM	1 MB - Top of DRAM

A.2 I/O MAPPING

Address	Optional Address	Optional Address	Optional Address	Function
000-01F				DMA Controller 1
020-03F				Interrupt Controller 1
040-05F				Timer
060-06F				Keyboard
070-07F				Real-time clock
080-09F				DMA Page Register
0A0-0BF				Interrupt Controller 2
0C0-0DF				DMA Controller 2
0F0-0F1, 0F8-0FF				Math Coprocessor
x90-x9F				Kontron Control Port
1F0-1F7, 3F6				Primary IDE
3F0-3F7	370-377			Floppy Disk
378-37A	3BC-3BE	2787-27A		Parallel Port (LPT1 by default)
3F8-3FF (COM1)	2F8-2FF (COM2)	3E8-3EF (COM3)	2E8-2EF (COM4)	Serial Port 1 (COM1 by default)
2F8-2FF (COM2)	3F8-3FF (COM1)	3E8-3EF (COM3)	2E8-2EF (COM4)	Serial Port 2 (COM2 by default)
3C0-3CF, 3D0-3DF, 3B0-3BB				Graphics Controller (I2C Port)

B. INTERRUPT LINES

B.1 IRQ LINES

The board is fully PC compatible with interrupt steering for PCI plug and play compatibility.

Controller # 1		Controller # 2	
IRQ 0	Timer Output 0	IRQ 8	Real-Time Clock
IRQ 1	Keyboard	IRQ 9	Available [1]
IRQ 2	Cascade Controller # 2	IRQ 10	Available [1]
IRQ 3*	Serial Port 2	IRQ 11	Available [1]
IRQ 4*	Serial Port 1	IRQ 12	PS/2 Mouse
IRQ 5*	Available [1]	IRQ 13	Coprocessor Error
IRQ 6*	Floppy Controller	IRQ 14	Primary IDE or available [1]
IRQ 7*	Parallel Port 1 or Available [1]	IRQ 15	N/C

* :All functions marked with an asterisk (*) can be disabled or reconfigured.
1 Available lines service on board and external PCI/ISA PnP devices or a Legacy ISA device.

B.2 DMA CHANNELS

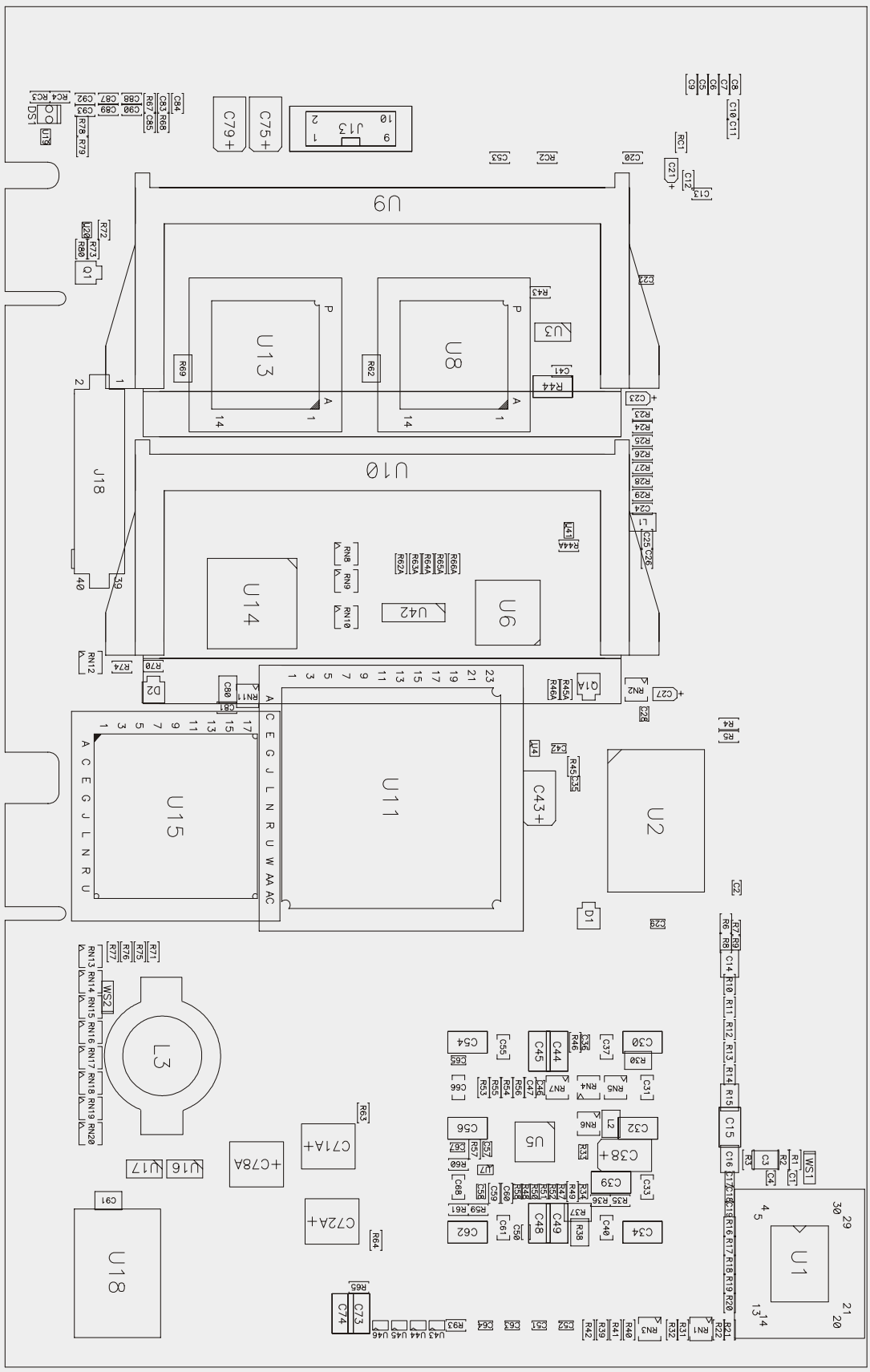
The ePCI-100 integrates the functionality of two 8237 DMA controllers. Eight DMA channels are available.

According to Plug and Play standards, the system BIOS automatically allocates DMA Channel 1 or 3 for the parallel port's ECP mode. Channel 2 is reserved for the floppy controller and Channel 4 is used to cascade Channels 0 through 7 to the microprocessor.

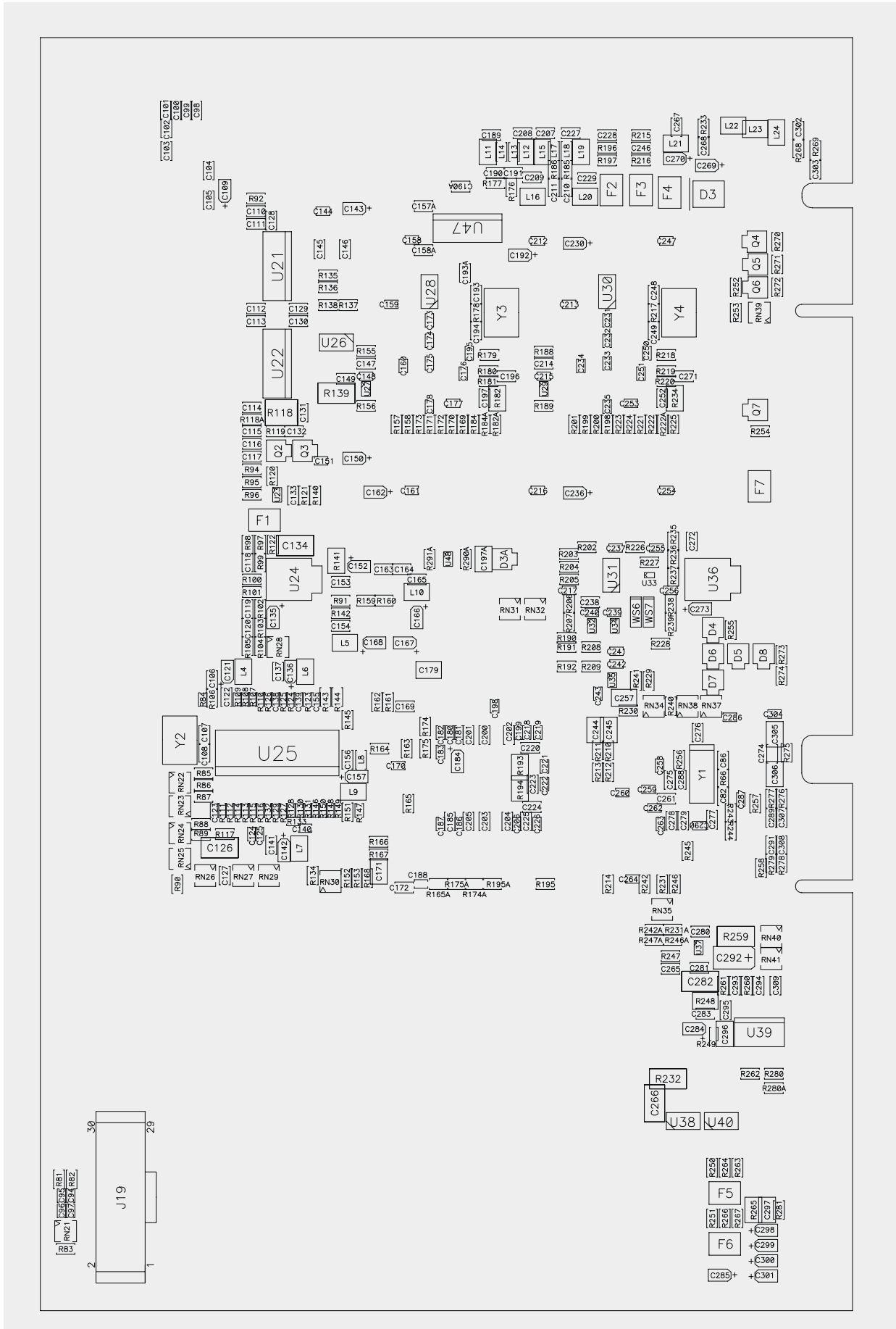
DMA Channel	Function
DMA 0	Available
DMA 1	PnP available (ECP)
DMA 2	Floppy controller
DMA 3	PnP available (ECP)
DMA 4	Cascade controller # 1
DMA 5	PnP available
DMA 6	PnP available
DMA 7	PnP available

C. BOARD DIAGRAMS

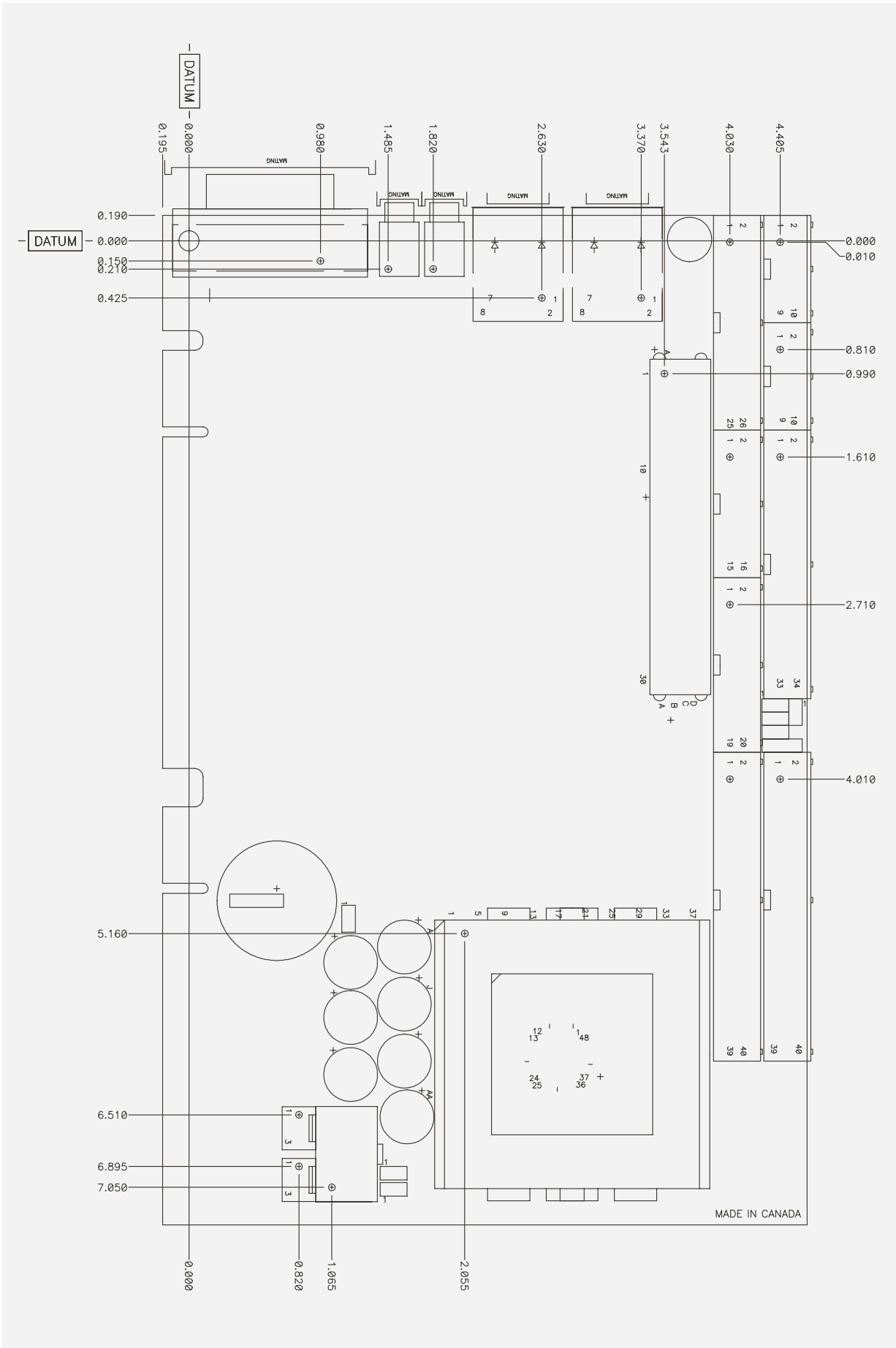
C.1 ASSEMBLY TOP DIAGRAM



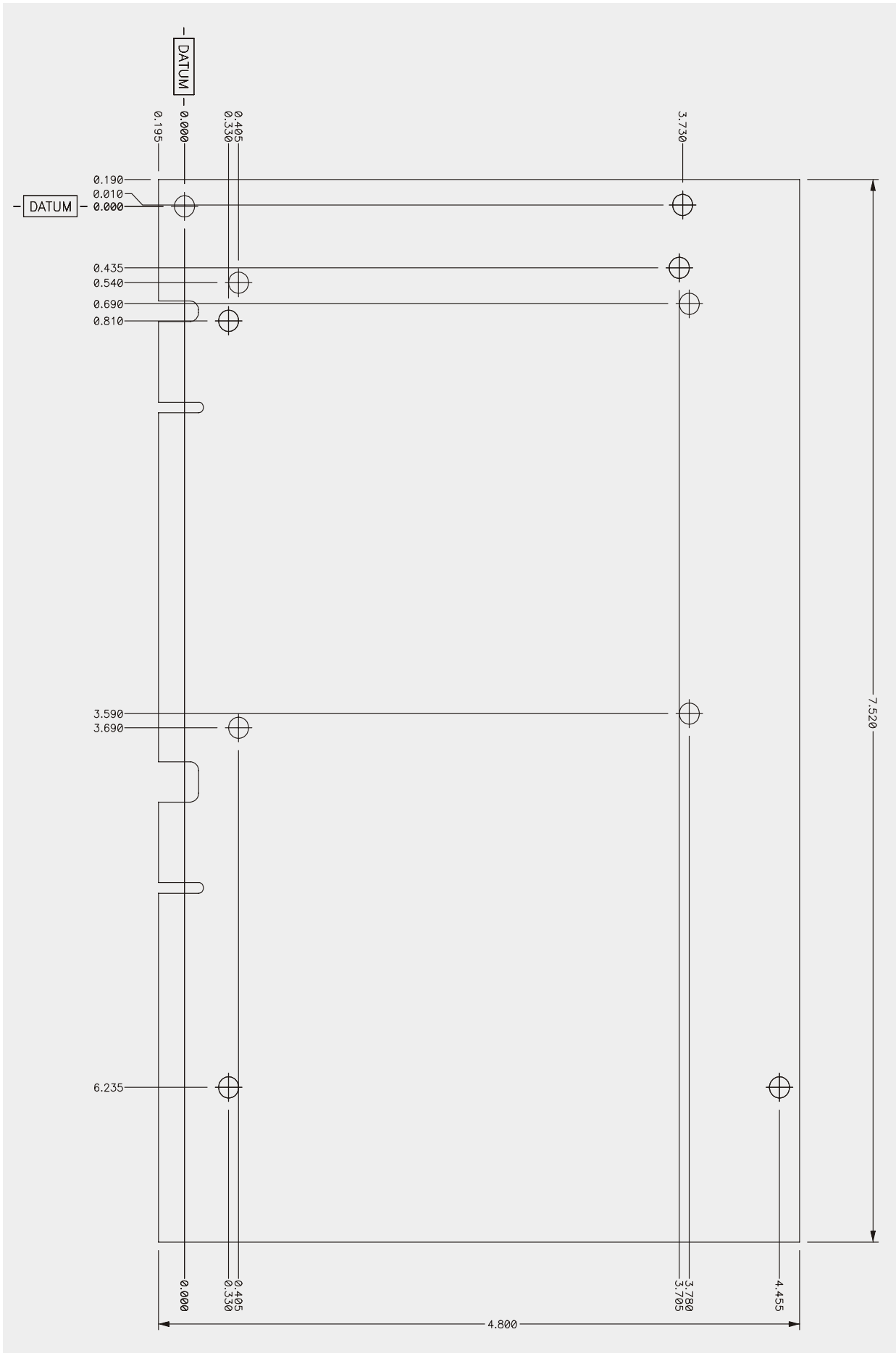
C.2 ASSEMBLY BOTTOM DIAGRAM



C.3 CONNECTOR DIMENSIONS



C.4 MOUNTING HOLES



D. CONNECTOR PINOUTS

D.1 EPCI-100 CONNECTORS AND HEADERS

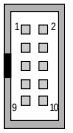
Connector	Description
J1	Serial Port 2
J2	Serial Port 1
J3	Floppy
J4 / J8	EIDE (Primary/Secondary)
J5	Parallel port
J6	Multifunction
J7	Hardware monitor
J9 / J10	Ethernet 1 and 0
J11 / J12	USB 1 / USB 0
J14	DVI
J15	External power
J16	CPU Fan
J17	Fan Header (monitored)
J18	CompactFlash disk
U9 / U10	SODIMM Socket
P1	PC/104+
BT1	Battery

D.1.1 J1 & J2 - Serial Ports 2 & 1 - RS-232

Note : NULL MODEM mode is available only on J2

Pin Number	
Signal	
DCD	1
RXD	3
TXD	5
DTR	7
GND	9

Top View

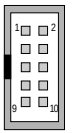


Pin Number	
	Signal
2	DSR
4	RTS
6	CTS
8	RI
10	N.C.

D.1.2 J1 - Serial Port 2 - RS-422/RS-485

Pin Number	
Signal	
RSV	1
RXB	3
TXB	5
RSV	7
GND	9

Top View

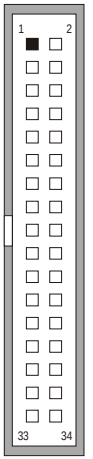


Pin Number	
	Signal
2	RSV
4	RXA
6	TXA
8	RSV
10	N.C.

D.1.3 J3 – Floppy Disk

Pin Number	
Signal	
GND	1
GND	3
GND	5
GND	7
GND	9
GND	11
GND	13
GND	15
N.C.	17
GND	19
GND	21
GND	23
GND	25
N.C.	27
FDETECT	29
GND	31
N.C.	33

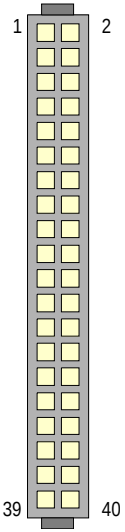
Top View



Pin Number	
	Signal
2	DENSEL#
4	N.C.
6	N.C.
8	Index#
10	MTR0#
12	DSEL1#
14	DSEL0#
16	MTR1#
18	DIR#
20	STEP#
22	WDATA#
24	WGATE#
26	TRK0#
28	WRPROT#
30	RDATA#
32	HDSEL#
34	DSKCHG#

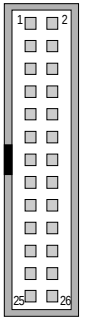
 # Active Low

D.1.4 J4/J8 - Primary & Secondary EIDE Connectors

Pin Number	Signal	Top View	Pin Number	Signal
RST#	1		2	GND
D7	3		4	D8
D6	5		6	D9
D5	7		8	D10
D4	9		10	D11
D3	11		12	D12
D2	13		14	D13
D1	15		16	D14
D0	17		18	D15
GND	19		20	N.C.
REQ	21		22	GND
IOW#	23		24	GND
IOR#	25		26	GND
IORDY	27		28	PRIMPDI
DACK#	29		30	GND
IRQ14 (J4)/IRQ15(J8)	31		32	N.C.
A1	33		34	DIAG#
A0	35		36	A2
CS0#	37		38	CS1#
ACT#	39		40	GND

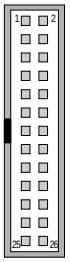
 # Active Low Signal

D.1.5 J5 - Parallel Port Connector - Standard Mode

Pin Number	Signal	Top View	Pin Number	Signal
STB#	1		2	ALF#
D0	3		4	ERR#
D1	5		6	INIT#
D2	7		8	SLCTIN#
D3	9		10	GND
D4	11		12	GND
D5	13		14	GND
D6	15		16	GND
D7	17		18	GND
ACK#	19		20	GND
BUSY	21		22	GND
PE	23		24	GND
SLCT	25		26	GND

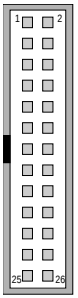
 # Active Low Signal

D.1.6 J5 - Parallel Port Connector - EPP Mode

Pin Number	Signal	Top View	Pin Number	Signal
WRITE#	1		2	DATASTB#
D0	3		4	N.C.
D1	5		6	N.C.
D2	7		8	ADDRSTRB#
D3	9		10	GND
D4	11		12	GND
D5	13		14	GND
D6	15		16	GND
D7	17		18	GND
INTR	19		20	GND
WAIT#	21		22	GND
N.C.	23		24	GND
N.C.	25		26	GND

 # Active Low Signal

D.1.7 J5 - Parallel Port Connector - ECP Mode

Pin Number	Signal	Top View	Pin Number	Signal
STROBE#	1		2	AUTOFD# HOSTACK[2]
PD0	3		4	FAULT#[1] PERIPHRQST#[2]
PD1	5		6	INIT#[1] REVERSERQST#[2]
PD2	7		8	SELECTIN#[1,2]
PD3	9		10	GND
PD4	11		12	GND
PD5	13		14	GND
PD6	15		16	GND
PD7	17		18	GND
ACK#	19		20	GND
BUSY, PERIPHACK[2]	21		22	GND
PERROR, ACKREVERSE[2]	23		24	GND
SELECT	25		26	GND

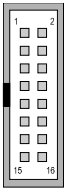
 # Active Low Signal, [1] Compatible Mode, [2] High Speed Mode

NOTE
For more information on the ECP protocol, please refer to the Extended Capabilities Port Protocol available from Microsoft Corporation, or contact our Technical Support Department.

D.1.8 J6 – Multifunction

Pin Number	Signal
KB:CLK	1
KB:DATA	3
VCC	5
SPEAKER	7
MOUSE:CLK	9
MOUSE:DATA	11
PBRES#	13
IDE:ACT#	15

Top View



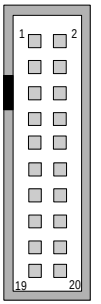
Pin Number	Signal
2	GND
4	GND
6	VCC
8	VCC
10	GND
12	GND
14	GND
16	VCC

 # Active Low Signal

D.1.9 J7 – Hardware Monitor Header

Pin Number	Signal
GND	1
N.C.	3
GPIO1/SMBDATA	5
APFLT#	7
EXFLT#	9
FANFLT#	11
CHASINT#	13
FAN_TACH1	15
FAN_TACH3	17
FAN_TACH5	19

Top View

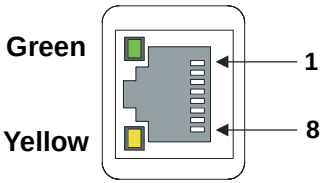


Pin Number	Signal
2	N.C.
4	GND
6	PIO2/SMBCLK
8	CPUFLT#
10	GND
12	GND
14	GND
16	FAN_TACH2
18	FAN_TACH4
20	FAN_TACH6

D.1.10 J9/J10 – Ethernet (Faceplate)

Signal	
TX+	1
TX-	2
RX+	3
NU*	4
NU*	5
RX-	6
NU*	7
NU*	8

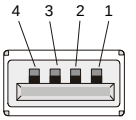
Front View



 # Line terminated with 75-ohm resistors.

D.1.11 J11(USB 1), J12 (USB 0) – Located on faceplate

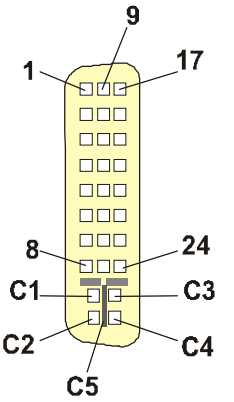
Signal	Pin
VCC	1
DATA-	2
DATA+	3
GND	4



D.1.12 J14 – DVI

Pin Number		Pin Number	
Signal		Signal	
TMDS_2-	1	HP_DET	16
TMDS_2+	2	TMDS_0-	17
SHIELD_2-4	3	TMDS_0+	18
Not connected	4	SHIELD_0-5	19
Not connected	5	Not connected	20
DDC_CLK	6	Not connected	21
DDC_DATA	7	SHIELD_CLK	22
VSYNC	8	TMDS_CLK+	23
TMDS_1-	9	TMDS_CLK-	24
TMDS_1+	10		
SHIELD_1-3	11	RED	C1
Not connected	12	GREEN	C2
Not connected	13	BLUE	C3
VCC	14	HSYNC	C4
GND	15	GND	C5

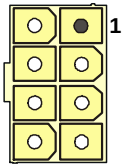
Front View



D.1.13 J15 - External Power

Signal	Pin #
+3.3V	1
+12V	2
N.C.	3
+3.3V	4
GND	5
GND	6
VCC	7
VCC	8

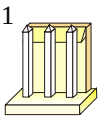
Top View



D.1.14 J16/J17 – CPU Fan and Fan Header

Pin #	Signal
1	Sense
2	+12V DC
3	GND

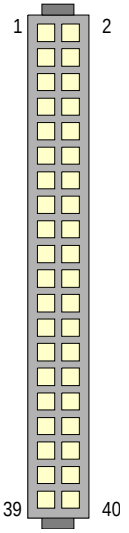
Front View



D.1.15 J18 - CompactFlash Disk Connector

Pin Number	
Signal	
D11	1
D12	3
D13	5
D14	7
D15	9
CS1#	11
DMACK#	13
DMARQ	15
PDIAG#	17
IRQ15	19
VCC	21
GND	23
RESET#	25
CSEL	27
A1	29
A0	31
D0	33
D1	35
D2	37
IOCS16#	39

Top View



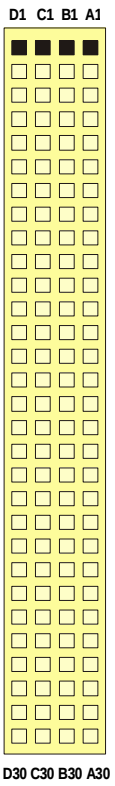
Pin Number	
	Signal
2	GND
4	D3
6	D4
8	D5
10	D6
12	D7
14	CS0#
16	IOR#
18	IOW#
20	VCC
22	VCC
24	GND
26	GND
28	A2
30	DASP#
32	IORDY#
34	D8
36	D9
38	D10
40	GND

 # Active Low

D.1.16 P1 – PC/104+

	A	B	C	D	
1	5V_KEY	N.C.	VCC	AD0	1
2	VI/O	AD2	AD1	VCC	2
3	AD5	GND	AD4	AD3	3
4	C/BE0#	AD7	GND	AD6	4
5	GND	AD9	AD8	GND	5
6	AD11	VI/O	AD10	N.C. (MM66EN)	6
7	AD14	AD13	GND	AD12	7
8	+3.3V	C/BE1#	AD15	+3.3V	8
9	SERR#	GND	SB0#	PAR	9
10	GND	PERR#	+3.3V	SDONE	10
11	STOP*	+3.3V	LOCK#	GND	11
12	+3.3V	TRDY#	GND	DEVSEL#	12
13	FRAME#	GND	IRDY#	+3.3V	13
14	GND	AD16	+3.3V	C/BE2#	14
15	AD18	+3.3V	AD17	GND	15
16	AD21	AD20	GND	AD19	16
17	+3.3V	AD23	AD22	+3.3V	17
18	IDSEL0	GND	IDSEL1	IDSEL2	18
19	AD24	C/BE3#	VI/O	IDSEL3	19
20	GND	AD26	AD25	GND	20
21	AD29	VCC	AD28	AD27	21
22	VCC	AD30	GND	AD31	22
23	REQ0#	GND	REQ1#	VI/O	23
24	GND	REQ2#	VCC	GNT0#	24
25	GNT1#	VI/O	GNT2#	GND	25
26	VCC	CLK0	GND	CLK1	26
27	CLK2	VCC	CLK3	GND	27
28	GND	INTD#	VCC	RESET#	28
29	+12V	INTA#	INTB#	INTC#	29
30	-12V	N.C.	NN.C.	3.3V_KEY	30

Top View



 # Active Low Signal

E. BIOS SETUP ERROR CODES

E.1 POST BEEP

POST beep codes are defined in the BIOS to provide low level tone indication when an error occurs during the BIOS initialization.

Beep codes consist of a combination of long and short beeps. They are described as follows:

Beep Codes

Post code	Beep Code	Description
41	**-*	Enterring the boot block recovery code (i.e. Main BIOS checksum error)
22	*-*-*	Error when getting the boot block flash ID code
33	*-*-*-*	Error when erasing the boot block flash
44	*-*-*-*-*	Error when programming the boot block flash
55	*-*	Success of the boot block recovery code. The board is ready to be manually reset.

Legend * = 1 Short beep code, ** = 1 Long beep code, - = Silence

E.2 POST MESSAGES

During the Power On Self Test (POST), if the BIOS detects an error requiring you to do something to fix, it will either sound a beep code or display a message.

If a message is displayed, it will be accompanied by:

"PRESS F1 TO CONTINUE, DEL TO ENTER SETUP".

E.3 ERROR MESSAGES

One or more of the following messages may be displayed if the BIOS detects an error during the POST.

CMOS BATTERY HAS FAILED

1. If it's the first boot, check for the onboard battery jumper W3. The board is shipped with W3 jumper set to OFF (onboard battery disconnected). This jumper must be shorted (ON) for proper battery operation.
2. CMOS battery is no longer functional. It should be replaced.

CMOS CHECKSUM ERROR

Checksum of CMOS is incorrect. This indicates that CMOS has become corrupt. This error may have been caused by a weak battery. Check the battery and replace if necessary.

DISK BOOT FAILURE, INSERT SYSTEM DISK AND PRESS ENTER

No boot device was found. This could mean either a boot drive was not detected or the drive does not contain proper system boot files. Insert a system disk into Floppy Drive A and press Enter. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also be sure the disk is formatted as a boot device. Then reboot the system.

KEYBOARD ERROR OR NO KEYBOARD PRESENT

Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.
If you are purposely configuring the system without a keyboard, set the error halt condition in Setup to HALT ON ALL, BUT KEYBOARD. This will cause BIOS to ignore the missing keyboard and continue the boot.

OFFENDING SEGMENT

This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem cannot be isolated.

PRESS F1 TO DISABLE NMI, F2 TO REBOOT

When BIOS detects a Non Maskable Interrupt condition, this will allow you to disable the NMI and continue to boot, or you can reboot the system with the NMI enabled.

PhoenixBIOS 4.0 Release 6.0 POST Tasks and Beep Codes

When you turn on or reset an IBM- compatible PC, the BIOS first performs a number of tasks, called the **Power- On- Self- Test** (**POST**). These tasks test and initialize the hardware and then boot the Operating System from the hard disk. At the beginning of each POST task, the BIOS outputs the **test- point error code** to I/ O port 80h. Programmers and technicians use this code during trouble shooting to establish at what point the system failed and what routine was being performed. Some motherboards are equipped with a seven-segment LED display that displays the current value of port 80h. For production boards which do not contain the LED display, you can purchase an installable "Port 80h" card that performs the same function. If the BIOS detects a terminal error condition, it issues a terminal- error beep code (See following), attempts to display the error code on upper left corner of the screen and on the port 80h LED display, and halts POST. It

attempts repeatedly to write the error to the screen. This attempt may "hash" some CGA displays.
If the system hangs before the BIOS can process the error, the value displayed at the port 80h is the last test performed. In this case, the screen does not display the error code.

Terminal POST Errors

There are several POST routines that require success to finish POST. If they fail, they issue a **POST Terminal Error** and shut down the system. Before shutting down the system, the error handler issues a beep code signifying the test point error, writes the error to port 80h, attempts to initialize the video, and writes the error in the upper left corner of the screen (using both mono and color adapters). The routine derives the beep code from the test point error as follows:

1. The 8- bit error code is broken down to four 2- bit groups.
2. Each group is made one- based (1 through 4) by adding 1.
3. Short beeps are generated for the number in each group.

Example: **Testpoint 16h = 00 01 01 10 = 1- 2- 2- 3 beeps**

POST Task Routines

The following is a list of the Test Point codes written to port 80h at the start of each routine, the beep codes issued for terminal errors, and a description of the POST routine. Unless otherwise noted, these codes are valid for PhoenixBIOS 4.0 Release 6.0.

NOTE: The following routines are sorted by their test point numbers assigned in the BIOS code. Their actual order as executed during POST can be quite different.

02h Verify Real Mode	03h Disable Non- Maskable Interrupt (NMI)
04h Get CPU type	06h Initialize system hardware
08h Initialize chipset with initial POST values	09h Set IN POST flag
0Ah Initialize CPU registers	0Bh Enable CPU cache
0Ch Initialize caches to initial POST values	0Eh Initialize I/ O component
0Fh Initialize the local bus IDE	10h Initialize Power Management
11h Load alternate registers with initial POST values	12h Restore CPU control word during warm boot
13h Initialize PCI Bus Mastering devices	14h Initialize keyboard controller
16h 1- 2- 2- 3 BIOS ROM checksum	17h Initialize cache before memory autosize
18h 8254 timer initialization	1Ah 8237 DMA controller initialization
1Ch Reset Programmable Interrupt Controller	20h 1- 3- 1- 1 Test DRAM refresh
22h 1- 3- 1- 3 Test 8742 Keyboard Controller	24h Set ES segment register to 4 GB
26h Enable A20 line	28h Autosize DRAM

29h Initialize POST Memory Manager	2Ah Clear 512 KB base RAM
2Ch 1- 3- 4- 1 RAM failure on address line ***xxxx*** *	2Eh 1- 3- 4- 3 RAM failure on data bits ***xxxx*** * of low byte of memory bus
2Fh Enable cache before system BIOS shadow	30h 1- 4- 1- 1 RAM failure on data bits ***xxxx*** * of high byte of memory bus
32h Test CPU bus- clock frequency	33h Initialize Phoenix Dispatch Manager
36h Warm start shut down	38h Shadow system BIOS ROM
3Ah Autosize cache	3Ch Advanced configuration of chipset registers
3Dh Load alternate registers with CMOS values	42h Initialize interrupt vectors
45h POST device initialization	46h 2- 1- 2- 3 Check ROM copyright notice
48h Check video configuration against CMOS	49h Initialize PCI bus and devices
4Ah Initialize all video adapters in system	4Bh QuietBoot start (optional)
4Ch Shadow video BIOS ROM	4Eh Display BIOS copyright notice
50h Display CPU type and speed	51h Initialize EISA board
52h Test keyboard	54h Set key click if enabled
58h 2- 2- 3- 1 Test for unexpected interrupts	59h Initialize POST display service
5Ah Display prompt "Press F2 to enter SETUP"	5Bh Disable CPU cache
5Ch Test RAM between 512 and 640 KB	60h Test extended memory
62h Test extended memory address lines	64h Jump to UserPatch1
66h Configure advanced cache registers	67h Initialize Multi Processor APIC
68h Enable external and CPU caches	69h Setup System Management Mode (SMM) area
6Ah Display external L2 cache size	6Bh Load custom defaults (optional)
6Ch Display shadow- area message	6Eh Display possible high address for UMB recovery
70h Display error messages	72h Check for configuration errors
76h Check for keyboard errors	7Ch Set up hardware interrupt vectors
7Eh Initialize coprocessor if present	80h Disable onboard Super I/ O ports and IRQs
81h Late POST device initialization	82h Detect and install external RS232 ports
83h Configure non- MCD IDE controllers	84h Detect and install external parallel ports
85h Initialize PC- compatible PnP ISA devices	86h Re- initialize onboard I/ O ports.
87h Configure Motheboard Configurable Devices (optional)	88h Initialize BIOS Data Area
89h Enable Non- Maskable Interrupts (NMIs)	8Ah Initialize Extended BIOS Data Area
8Bh Test and initialize PS/ 2 mouse	8Ch Initialize floppy controller
8Fh Determine number of ATA drives (optional)	90h Initialize hard- disk controllers
91h Initialize local- bus hard- disk controllers	92h Jump to UserPatch2
93h Build MPTABLE for multi- processor boards	95h Install CD ROM for boot
96h Clear huge ES segment register	97h Fixup Multi Processor table
98h 1- 2 Search for option ROMs. One long, two short beeps on	checksum failure
99h Check for SMART Drive (optional)	9Ah Shadow option ROMs
9Ch Set up Power Management	9Dh Initialize security engine (optional)
9Eh Enable hardware interrupts	9Fh Determine number of ATA and SCSI drives
A0h Set time of day	A2h Check key lock
A4h Initialize Typematic rate	A8h Erase F2 prompt
AAh Scan for F2 key stroke	ACh Enter SETUP
AEh Clear Boot flag	B0h Check for errors
B2h POST done - prepare to boot operating system	B4h 1 One short beep before boot
B5h Terminate QuietBoot (optional)	B6h Check password (optional)
B9h Prepare Boot	BAh Initialize DMI parameters
BBh Initialize PnP Option ROMs	BCh Clear parity checkers

BDh Display MultiBoot menu	BEh Clear screen (optional)
BFh Check virus and backup reminders	C0h Try to boot with INT 19
C1h Initialize POST Error Manager (PEM)	C2h Initialize error logging
C3h Initialize error display function	C4h Initialize system error handler
C5h PnPnd dual CMOS (optional)	C6h Initialize notebook docking (optional)
C7h Initialize notebook docking late	C8h Force check (optional)
C9h Extended checksum (optional)	D2h Unknown interrupt
E0h Initialize the chipset	E1h Initialize the bridge
E2h Initialize the CPU	E3h Initialize system timer
E4h Initialize system I/ O	E5h Check force recovery boot
E6h Checksum BIOS ROM	E7h Go to BIOS
E8h Set Huge Segment	E9h Initialize Multi Processor
EAh Initialize OEM special code	EBh Initialize PIC and DMA
ECh Initialize Memory type	EDh Initialize Memory size
EEh Shadow Boot Block	EFh System memory test
F0h Initialize interrupt vectors	F1h Initialize Run Time Clock
F2h Initialize video	F3h Initialize System Management Mode
F4h 1 Output one beep before boot	F5h Boot to Mini DOS
F6h Clear Huge Segment	F7h Boot to Full DOS

* If the BIOS detects error 2C, 2E, or 30 (base 512K RAM error), it displays an additional word- bitmap (***xxxx***) indicating the address line or bits that failed. For example, "2C 0002" means address line 1 (bit one set) has failed. "2E 1020" means data bits 12 and 5 (bits 12 and 5 set) have failed in the lower 16 bits. Note that error 30 cannot occur on 386SX systems because they have a 16 rather than 32- bit bus. The BIOS also sends the bitmap to the port- 80 LED display. It first displays the check point code, followed by a delay, the high- order byte, another delay, and then the low- order byte of the error. It repeats this sequence continuously.

F. BIOS UPDATE & EMERGENCY PROCEDURE

BIOS UPDATE PROCEDURE

The BIOS update procedure can be found with the Emergency Recovery procedure on our ftp site: ftp://ftp.kontron.ca/Support in the FAQ section:

Download the FAQ# KC_0028 at location:

ftp://ftp.kontron.ca/Support/Support_FAQ - Questions & Answers/

EMERGENCY PROCEDURE

Symptoms:

- No POST code on a power up (when using a POST card).
- Board does not boot, even after usual hardware and connection verifications.
- At power up, there is floppy disk led activity, which is one sign that the BIOS as detected a corrupted BIOS CRC prior POST and falled back automatically to Emergency Recovery Mode looking for the floppy Emergency disk.

Please go on our FTP site in order to get the latest Emergency Recovery BIOS for that specific product.

BIOS maybe found at: Ftp://Ftp.Kontron.ca/Support/BIOS_Emergency/

Emergency Recovery Procedure is included within the Zip file of the Emergency BIOS to download. Latest Emergency Recovery procedure can be found on the FAQ section of the FTP site under FAQ # KC_0028 at location:

ftp://ftp.kontron.ca/Support/Support_FAQ - Questions & Answers/

G. GETTING HELP

At Kontron, we take great pride in our customer's successes. We strongly believe in providing full support at all stages of your product development.

If at any time you encounter difficulties with your application or with any of our products, or if you simply need guidance on system setups and capabilities, you may contact our Technical Support department at:

CANADIAN HEADQUARTERS
Tel. (450) 437-5682
Fax: (450) 437-8053

If you have any questions about Kontron, our products or services, you may reach us at the above numbers or by writing to :

Kontron Inc..
616 Curé Boivin
Boisbriand, Québec
J7G 2A7 Canada

LIMITED WARRANTY

Kontron Inc, ("The seller") warrants its boards to be free from defects in material and workmanship for a period of two (2) years commencing on the date of shipment. The liability of the seller shall be limited to replacing or repairing, at the seller's option, any defective units. Equipment or parts, which have been subject to abuse, misuse, accident, alteration, neglect, or unauthorized repair are not covered by this warranty. This warranty is in lieu of all other warranties expressed or implied.

Returning Defective Merchandise

If your Kontron product malfunctions, please do the following before returning any merchandise:

1) Call our Technical Support department in Canada at (450) 437-5682. Make certain you have the following at hand:

- The Kontron Invoice number
- Your purchase order number
- The serial number of the defective board.

2) Give the serial number found on the back of the board and explain the nature of your problem to a service technician.

3) If the problem cannot be solved over the telephone, the technician will further instruct you on the return procedure.

4) Prior to returning any merchandise, make certain you receive an RMA number from Kontron's Technical Support and clearly mark this number on the outside of the package you are returning. To request a number, follow these steps:

- Make a copy of the request form on the following page.
- Fill out the form and be as specific as you can about the board's problem.
- Fax it to us.

5) When returning goods, please include the name and telephone number of a person whom we can contact for further explanations if necessary. Where applicable, always include all duty papers and invoice(s) associated with the item(s) in question.

6) When returning a Kontron board:

   i) Make certain that the board is properly packed: Place it in an antistatic plastic bag and pack it in a rigid cardboard box.

   ii) Ship prepaid to (but not insured, since incoming units are insured by Kontron):

Kontron Inc.
616 Curé Boivin
Boisbriand, Québec
J7G 2A7 Canada

RETURN TO MANUFACTURER AUTHORIZATION REQUEST

Contact Name : _____

Company Name : _____

Street Address : _____

City : _____ Province/State: _____

Country : _____ Postal/Zip Code: _____

Phone Number : _____ Extension : _____

Fax Number : _____

Serial Number	Failure or Problem Description	P.O. # (if not under warranty)

Fax this form to Kontron's Technical Support department in Canada at (450) 437-8053