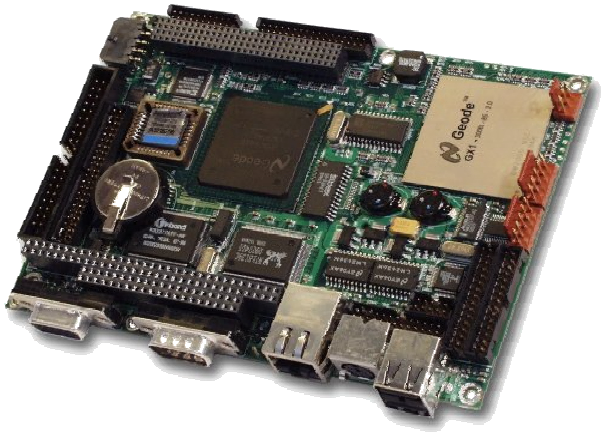
User's Hardware Manual

GX1LCD

Boards



Ver. 1.3 – 19. September 2002.

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Document revision history.

Revision	Date	By	Comment
1.0	14. July. 2001	PJA	Initial release
1.1	9. Nov. 2001	PJA	Production update
1.2	21. May. 2002	JSN	Manual update
1.3	19.Sept. 2002	PJA	EN60950 requirement added. Inside renamed to Kontron Technology.

Kontron Technology Technical Support and Services

If you have questions about installing or using your Kontron Technology Product, check this User's Manual first – you will find answers to most questions here. To obtain support, please contact your local Distributor or Field Application Engineer (FAE).

Before Contacting Support:
Before requesting technical support be prepared to provide as much information as possible:

- CPU Board
  1. Type.
  2. Part-number (Number starting with "552" (GX1LCD/3.5") or "553"(GX1LCD/S)).
  3. Serial Number.
- Configuration
  1. CPU clock speed.
  2. DRAM Type and Size.
  3. BIOS Revision (Find the Version Info in the BIOS Setup in the Inside Section).
  4. BIOS Settings different than *Default* Settings (Refer to the Software Manual).
- System
  1. O/S Make and Version.
  2. Driver Version numbers (Graphics, Network, and Audio).
- Attached Hardware: Harddisks, Floppy, LCD Panels etc.

Table of contents

1. Introduction

This manual describes the GX1LCD boards made by KONTRON Technology A/S. The boards will also be denoted GX1LCD or GX1 family if no differentiation is required.

All boards are based on the Geode GX1 processor with MMX enhancement from National ®. This processor is abbreviated GX1 in this manual.

Use of this manual implies a basic knowledge of PC-AT hard- and software. This manual is focused on describing the GX1LCD Board's special features and is not intended to be a standard PC-AT textbook.

New users are recommended to study the short installation procedure stated in chapter 2 before switching-on the power.

All configuration and setup of the CPU board is either done automatically or by the user in the CMOS setup menus. No jumper configuration is required.

2. Installation procedure

2.1 Check the Kit Contents

The standard shipment should contain the following items:
1.) GX1LCD Board.
2.) Passive cooler (Mounted).
3.) Power Supply Adapter

For OEM shipments this contents list may be different than listed.

The optional accessory for the GX1 family is currently:

1. PC133 SDRAM module for SODIMM144 socket.
2. Audio Bracket for Audio Connector (JPAUX) for GX1LCD/S.
3. Audio Bracket for Audio Connectors (BRACK1, 2) for GX1LCD/3.5".
4. Panellink Module for installing in the Video Interface Module SODIMM144 connector.
5. DVI-S100 Module for installing in the Video Interface Module SODIMM144 connector.
6. LCDADPT 3V3 module for installing in the Video Interface Module SODIMM144 connector for support of Direct LCD connections on GX1LCD/3.5" boards.
7. DSTN module for installing in the Video Interface Module SODIMM144 connector for support of DSTN panels.

8. ATX power supply interface cable for GX1LCD/3.5" boards.
9. Standard 40-pin Internal IDE Harddisk Cable for Harddisk Connector (IDE1).
10. Harddisk Cable, 2mm to 3.5" Disks for Harddisk connector (IDE2) for GX1LCD/3.5".
11. Harddisk Cable, 2mm to 2.5" Disks for Harddisk connector (IDE2) for GX1LCD/3.5".
12. Standard 34-pin Internal Floppy Disk Drive Cable for Floppy Connector (FLOPPY) for GX1LCD/S.
13. Floppy Disk Drive Cable, 2mm, 34-pin, Internal for Floppy Connector (FLOPPY) for GX1LCD/3.5".
14. Y-cable for Keyboard and PS/2 Mouse for Keyboard Connector (KBD).
15. PS/2 Mouse Bracket for PS/2 Mouse Connector (JPMSE).
16. Serial and Parallel Port Bracket for Serial Com2 (COM2) and Parallel Port (PRINTER) Connectors for GX1LCD/S.
17. Serial Port Cable for COM3 and 4 (COM3, 4) for GX1LCD/S.
18. Serial Port Cable (2mm) for COM2 (COM2) for GX1LCD/3.5".
19. Parallel Port Cable (2mm) for PRINTER (PRINTER) for GX1LCD/3.5".
20. USB Bracket for USB Pin-header (USB) for GX1LCD/S.

21. GX1LCD Manual and Driver CDROM.

22. M-Systems DiskOnChip 2000 for DiskOnChip Socket (GX1LCD/S only).
23. Compact Flash card for insertion in Compact Flash Connector (CFLASH).

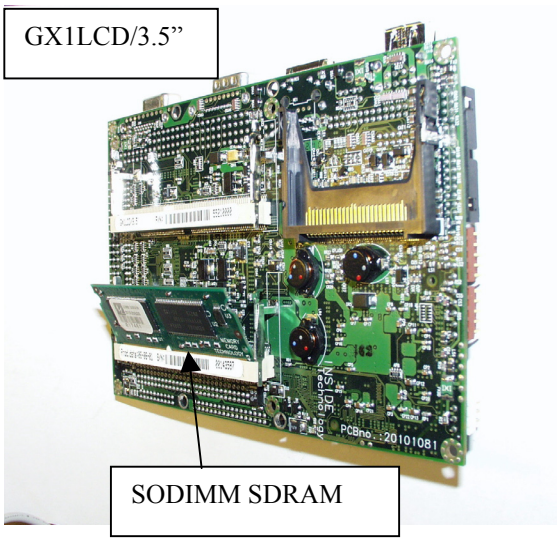
For an updated accessory list for the GX1LCD Product Family please check the Kontron Technology WorldWideWeb: www.inside.dk or contact the FAE. Updated drivers and manuals are also available here.

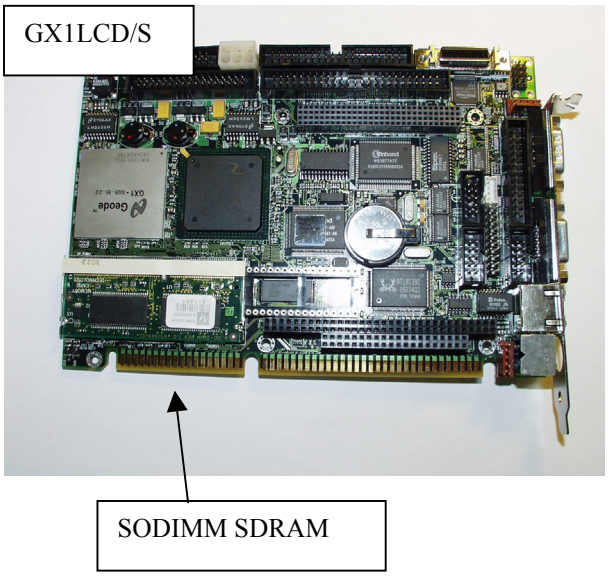
2.2 Installing the Board

To get the board running, follow these steps. The Board will have CPU and Cooler mounted when shipped from Kontron Technology.

1. Turn off the power supply.

2. Insert the SODIMM144 SDRAM module. Be careful to push it in the slot before rotating it into position. The locking mechanism will typically make a *click* when the module is locked in position. When running 100MHz clock speed on the SDRAM, the SDRAM must be rated for PC133. At 83MHz clock speed the SDRAM used can be PC100 rated.





3. Insert all external cables for hard disk, floppy, keyboard etc. except for flat panel. **A CRT monitor must be connected in order to change CMOS settings to flat panel support**.

4. Connect power supply to the board by the PWRCON connector and insert the board in a backplane if required (GX1LCD/S only).

5. Turn on the power.

6. Enter the BIOS setup by pressing the “F2” key during boot up. Setup the Processor clock speed in the Main menu. Refer to the Software Manual for details.

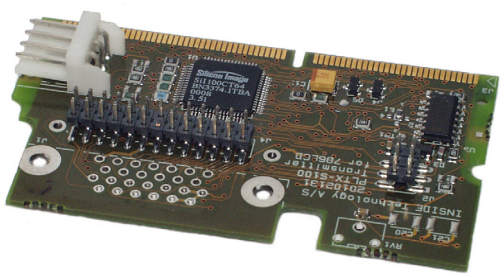
7. If Flat Panel Display is to be utilised, make sure the Panel type and Panel voltage in the BIOS setup in the Inside Utilities menu is correct before turning off the power and connecting the display cable. Refer to next Section for a description of the options for mounting a LCD Panel to the GX1LCD/3.5” and GX1LCD/S Boards.

Note: In case of corrupt CMOS settings the board may display an error message followed by “Press F1 to continue”. To clear the non-PnP part of the CMOS (ESCD area – Extended System Configuration Data area) enter the Advanced menu and set “Reset Configuration Data” to *Yes*. At next boot the setting will be reset back to *No*.
To clear all CMOS settings, including Password protection, remove the battery for approximately 1 minute then reinsert it.

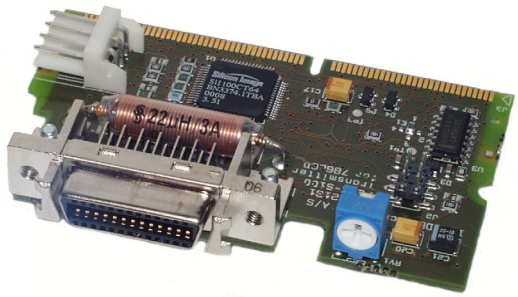
2.3 LCD Panel Mounting Options

The For GX1LCD/S boards flat panels can be connected directly to the onboard 50-pin LCD PANEL connector or via the Panellink connection PNLLINK connector (see Connector Layout).

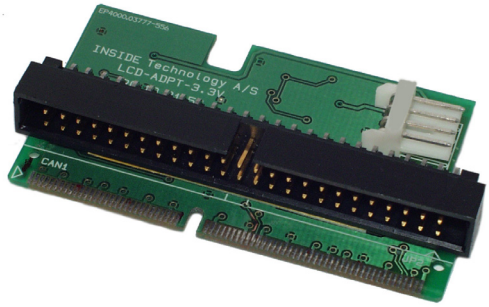
For GX1LCD/3.5" boards flat panels can be connected using a module connected to the VGA SODIMM connector (See Connector Layout). Modules for Direct digital, Panellink, DVI- and DSTN connection are available from Kontron Technology.



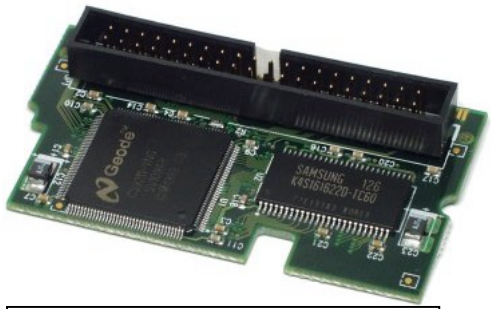
Internal Panellink SODIMM Module for GX1LCD/3.5"



External Panellink SODIMM Module for GX1LCD/3.5"



50-pole LCD Connector SODIMM Module for GX1LCD/3.5"



DSTN SODIMM Module for GX1LCD/3.5"

2.4 Requirement according to EN60950 :

Users of 786LCD boards should take care when designing chassis interface connectors in order to fulfil the EN60950 standard :

When an interface/connector has a VCC (or other power) pin, that is directly connected to the VCC (or other) plane :

To protect the external power lines of peripheral devices the customer has to take care about :

- That the wires have the right diameter to withstand the maximum available power.
- That the enclosure of the peripheral device fulfils the fire protecting requirements of IEC/EN 60950.

Lithium Battery precautions:

CAUTION! Danger of explosion if battery is incorrectly replaced. Replace only with same or equivalent type recommended by manyfacturer. Dispose of used batteries according to the manufacturer's instructions.	**VORSICHT!** Explosionsgefahr bei unsachgemäßem Austausch der Batterie. Ersatz nur durch den selben oder einen vom Hersteller empfohlenen gleichwertigen Typ. Entsorgung gebrauchter Batterien nach Angaben des Herstellers.
ADVARSEL! Lithiumbatteri – Eksplosionsfare ved fejlagtig håndtering. Udskiftning må kun ske med batteri af samme fabrikat og type. Levér det brugte batteri tilbage til leverandøren.	**ADVARSEL** Eksplosjonsfare ved feilaktig skifte av batteri. Benytt samme batteritype eller en tilsvarende type anbefalt av apparatfabrikanten. Brukte batterier kasseres i henhold til fabrikantens instruksjoner.
VARNING Explosionsfara vid felaktigt batteribyte. Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren. Kassera använt batteri enligt fabrikantens instruktion.	**VAROITUS** Paristo voi räjähtää, jos se on virheellisesti asennettu. Vaihda paristo ainoastaan laltevalmistajan suosittelemaan tyyppiln. Hävitä käytetty paristo valmistajan ohjeiden mukaisesti.

3. System specification

The GX1LCD Family is based on the National Geode GX1 Processor with the chipset CS5530A. Configuration of the boards is done from the BIOS setup. Some features may additionally be reconfigured by user applications.

3.1 Configuration overview

The GX1LCD board family consist of four boards ranging from a low-cost board which provides basic PC functionality to a high-end board which provides improved interfacing to displays and improved performance as well as additional interfacing features. The configuration of these boards is listed below.

Model	GX1LCD/3.5" Standard	GX1LCD/3.5" Plus	GX1LCD/S Standard	GX1LCD/S Plus
Processor	200MHz	300 MHz	200 MHz	300 MHz
BIOS	Phoenix + Kontron Technology	Phoenix + Kontron Technology	Phoenix + Kontron Technology	Phoenix + Kontron Technology
Cooling	Passive	Passive	Passive	Passive
Chipset	National CS5530A	National CS5530A	National CS5530A	National CS5530A
DRAM Type	SDRAM, PC133	SDRAM, PC133	SDRAM, PC133	SDRAM, PC133
DRAM (Max)	128 MB	128 MB	128 MB	128 MB
Cache Type (GX1)	Level 1	Level 1	Level 1	Level 1
Cache (Kbyte)	16 Kb	16 Kb	16 Kb	16 Kb
M-Systems Disk on chip	No	No	DOC2000 Socket	DOC2000 Socket
Compact Flash Disk	CF Socket, Type I, II	CF Socket, Type I, II	CF Socket, Type I	CF Socket, Type I
HDD	2 x 2 EIDE (ATA-33)*	2 x 2 EIDE (ATA-33)*	2 EIDE (ATA-33)*	2 EIDE (ATA-33)*
FDD	2 x 1.44/2.88	2 x 1.44/2.88	2 x 1.44/2.88	2 x 1.44/2.88
Bus	ISA PC/104	ISA PC/104+	ISA PC/104	ISA PC/104 +
Graphics Ctrl.	National CS5530A	National CS5530A	National CS5530A	National CS5530A
Video RAM	UMA Up to 4MB	UMA Up to 4MB	UMA Up to 4MB	UMA Up to 4MB
Display	CRT/LCD 18 bit	CRT/LCD 18 bit	CRT/LCD 18 bit	CRT/LCD 18 bit
VGA / PCI SODIMM Extension Connector	Yes	Yes	No	No

Model	GX1LCD/3.5" Standard	GX1LCD/3.5" Plus	GX1LCD/S Standard	GX1LCD/S Plus
Resolution	640 x 480 800 x 600 1024 x 768 (16bpp) 1280 x 1024(8bpp)	640 x 480 800 x 600 1024 x 768 (16bpp) 1280 x 1024(8bpp)	640 x 480 800 x 600 1024 x 768 (16bpp) 1280 x 1024(8bpp)	640 x 480 800 x 600 1024 x 768 (16bpp) 1280 x 1024(8bpp)
PanelLink, 24 bit MSB aligned	With VGA SODIMM Adapter Module	With VGA SODIMM Adapter Module	No	No
USB	12 MBit 2 Ch.	12 MBit 2 Ch.	12 MBit 2 Ch.	12 MBit 2 Ch.
IrDA	Optional	Optional	Optional	Optional
Ethernet	Realtek 8139C 10/100 MBit	Realtek 8139C 10/100 MBit	Realtek 8139C 10/100 MBit	Realtek 8139C 10/100 Mbit
Serial Ports	2 x RS232C	2 x RS232C or 1 x RS232C + 1 x RS422/485	2 x RS232C	4 x RS232C or 3 x RS232C + 1 x RS422/485
Parallel Port	SPP/ECP/EPP	SPP/ECP/EPP	SPP/ECP/EPP	SPP/ECP/EPP
SW Watchdog	Yes	Yes	Yes	Yes
Temperature Monitor	No	Yes	No	Yes
Power Supply Monitoring	No	Yes	No	Yes
Fan Connector + Supervision	No	Yes	No	Yes
Keyboard	PC/AT	PC/AT	PC/AT	PC/AT
Mouse	PS/2	PS/2	PS/2	PS/2
Speaker	On Board	On Board	On Board	On Board
Sound, Line In/Out, Mic. In, Speaker Out, CDROM In	No	Sound Bracket*	No	Sound Bracket*
Battery	Lithium	Lithium	Lithium	Lithium
Real Time Clock	Yes	Yes	Yes	Yes
General I/O	8 (2x4)	8 (2x4)	8	8
EMI	EN-55022/ EN-50082	EN-55022/ EN-50082	EN-55022/ EN-50082	EN-55022/ EN-50082
Operating Temp.	0 - 60 °C.	0 - 60 °C.	0 – 60 °C.	0 - 60 °C.
Dimensions	145 x 102 mm 5.7" x 4.0"	145 x 102 mm 5.7" x 4.0"	179.5 x 123 mm 7.1" x 4.8"	179.5 x 123 mm 7.1" x 4.8"

* O/S support restrictions apply; refer to Software manual for details.

3.2 Component main data

The main data for the functions and components on the board are listed below. Availability of some of the features depends on the configuration as listed above. For further details, refer to chapter 3.3 and the connector definitions in chapter 5.

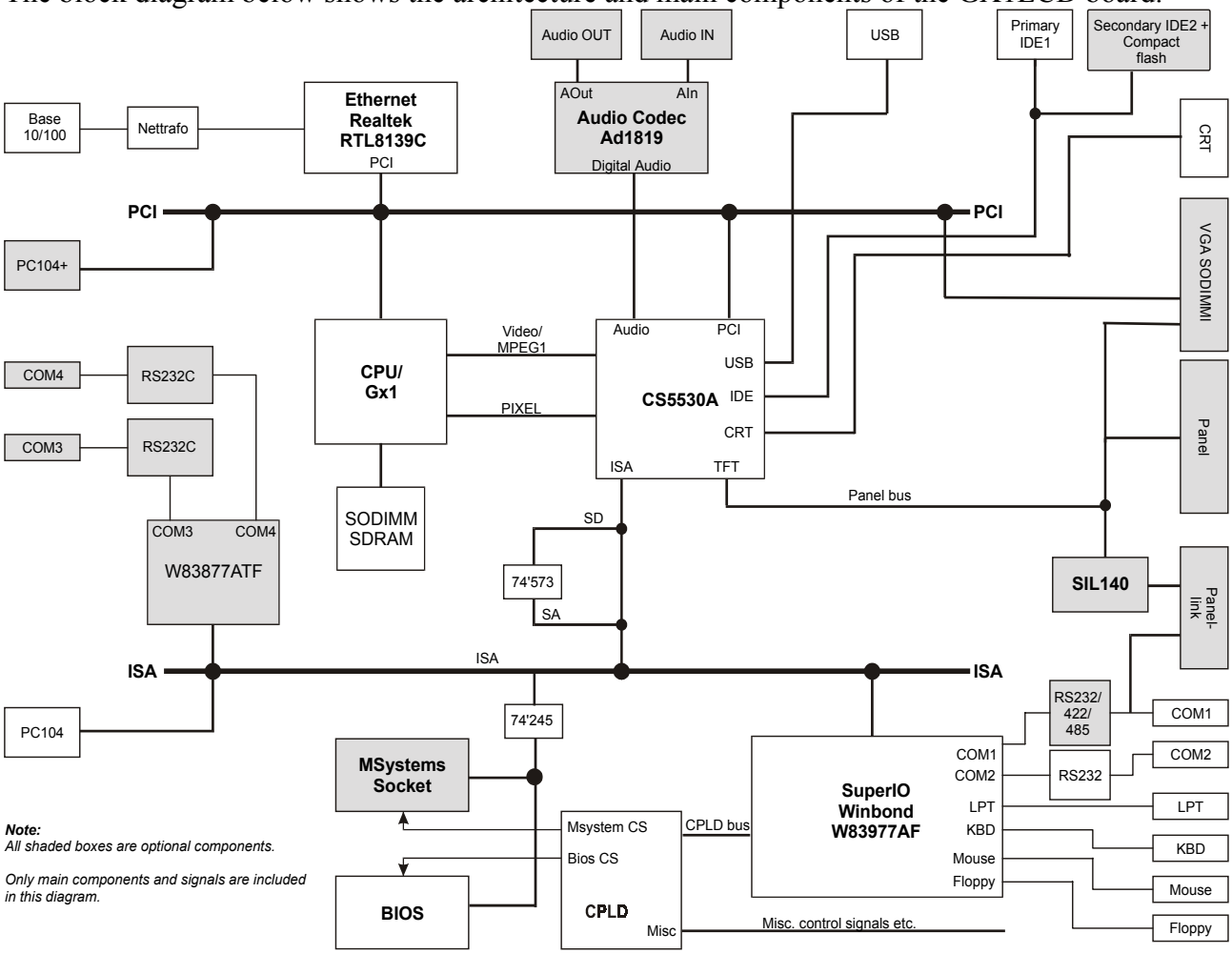
Processor	National Geode GX1processor with MMX enhancement (GX1)
Cache	Build in 16kB level 1 write-back cache in processor. The GX1 processor does not support external cache.
CPU Clock rate	External: PCI clock (33MHz) Internal: Configurable to 133, 200, and 300MHz* in the BIOS. Maximum frequency depends on the processor mounted on the board. (*depending on CPU mounted).
Chipset/Companion chip	National CS5530A.
System Clock Rate	33MHz PCI-bus. Internal clock multiplier in GX1 provides internal frequency.
SDRAM memory	SODIMM 144 pin form factor Operating voltage: 3.3V **SDRAM modules must comply with the PC100 specification if running at 83MHz SDRAM speed (Setup in the Main menu in the BIOS).** **SDRAM modules must comply with the PC133 specification if running at 100MHz SDRAM speed (Setup in the Main menu in the BIOS).** Up to 128MB supported.
Plug and Play features	PCI and ISA plug and play provided by BIOS On-board I/O devices are reallocated if other devices are found.
Graphics – XPRESS Graphics	XPRESS Graphics controlled by the GX1 CPU and the Companion chip. CRT and TFT interface is provided. Refer to section 3.3.2 for details on operation modes. See the software manual for details on driver installation and support for various operating systems.
Flat Panel Interface	A flat panel connector is provided in order to interface to a wide range of displays. Selection of display is performed in the BIOS, which will program refresh rates and timing of the graphics controller.
PanelLink	Supports 24 bit display interface with dotclock up to 65MHz. Transmission is performed at up to 650MHz on 4 differential lines at up to 10m distance.
Ethernet	10Base-T and 100Base-T Ethernet is supported (IEEE802.3, [6]). The Realtek 8139C Ethernet controller provides PCI bus-mastering operation for improved performance.

USB	USB controller integrated in the CS5530A companion chip is used. Two 12MBps USB channels are provided. USB Legacy is currently not supported.
M-systems Disk on Chip	A DIP32 connector is provided to support the M-systems Disk on Chip 2000 flash disk system. GX1LCD/S Boards only.
BIOS	Phoenix PICO BIOS v. 4.0. VSA (Virtual System Architecture) code from Cyrix corp.
Watchdog circuit	Supervision of power supply, fan-current and temperature. A watchdog timer is provided to reboot in case of system lockup. These features are configured in the CMOS setup. See the software manual for details.
Real-Time-Clock and CMOS memory	System configuration, date and time are maintained by CMOS memory with battery backup.
On-board Peripheal interfaces	AT-keyboard interface, PS/2 mouse interface, RS232C interface. Charge pump driver requiring 5V only. RS232C or 485 interface. Charge pump driver requiring 5V only. All RS232/RS485 ports are controlled by NS16550 comp. UART. Parallel printer interface (Centronic, ECP, EPP mode). EIDE hard disk interface with support for Ultra DMA33 mode (Mode 2). Compact flash connector for flash disk. Floppy drive interface (2 x 360kB to 2.88MB)
EMI	All Peripheral interfaces intended for connection to external equipment are EMI protected.
ISA-bus	The ISA bus is made available on the Edge connector and by the PC104 bus connector. ISA bus interface does not support Bus-mastering.
PCI-bus	A PC104+ extension compliant to the *PC104Plus Specification v1.0* provides a PCI bus with support for up to 3 bus masters. The bus operates at 3.3V signal levels. A 5V supply is provided in the connector. 3.3V supply is provided for light loads.
Power supply	External power supplies: VCC Supply: +5V +5% +12V Supply +12V ± 5% -12V Supply -12V ± 5% All functions on the board can operate from a 5V supply only. Connection of +/-12V can be made for external ISA/PC104 boards connected to the board.

Power Consumption	Approximately 4-8W depending on CPU and clock speed selected.
Battery	Exchangeable 3.0V Lithium battery for onboard RTC. Manufacturer Toshiba / Part-number CR2032. Approximate 9 years retention. Battery is protected against internal and external shorting according to UL requirements. **CAUTION: Danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.**
Environmental Conditions	**Operating**: 0°C – 60°C operating temperature (forced cooling). It is the customer's responsibility to provide sufficient airflow to/from the board. 10% - 90% relative humidity (non-condensing) **Storage**: -10°C – 85°C 5% - 95% relative humidity (non-condensing)
Audio	Audio based on AC97 codec. The following inputs/outputs are provided: Line in, CD-ROM in, Microphone in (mono), Line out, and Speaker out. Audio bracket is optionally supplied for mini-jack connection. VSA (Virtual System Architecture) emulation of Sound Blaster 16.
Dimensions	GX1LCD/3.5": 145 mm x 102 mm x 30 mm (incl. Passive cooler). GX1LCD/S: 179.5 mm x 123 mm x 26 mm (incl. Passive cooler).

3.3 System overview

The block diagram below shows the architecture and main components of the GX1LCD board.



The two key components on the board are the National GX1 CPU and the CS5530A companion chip. These two devices provide the ISA and PCI bus to which all the major components are attached.

All shaded components are optional and are therefore only provided in some configurations.

The following sections will provide additional details about the functions of the board, shaded paragraphs indicate that the availability will depend on the model; check the differences in section 3.1.

3.3.1 CPU/GX1 and CS5530A

The National GX1 CPU along with the CS5530A companion chip provide the basic functionality and busses of the system:

- Interface to SDRam, 64 bit databus. PC100/ PC133 compliant SDRAM must be used.
- PCI interface provided by the GX1 CPU.
- PCI to ISA bridge provided by the 5530A.
- VGA-controller with video memory shared with system memory (UMA). The image data is transferred to the companion chip by means of the *Pixel* bus.

- A maximum of 4MB Video memory (UMA) can be shared with system memory. If a graphics resolution change requires an increased amount of graphics memory, the system must be rebooted, as there is no way system DRAM can be recovered from the operating system.
- CRT and TFT interface. Data is provided by the *Pixel* and *Video* interface from the CPU. The TFT interface and the SA part of the ISA bus share pins as described later.
- *Video* interface from the GX1 to the 5530. This data-stream is buffered and multiplexed with the Pixel bus for windowed video viewing. This interface may assist the processor in connection with motion picture decoding.
- USB integrated in the 5530.
- IDE interface supporting Ultra DMA. Two connectors are provided: A standard IDE interface on the primary controller and a compact flash and 40-pin connector on the secondary controller
- Digital audio interface to an AC97 compliant audio codec.

3.3.2 XPRESS Graphics

As mentioned previously, the XPRESS Graphics is based on the GX1 CPU and the CS5530A Companion chip.
This graphics controller is very cost efficient since almost no additional components are required. This is achieved by using the SDRAM as frame-buffer and by integrating the graphics engine and display interface in the GX1 CPU and the CS5530A companion chip.
This controller provides a CRT as well as a TFT interface which support the modes listed below:

Resolution	BPP	Refresh/ Hz	Dotclock/ MHz	TFT bits	CRT	Simultanous TFT/Panel
640x480	8, 16	60	25,175	9,12,18	Yes	Yes
640x480	8, 16	72	31,5	–	Yes	No
640x480	8, 16	75	31,5	–	Yes	No
800x600	8, 16	60	40	9,12,18	Yes	Yes
800x600	8, 16	72	50	–	Yes	No
800x600	8, 16	75	49,5	–	Yes	No
1024x768	8, 16	60	65	9,12,18	Yes	No
1024x768	8, 16	70	75	–	Yes	No
1024x768	8, 16	75	78,5	–	Yes	No
1280x768	8	60	108	–	Yes	No
1280x768	8	75	135	–	Yes	No

The Panel interface options are described in Section 2.3.

3.3.3 PCI-bus

The PCI-bus on the board is provided by the GX1 CPU and will always run at 33MHz.
The GX1 CPU provides support for up to 3 bus masters. Two of these bus master signals are used by the 5530 and the Realtek 8139C Ethernet controller.
In order to comply with the PC104+ specification additionally 3 sets of bus master signals are generated by means of an arbiter connected to a 3rd set of bus-master signals on the GX1 CPU.
The arbitration algorithm being used provides a fair and equal arbitration for each of the PC104+ bus-masters.
The PCI interface provided in the PC104+ connector complies with the PC/104+ specification version 1.0 February 1997 [2].
The PC104+ specification essentially defines another physical interface to the PCI-bus defined in the PCI v2.1 specification [5].

3.3.4 ISA bus

The 5530 companion chip provides a PCI-ISA bridge, which operate in slave mode. This means that all GX1LCD boards only support ISA slave mode.

ISA master mode allows an ISA board to grant the bus and get the bus master status. The bus master has the ability to generate bus cycles and transferring data without involvement of the CPU or DMA (Direct memory access).
ISA boards that utilise the bus master mode are less common today.

3.3.5 SDRam interface

This board uses SDRAM in the compact SODIMM-144 form factor. 3.3V SDRAM modules must be used.
For CPU / SDRAM Clock settings of 300MHz/ 100MHz PC133 SDRAM must be used. For CPU / SDRAM Clock settings of 300MHz/ 83MHz PC133 SDRAM must be used (see Software Manual).

3.3.6 Panel interface

An alternative display to the standard CRT monitor is a digital flat panel interface in which the color of each pixel is digitally encoded.
The panel data may be transferred in two ways:

- Parallel (available on PANEL connector) where the color of each pixel is transferred over a number of signal lines at rates up to 65MHz.
- Serial where the data is transferred over a few high speed digital lines at up to 650MHz. This interface is provided by the Silicon Image (http://www.siimage.com) SIL140 Panel Link transmitter.

The parallel interface is only suitable for small distances (less than 50 cm) and is typically implemented by means of ribbon cables. The user should consider the EMC design of the box and cabling when this interface is used.
It should also be noted that the signal level of these is 3.3V, but does comply to the TTL signal levels. Some (mostly older) displays require 5V signal level.

The Panel link interface transfers the data in low voltage differential mode through 4 twisted pair lines. This interface reduces EMC problems and allows display distances of up to 10m.
Part of the COM1 interface is also provided in the Panel link connector in order to facilitate easy connection to a mouse, touch screen or other device (GX1LCD/S only).
More and more panels are now seen with Panel Link as their standard interface. If a Panel Link interface is not provided on the panel, a Panel Link receiver may be used to convert the serial data to a format suitable for the screen. For currently available Panel Link receivers please check our Web-site.

The Panel interface options are described in Section 2.3.

3.3.7 Audio

The CS5530A companion chip provides audio support by means of an AC97 codec interface. The audio codec provides mixing of the analog signals as well as Digital/analog conversion.
The following analog interfaces are provided.

- Line-in, stereo.
- CR-ROM input, stereo.
- Microphone, single input with microphone bias circuit.
- Lineout, stereo.
- Speaker out, stereo. 2x0.5W in 4Ω on GX1LCD/S.

Access to the audio signals is provided by a pinrow (JPAUX) on GX1LCD/S or by a dedicated audio bracket.
Access to the audio signals is provided by a pinrow (BRACK1, 2) on GX1LCD/3.5" or by a dedicated audio bracket.

3.3.8 IDE interface

The CS5530S companion chip provides a primary as well as a secondary IDE controller with support of Ultra DMA33 mode and PCI bus mastering for the data transfer.
A standard IDC40 connector and an optional compact flash connector on the backside of the board provide access to these controllers.

3.3.9 USB

The USB interface provides two channels controlled by the CS5530A.
The signals are provided by means of a pinrow or by an USB bracket adapter on GX1LCD/S or by Type A USB Connector on GX1LCD/3.5".
USB Legacy is currently not supported.

3.3.10 Ethernet

The Ethernet interface is based on a Realtek 8139C Ethernet controller supporting 10MBit as well as 100Mbit Base-T interface.
The controller is attached to the PCI bus and uses PCI bus mastering for data transfer. The CPU is thereby not loaded during the actual transfer.

3.3.11 Winbond W83877ATF

This device provides additionally two RS232C COM-ports on GX1LCD/S Plus Boards (Total of 4 COM Ports). Operates in RS232 mode by means of a charge pump driver. Only 5V supply is required.

3.3.12 Winbond W83977AF

This is the main IO controller with the following features:

- COM1. A RS485/RS232 driver is used providing RS232, RS422/RS485. Selection of the mode is made in the BIOS. Driver uses charge pumps requiring only +5V.
- COM2. Operates in RS232 mode by means of a charge pump driver. Only 5V supply is required.
- LPT. Support for SPP, EPP and ECP modes.
- Keyboard interface.
- Mouse interface.
- IrDA interface for infrared communication. Maximum speed 115KBps. This interface shares the controller of COM2.

- NVRam with battery backup for BIOS configuration and real time clock.

Additionally, a number of general-purpose IO pins are used for the feature connector General-purpose IO pins and for various control signals on the board.

3.3.13 M-system Disk on Chip (GX1LCD/S only)

Access to the BIOS and M-system disk on chip socket is controlled by the CPLD on the board. In this way, it is possible to provide an address window for the disk on chip support. Information on DOC2000 devices may be found on http://www.m-sys.com.

The M-systems socket may additionally be used to bootstrap the system if the on-board BIOS should be erased. This requires an external flash BIOS (e.g Atmel 29C040A) inserted with a 3.3KΩ pull-down on the chip select signal (CS Pin 22, GND Pin 16). Contact Support for instructions on bootstrapping.

3.3.14 Supervision

The Board supervision includes Power supplies, Board and CPU Temperature, and Fan rotation. A Watchdog Timer is provided in case of system lockup.

3.3.15 PLD

Some of the features mentioned require additional control and configuration signals not provided by the standard busses.
Examples of the functions of the PLD are:

- Supervision action on temperature, fan, and SW watch-dog alarms.
- CPU speed setting and other configurations eliminating the need for jumpers or dip-switches.

These configurations and features are encapsulated in the BIOS setup to provide an easy-to-use hardware independent interface. Please refer to the Software Manual User Utilities Section for further information.

4. System Resources

4.1 Memory Map

The following table indicates memory map for the **GX1LCD** boards. The address ranges specifies the runtime code length.

Address Range	Length	Description	Note
00000000-000002FFh	768 bytes	BIOS Interrupt Vector Table	
00000300-000003FFh	256 bytes	BIOS Stack Area	
00000400-000004FFh	256 bytes	BIOS Data Area	
00000500-0009FFFFh	639 Kbytes	Application Memory. Used by the operating system, device drivers and TSRs	
000A0000-000BFFFFh	128 Kbytes	Video memory page	1
000C0000-000C7FFFh	32 Kbytes	Video BIOS ROM (CS5530)	1
000C8000-000D7FFFh	48 Kbytes	Occupied by Network Boot Extension if enabled	2
000D8000-000DFFFFh	32 Kbytes	Available for external ROM BIOS Extensions	
000E0000-000E3FFFh	16 Kbytes	Occupied by M-System support on GX1LCD/S Boards if enabled.	3
000E4000-000FFFFFh	112 Kbytes	System BIOS ROM	
00100000-1FFFFFFFh	511 Mbytes	Application Memory. Accessible through EMM-handler or as Extended memory	
FFFF0000-FFFFFFFFh	64 Kbytes	System BIOS ROM (mirrored)	

Note:
1. Used by the on-board VGA controller, if enabled.
2. Pressing Shift-F10 during boot and setting ”Boot order” option enables net Boot ROM.
3. This area must be enabled in order to reprogram the BIOS on GX1LCD/S Boards.

4.2 I/O - Map.

On the GX1LCD board only ISA slave mode is supported.
The drive capabilities allow for up to five external ISA slots to be driven without external data buffers. The accessible I/O area on the ISA-bus is 64Kbytes with 16 address bits and the accessible Memory area is 16Mbytes with 24 address bits.
Certain I/O addresses are subject to change during boot as PnP managers may relocate devices or functions. The addresses shown in the table are typical locations

I/O Port	Access	Read/ Write	Description
0000h – 001Fh are used by the 8237 Compatible DMA Controller 1			
DMA Current Address and Byte Count Registers Ch.3-0			
0000h	PCI	R/W	DMA channel 0 Address bits [15:0] : byte 0 (low byte), followed by byte 1.
0001h	PCI	R/W	DMA channel 0 Byte count [15:0] : byte 0 (low byte), followed by byte 1.
0002h	PCI	R/W	DMA channel 1 Address bits [15:0] : byte 0 (low byte), followed by byte 1.
0003h	PCI	R/W	DMA channel 1 Byte count [15:0] : byte 0 (low byte), followed by byte 1.
0004h	PCI	R/W	DMA channel 2 Address bits [15:0] : byte 0 (low byte), followed by byte 1.
0005h	PCI	R/W	DMA channel 2 Byte count [15:0] : byte 0 (low byte), followed by byte 1.
0006h	PCI	R/W	DMA channel 3 Address bits [15:0] : byte 0 (low byte), followed by byte 1.
0007h	PCI	R/W	DMA channel 3 Byte count [15:0] : byte 0 (low byte), followed by byte 1.
DMA Status and Command Register Ch.3-0			
0008h	PCI	R	DMA channels 3-0 status register Bit 7 1 Channel 3 request Bit 6 1 Channel 2 request Bit 5 1 Channel 1 request Bit 4 1 Channel 0 request Bit 3 1 Terminal count on channel 3 Bit 2 1 Terminal count on channel 2 Bit 1 1 Terminal count on channel 1 Bit 0 1 Terminal count on channel 0
0008h	PCI	W	DMA channels 3-0 command register Bit 7 0 DACK# sense active low 1 DACK# sense active high Bit 6 0 DREQ sense active high 1 DREQ sense active low Bit 5 0 Late write selection 1 Extended write selection Bit 4 0 Fixed priority 1 Rotating priority Bit 3 0 Normal timing 1 Compressed timing Bit 2 0 Enable controller 1 Disable controller Bit 1 0 Reserved. Must be 0. Bit 0 0 Reserved. Must be 0.
DMA Request Register			
0009h	PCI	W	DMA write request register, Channels 3-0 Bits 7-3 0 Reserved. Must be 0. Bit 2 0 Resets individual DMA Channel Service SW Request Bit 1-0 1 Sets the request bit. 00 DMA Channel 0 select 01 DMA Channel 1 select 10 DMA Channel 2 select 11 DMA Channel 3 select

DMA Mask Register			
000Ah	PCI	W	DMA channel 3-0 mask register Bits 7-3 - Reserved. Must be 0. Bit 2 0 Enable DREQ for the selected channel. 1 Disable DREQ for the selected channel. Bit 1-0 Channel select 00 Channel 0 01 Channel 1 10 Channel 2 11 Channel 3
DMA Channel Mode Register			
000Bh	PCI	W	DMA channel 3-0 write mode register Bits 7-6 Transfer Mode select 00 Demand mode 01 Single mode 10 Block mode 11 Cascade mode Bit 5 0 Address increment 1 Address decrement Bit 4 0 Disable auto-initialization 1 Enable auto-initialization Bit 3-2 Select type of operation 00 Verify operation 01 Memory write 10 Memory read 11 Reserved Bits 1-0 Channel select 00 Channel 0 01 Channel 1 10 Channel 2 11 Channel 3
Misc. DMA Registers			
000Ch	PCI	W	DMA 1 Clear byte pointer flip/flop. Channels 3-0. Command enabled with a write to the I/O port address.
000Dh	PCI	W	DMA 1 Master Clear Register. Channels 3-0. Same effect as HW reset. Command enabled with a write to the I/O port address.
000Eh	PCI	W	DMA 1 Clear Mask Register. Channels 3-0. Enables acceptance of DMA requests for all four channels. Command enabled with a write to the I/O port address.
000Fh	PCI	R/W	DMA 1 Mask Register, read/write all mask bits. Channels 3-0. Bits 7-4 0 Reserved. Must be 0. Channel Mask Bits Bit 3 0 Disable ch. 3 DREQ 1 Enable ch. 3 DREQ Bit 2 0 Disable ch. 2 DREQ 1 Enable ch. 2 DREQ Bit 1 0 Disable ch. 1 DREQ 1 Enable ch. 1 DREQ Bit 0 0 Disable ch. 0 DREQ 1 Enable ch. 0 DREQ
0020h – 0021h are used by the 8259 compatible Programmable interrupt controller 1			
Int. 1 Control			
0020h	PCI/ISA	W	Initialization Command Word 1 Register. Set Bit 4 to 1 to access ICW1. Bit 7-5 000 Reserved. Set to 0. Bit 4 1 ICW1 Select. Must be 1 to select ICW1. Bit 3 0 Edge Trigger Mode 1 Level Trigger Mode Bit 2 0 8 byte Vector Address Intervals 1 4 byte Vector Address Intervals Bit 1 0 Cascade Mode. Must be 0. Bit 0 1 ICW4 Write Required. Must be set to 1.

0020h	PCI/ISA	W	Operational Control Word 2 Register. Set Bits 4 and 3 to 00 to access OCW2. Bits 7-5 000 Rotate in automatic EOI mode (clear) 001 Non-specific EOI 010 No Action. 011 Specific EOI (bits [2:0] must be valid) 100 Rotate in automatic EOI mode (set) 101 Rotate on non-specific EOI command 110 Set priority command (bits [2:0] must be valid) 111 Rotate on specific EOI command Bits 4-3 00 OCW2 Select. Must be 00 to select OCW2. Bits 2-1 nnn The interrupt request to which the command applies
0020h	PCI/ISA	W	Operational Control Word 3 Register. Set Bits 4 and 3 to 01 to access OCW3. Bit 7 0 Reserved. Must be 0. Bit 6-5 00 No Action. 01 Normal mask mode. 10 No Action. 11 Enter special mask mode. Bit 4-3 01 Must be programmed to 01 to select OCW3 Bit 2 0 No poll command. 1 Poll command. Next I/O read to irq controller is treated as highest priority request. Bit 1-0 00 No Action. 01 No Action. 10 Read interrupt request register on next read of port 0020h. 11 Read interrupt in-service register on next read of port 0020h.
0020h	PCI/ISA	R	IRQ and IS read to port 0020h following write to OCW3. Interrupt request register: Bits 7-0 0 No active request for the corresponding interrupt line. 1 Active request for the corresponding interrupt line. Interrupt in-service register: Bits 7-0 0 The corresponding interrupt line is not being serviced. 1 The corresponding interrupt line is being serviced.
Int. 1 Mask.			
0021h	PCI/ISA	W	Initialization Command Word 2-4. Following a write to the ICW1 a initialization sequence with three I/O writes to respectively ICW2, ICW3 and ICW4 Initialization Command Word 2: Bits 7-3 nnnnn Address lines A7-A3 of the base vector address for the 000 interrupt controller. Bits 2-0 Interrupt Request Level. Must be programmed to all 0s. Initialization Command Word 3: Bits 7-3 Reserved. Must be 0s. Bit 2 Cascaded Mode Enable Bit 0 Reserved. Must be all 0s. Initialization Comand Word 4: Bits 7-5 000 Reserved (should be zeroes). Bit 4 0 No special fully-nested mode. 1 Special fully-nested mode. Bit 3-2 00 Buffered Mode. Must be programmed to 00 selecting Non-buffered mode. Bit 1 0 Normal EOI. 1 Auto EOI. Bit 0 0 8085 mode. 1 8086 and 8080 mode. (Intel Architecture Based system).
0021h	PCI/ISA	R/W	Operation Command Word 1 (OCW1) Bit 7 0 Enable IRQ7 interrupt Bit 6 0 Enable IRQ6 interrupt Bit 5 0 Enable IRQ5 interrupt Bit 4 0 Enable IRQ4 interrupt Bit 3 0 Enable IRQ3 interrupt Bit 2 0 Enable IRQ2 interrupt Bit 1 0 Enable IRQ1 interrupt Bit 0 0 Enable IRQ0 interrupt
0022h-0023h are used by Geode GX1 Configuration Access Registers.			
0022h 0023h		W R/W	Config Port / Index Port. Data Port.

0040h – 0043h are used by the 82C54 compatible Programmable timer 1			
Timer Counter 1 : Counter 0-2 Count			
0040h	PCI/ISA	R	Programmable interval timer counter 0 status byte format register. This status byte can be read following an Interval Timer Read Back Command. Bit 7 Counter Out Pin State 0 Pin is 0 1 Pin is 1 Bit 6 Count Register Status 0 Count has been transferred from CR to CE and is available for reading. 1 Count has not been transferred from CR to CE and is not yet available for reading. Bits 5-4 Read/Write Selection Status 00 Counter Latch Command 01 R/W Least Significant Byte (LSB) 10 R/W Most Significant Byte (MSB) 11 R/W LSB then MSB. Bits 3-1 Mode Selection Status 000 Mode 0 selected 001 Mode 1 selected x01 Mode 2 selected x11 Mode 3 selected 100 Mode 4 selected 101 Mode 5 selected Bit 0 Countdown Type Status 0 Binary countdown 1 Binary coded decimal (BCD) countdown
0040h	PCI/ISA	W	Counter 0 Access Ports register. Bits 7-0 - Used to program 16-bit Count register. The order of programming LSB and MSB is defined with the Interval Counter Control Register.
0041h	PCI/ISA	R	Programmable timer counter 1 status byte format register. Equivalent to counter 0 byte definition.
0041h	PCI/ISA	R/W	Counter 1 Access Ports register. Equivalent to counter 0 byte definition.
0042h	PCI/ISA	R	Programmable timer counter 2 status byte format register. Equivalent to counter 0 byte definition.
0042h	PCI/ISA	R/W	Counter 2 Access Ports register. Equivalent to counter 0 byte definition.
Timer Counter 1 Command Mode			
0043h	PCI/ISA	W	Programmable timer mode port. Control word register for counters 0, 1 and 2 Bits 7-6 00 Counter 0 select 01 Counter 1 select 10 Counter 2 select 11 Read Back Command Bits 5-4 00 Counter latch command 01 R/W counter bits LSB only 10 R/W counter bits MSB only 11 R/W counter bits LSB first, then bits MSB Bits 3-1 Counter Mode Selection 000 Mode 0 Out signal on end of count. 001 Mode 1 Hardware retriggerable one-shot X10 Mode 2 Rate generator (divide by n counter) X11 Mode 3 Square wave output 100 Mode 4 Software triggered strobe 101 Mode 5 Hardware triggered strobe Bit 0 0 Binary counter is 16 bits (count max. 2^{16}) 1 Binary code decimal (BCD) counter (count max. 2^4)
Read Back Command			
0043h	PCI/ISA	W	Read Back Command for counters 0,1 and 2. Must follow a write to Control word register. The requested count or status may be read by access to the counter's I/O address. Bit 7-6 00 Read Back Command. Bit 5 0 Current count will be latched. 1 Current count will not be latched. Bit 4 0 Status of selected counters will be latched. 1 Status of selected counters will not be latched. Bit 3-1 001 Counter 0 Select. 010 Counter 1 Select. 100 Counter 2 Select. Bit 0 0 Reserved. Must be 0.

Counter Latch Command			
0043h	PCI/ISA	W	Counter Latch Command for counters 0,1 and 2. Must follow a write to Control word register. The requested count or status may be read by access to the counter's I/O address. Bit 7-6 00 Latch counter 0 select. 01 Latch counter 1 select. 10 Latch counter 2 select. 11 Read back command. Bit 5-4 00 Counter Latch Command. Bit 3-0 0 Reserved. Don't care.
0060h & 0064h are used by the 8042 compatible keyboard-controller.			
Keyboard controller data port.			
0060h	PCI/ISA	R	Keyboard input buffer. A read of address 60h resets IRQ1 and IRQ12 (if enabled). Bit 7 0 Keyboard inhibited Bit 6 0 Primary display is VGA 1 Primary display is MDA Bit 5 0 System BIOS performs diagnostics on the motherboard in an Infinite loop. 1 Any other diagnostic function Bit 4 Motherboard RAM 0 256 kB 1 >= 512 kB Bit 3-1 - Reserved Bit 0 0 The motherboard passed the diagnostics tests when diagnostic mode was enabled.
0060h	PCI/ISA	W	Keyboard output port. Bit 7 0 Keyboard data is being transferred Bit 6 0 The keyboard clock signal is being used in data transfer Bit 5 0 PC-type mouse being used 1 PS/2-type mouse being used Bit 4 0 Output buffer full, IRQ1 generated 1 Output buffer not full Bit 3-2 - Reserved Bit 1 0 The system processor address 20 line is inhibited on the system bus 1 Address line 20 in not inhibited Bit 0 0 Reset system processor 1 This bit should always be kept at 1
0061h is used by NMI Status and Control.			
0061h	PCI/ISA	R/W	NMI Status and Control
		R	Bit 7 0 This bit must be 0 when writing to port 61h. 1 This bit is set if PCI device or main memory detects a system board error and pulses the PCI PERR#/SERR# line.
		R	Bit 6 0 This bit must be 0 when writing to port 61h. 1 This bit is set if an expansion board asserts IOCHK# on the ISA Bus.
		R	Bit 5 0 This bit must be 0 when writing to port 61h. 1 This bit reflects the Counter 2 OUT signal state.
		R	Bit 4 0 This bit must be 0 when writing to port 61h. 1 The Refresh Cycle Toggle bit toggles from 0 to 1 or 1 to 0 following every refresh cycle.
		R/W	Bit 3 0 Enable IOCHK# NMIs. 1 Clear and disable IOCHK# NMIs.
		R/W	Bit 2 0 Enable PCI SERR#. 1 Clear and disable PCI SERR#.
		R/W	Bit 1 0 Speaker Output is 0. 1 Speaker Output is the Counter 2 OUT signal value.
		R/W	Bit 0 0 Timer Counter 2 Disable. 1 Timer Counter 2 Enable.

0060h & 0064h are used by the 8042 compatible keyboard-controller.			
0064h	PCI/ISA	R	Keyboard controller status. Bit 7 0 No parity error 1 Parity error on last byte of transmission from keyboard Bit 6 0 No timeout 1 Received a timeout on last transmission Bit 5 0 No timeout 1 Transmission from keyboard controller to keyboard timed out Bit 4 0 Keyboard inhibited 1 Keyboard not inhibited Bit 3 0 Data. System writes to input buffer via I/O port 0060h 1 Command. System writes to input buffer via I/O port 0064h Bit 2 0 System flag status. Set to 0 after a power on reset. 1 The keyboard controller sets this bit according to the command from the system. Bit 1 0 Input buffer (0060h or 0064h) is empty 1 Input buffer full Bit 0 0 Output buffer has no data 1 Output buffer full
0064h	PCI/ISA	W	Keyboard Command Write
0070h - 0071h are used by the RTC clock and CMOS RAM.			
0070h	PCI/ISA	W	Real Time Clock (CMOS RAM) address register and NMI mask Bit 7 0 NMI disabled 1 NMI enabled Bits 6-0 n x 7 CMOS RAM index address register
0071h	PCI/ISA	R/W	CMOS RAM data register port
0080h is used for power-on diagnostics port.			
0080h	PCI/ISA	R	Manufacturing test port (POST checkpoints can be accessed via this port)
0080h	PCI/ISA	R/W	Temporary storage for additional DMA page register
0081h - 008Fh are used for DMA control.			
0081h	PCI/ISA	R/W	DMA channel 2 Address bits [23:16]
0082h	PCI/ISA	R/W	DMA channel 3 Address bits [23:16]
0083h	PCI/ISA	R/W	DMA channel 1 Address bits [23:16]
0084h	PCI/ISA	R/W	Additional DMA page register (Reserved)
0085h	PCI/ISA	R/W	Additional DMA page register (Reserved)
0086h	PCI/ISA	R/W	Additional DMA page register (Reserved)
0087h	PCI/ISA	R/W	DMA channel 0 Address bits [23:16]
0088h	PCI/ISA	R/W	Additional DMA page register (Reserved)
0089h	PCI/ISA	R/W	DMA channel 6 Address bits [23:16]
008Ah	PCI/ISA	R/W	DMA channel 7 Address bits [23:16]
008Bh	PCI/ISA	R/W	DMA channel 5 Address bits [23:16]
008Ch	PCI/ISA	R/W	Additional DMA page register (Reserved)
008Dh	PCI/ISA	R/W	Additional DMA page register (Reserved)
008Eh	PCI/ISA	R/W	Additional DMA page register (Reserved)
008Fh	PCI/ISA	R/W	DMA low page register refresh
0092h is used for the Peripheral controller Fast GateA20 and Keyboard reset.			
0092h	PCI/ISA	R/W	Port 92 Register. Bits 7-2 - Reserved. Bit 1 - Fast gate A20 option 0 CPU address wrap around 1MB boundary 1 No wrap around. Bit 0 1 Force a Fast CPU reset, for protected mode switchings.

00A0h-00A1h are used for Programmable interrupt controller 2.			
Except for the differences noted below, the bit definitions are the same as those for addresses 0020h-0021h.			
Int. 2 Control			
00A0h	PCI/ISA	R/W	Programmable interrupt controller 2
Int. 2 Mask			
00A1h	PCI/ISA	R/W	Programmable interrupt controller 2 mask (OCW1) Bit 7 0 Enable IRQ15 interrupt Bit 6 0 Enable IRQ14 interrupt Bit 5 0 Enable IRQ13 interrupt Bit 4 0 Enable IRQ12 interrupt Bit 3 0 Enable IRQ11 interrupt Bit 2 0 Enable IRQ10 interrupt Bit 1 0 Enable IRQ9 interrupt Bit 0 0 Enable IRQ8 interrupt

00C0h - 00DFh are used by DMA controller 2.			
00C0h	PCI	R/W	DMA channel 4 Address bits [15:0] : byte 0 (low byte), followed by byte 1. Not used.
00C2h	PCI	R/W	DMA channel 4 Byte count [15:0] : byte 0 (low byte), followed by byte 1. Not used.
00C4h	PCI	R/W	DMA channel 5 Address bits [15:0] : byte 0 (low byte), followed by byte 1.
00C6h	PCI	R/W	DMA channel 5 Byte count [15:0] : byte 0 (low byte), followed by byte 1.
00C8h	PCI	R/W	DMA channel 6 Address bits [15:0] : byte 0 (low byte), followed by byte 1.
00CAh	PCI	R/W	DMA channel 6 Byte count [15:0] : byte 0 (low byte), followed by byte 1.
00CCh	PCI	R/W	DMA channel 7 Address bits [15:0] : byte 0 (low byte), followed by byte 1.
00CEh	PCI	R/W	DMA channel 7 Byte count [15:0] : byte 0 (low byte), followed by byte 1.
00D0h	PCI	R	DMA channel 7-4 status register Bit 7 1 Channel 7 request Bit 6 1 Channel 6 request Bit 5 1 Channel 5 request Bit 4 1 Channel 4 request Bit 3 1 Terminal count on channel 7 Bit 2 1 Terminal count on channel 6 Bit 1 1 Terminal count on channel 5 Bit 0 1 Terminal count on channel 4
00D0h	PCI	W	DMA channel 7-4 command register Bit 7 0 DACK# sense active low 1 DACK# sense active high Bit 6 0 DREQ sense active high 1 DREQ sense active low Bit 5 0 Late write selection 1 Extended write selection Bit 4 0 Fixed priority 1 Rotating priority Bit 3 0 Normal timing 1 Compressed timing Bit 2 0 Enable controller 1 Disable controller Bit 1 0 Reserved. Must be 0. Bit 0 0 Reserved. Must be 0.
00D2h	PCI	W	DMA channel 7-4 write request register Bit 7-3 0 Reserved (should all be zeroes) Bit 2 0 Resets individual DMA Channel Service SW Request 1 Sets the request bit. 00 Illegal 01 DMA Channel 5 select 10 DMA Channel 6 select 11 DMA Channel 7 select
00D4h	PCI	R/W	DMA channel 7-4 write single mask register bit Bits 7-3 0 Reserved (should all be zeroes) Bit 2 0 Clear mask bit 1 Set mask bit Bit 1-0 Channel select 00 Channel 4 01 Channel 5 10 Channel 6 11 Channel 7

00D6h	PCI	W	DMA channel 7-4 mode register Bits 7-6 Mode select 00 Demand mode 01 Single mode 10 Block mode 11 Cascade mode Bit 5 0 Address increment 1 Address decrement Bit 4 0 Disable autoinitialization 1 Enable autoinitialization Bit 3-2 Select type of operation 00 Verify operation 01 Memory write 10 Memory read 11 Reserved Bits 1-0 Channel select 00 Channel 4 01 Channel 5 10 Channel 6 11 Channel 7
00D8h	PCI	W	DMA channel 7-4 clear byte pointer flip/flop
00DAh	PCI	W	DMA channel 7-4 master clear
00DCh	PCI	W	DMA channel 7-4 clear mask register
00DEh	PCI	W	DMA channel 7-4 write mask register
00F0h – 00FFh INSIDE Technology On-board control registers.			
00F0h	PCI/ISA	-	
00F1h	PCI/ISA	-	
00F2h	PCI/ISA	R	Revision Information Register Bit 7-4 - PCB Revision Bit 3-0 - CPLD Revision
00F3h	PCI/ISA	R/W	GPIO Configuration Bit 0 - Read / Set Direction of GPIO3-0. Input (“0”), Output (“1”). Bit 1 - Read / Set Direction of GPIO7-4. Input (“0”), Output (“1”).
00F4h	PCI/ISA	R/W	GPIO Data
00F5h-00F9h	PCI/ISA	-	Reserved for Inside Technology use.
00FAh	PCI/ISA	R/W	Software Watchdog Control Bit 7-0 - Counter Value; Load counter with 00h to disable Watchdog. Value gives Watchdog countdown in half minutes 0-127 minutes (0-255).
00FBh-00FFh	PCI/ISA	-	Reserved for Inside Technology use.
0100h - 03FFh On-board peripherals and PC-AT / PC104 Adapter boards.			
0170h - 0177h may be used by on-board hard disk controller for secondary (1) IDE port. Depends on choice made in Main setup. The bit definitions for these addresses are the same as those for addresses 01F0h-01F7h.			
0170h	PCI/ISA	R/W	Hard disk 1 data register base port
0171h	PCI/ISA	R	Hard disk 1 error register
0171h	PCI/ISA	W	Hard disk 1 write pre-compensations register
0172h	PCI/ISA	R/W	Hard disk 1 sector count
0173h	PCI/ISA	R/W	Hard disk 1 sector number
0174h	PCI/ISA	R/W	Hard disk 1 number of cylinders, low byte
0175h	PCI/ISA	R/W	Hard disk 1 number of cylinders, high byte
0176h	PCI/ISA	R/W	Hard disk 1 drive/head register
0177h	PCI/ISA	R	Hard disk 1 status register
0177h	PCI/ISA	W	Hard disk drive 1 command register

01F0h - 01F7h may be used by on-board hard disk controller for primary (1) IDE port. Depends on choice made in Main setup.			
01F0h	PCI/ISA	R/W	Hard disk 0 data register base port
01F1h	PCI/ISA	R	Hard disk 0 error register **Diagnostic mode** Bits 7-3 - Reserved Bits 2-0 - Diagnostics mode errors 001 No errors 010 Controller error 011 Sector buffer error 100 ECC device error 101 Control processor error **Operation mode** Bit 7 0 Block is not bad 1 Bad block detected Bit 6 0 No error 1 Uncorrectable ECC error Bit 5 - Reserved Bit 4 0 ID not found 1 ID found Bit 3 - Reserved Bit 2 0 Command aborted 1 Command completed Bit 1 0 Track 000 found 1 Track 000 not found Bit 0 0 DAM found (CP-3002 is always 0) 1 DAM not found
01F1h	PCI/ISA	W	Hard disk 0 write pre-compensations register
01F2h	PCI/ISA	R/W	Hard disk 0 sector count
01F3h	PCI/ISA	R/W	Hard disk 0 sector number
01F4h	PCI/ISA	R/W	Hard disk 0 number of cylinders, low byte
01F5h	PCI/ISA	R/W	Hard disk 0 number of cylinders, high byte
01F6h	PCI/ISA	R/W	Hard disk 0 drive/head register Bit 7 1 Reserved Bit 6 0 Reserved Bit 5 1 Reserved Bit 4 - Drive select 0 First hard disk drive 1 Second hard disk drive Bit 3-0 nnnn Head select bits
01F7h	PCI/ISA	R	Hard disk 0 status register Bit 7 1 Controller is executing a command Bit 6 1 Drive is ready Bit 5 1 Write fault Bit 4 1 Seek complete Bit 3 1 Sector buffer requires servicing Bit 2 1 Disk data read corrected Bit 1 1 An index. Set to 1 each disk revolution Bit 0 1 Previous command ended with an error
01F7h	PCI/ISA	W	Hard disk drive 0 command register

0220h - 022Fh may be used by on-board VSA Audio Support (SB16 Compatible) Depends on choice made in Advanced setup			
0220h	PCI/ISA	R	Left FM Status port
0220h	PCI/ISA	W	Left FM Register Status port
0221h	PCI/ISA	W	Left FM Data port
0222h	PCI/ISA	R	Right FM Status port
0222h	PCI/ISA	W	Right FM Register status port
0223h	PCI/ISA	W	Right FM Status port

0224h	PCI/ISA	W	Mixer Register Address Register Data 00h Bit 7-0 Data reset 02h Bit 7-0 Reserved 04h Bit 7-4 Voice Volume Left Bit 3-0 Voice Volume Right 06h Bit 7-0 Reserved 08h Bit 7-0 Reserved 0Ah Bit 2-0 Microphone Mixing 0Ch Bit 2-1 Input Select 0Eh Bit 1 VSTC
			20h Bit 7-0 Reserved 22h Bit 7-4 Master Volume Left Bit 3-0 Master Volume Right 24h Bit 7-0 Reserved 26h Bit 7-4 FM Volume Left Bit 3-0 FM Volume Right 28h Bit 7-4 CD Volume Left Bit 3-0 CD Volume Right 2Ah Bit 7-0 Reserved 2Ch Bit 7-0 Reserved 2Eh Bit 7-4 Line Volume Left Bit 3-0 Line Volume Right
0225h	PCI/ISA	R/W	Mixer Data port
0226h	PCI/ISA	W	Reset
0228h	PCI/ISA	R	FM Status port
0229h	PCI/ISA	W	FM Data port
022Ah	PCI/ISA	R	Read Data port
022Ch	PCI/ISA	W	Command/Write Data
022Ch	PCI/ISA	R	Write Buffer Status (bit 7)
022Eh	PCI/ISA	R	Data Available Status (bit 7)
0240h – 024Fh may be used by on-board VSA Audio Support (SB16 Compatible) Depends on choice made in Advanced setup			
0240h-024Fh	PCI/ISA	-	The bit definitions for these addresses are the same as those for addresses 0220h-022Fh.
0260h – 026Fh may be used by on-board VSA Audio Support (SB16 Compatible) Depends on choice made in Advanced setup			
0260h-026Fh	PCI/ISA	-	The bit definitions for these addresses are the same as those for addresses 0220h-022Fh.
0278h – 027Fh may be used by on-board peripheral controller as Parallel port 2. Depends on choice made in Advanced setup. The bit definitions for these addresses are the same as those for addresses 0378h-037Fh.			
0278h	PCI/ISA	R/W	Parallel port 2, data
0279h	PCI/ISA	R/W	Parallel port 2, status
027Ah	PCI/ISA	R/W	Parallel port 2, control
027Bh	PCI/ISA	R/W	Parallel port 2, EPP address port
027Ch	PCI/ISA	R/W	Parallel port 2, EPP data port 0
027Dh	PCI/ISA	R/W	Parallel port 2, EPP data port 1
027Eh	PCI/ISA	R/W	Parallel port 2, EPP data port 2
027Fh	PCI/ISA	R/W	Parallel port 2, EPP data port 3
0280h - 028Fh may be used by on-board VSA Audio Support (SB16 Compatible) Depends on choice made in Advanced setup			
0280h-028Fh	PCI/ISA	-	The bit definitions for these addresses are the same as those for addresses 0220h-022Fh.
02E8h – 02EFh may be used by on-board peripheral controller as Serial port 4. Depends on choice made in Advanced setup. The bit definitions for these addresses are the same as those for addresses 03F8h-03FFh.			
02E8h	PCI/ISA	R	Receiver buffer register, when DLAB is 0
02E8h	PCI/ISA	W	Transmitter buffer register, when DLAB is 0
02E8h	PCI/ISA	R/W	Divisor latch LSB, when DLAB is 1
02E9h	PCI/ISA	R/W	Divisor latch MSB, when DLAB is 1
02E9h	PCI/ISA	R/W	Interrupt enable register, when DLAB is 0
02EAh	PCI/ISA	R	Interrupt identification register
02EAh	PCI/ISA	W	FIFO control register
02EBh	PCI/ISA	R/W	Line control register

02ECh	PCI/ISA	R/W	Modem control register
02EDh	PCI/ISA	R/W	Line status register
02EEh	PCI/ISA	R/W	Modem status register
02EFh	PCI/ISA	R/W	Scratch pad register

02F8h - 02FFh may be used by on-board peripheral controller as Serial port 2.

Depends on choice made in Advanced setup.
The bit definitions for these addresses are the same as those for addresses 03F8h-03FFh.

02F8h	PCI/ISA	R	Receiver buffer register, when DLAB is 0
02F8h	PCI/ISA	W	Transmitter buffer register, when DLAB is 0
02F8h	PCI/ISA	R/W	Divisor latch LSB, when DLAB is 1
02F9h	PCI/ISA	R/W	Divisor latch MSB, when DLAB is 1
02F9h	PCI/ISA	R/W	Interrupt enable register, when DLAB is 0
02FAh	PCI/ISA	R	Interrupt identification register
02FAh	PCI/ISA	W	FIFO control register
02FBh	PCI/ISA	R/W	Line control register
02FCh	PCI/ISA	R/W	Modem control register
02FDh	PCI/ISA	R/W	Line status register
02FEh	PCI/ISA	R/W	Modem status register
02FFh	PCI/ISA	R/W	Scratch pad register

0370h - 0377h may be used by on-board peripheral controller as Floppy disk controller port 2.

Depends on choice made in Advanced setup.
The bit definitions for these addresses are the same as those for addresses 03F0h-03F7h.

0370h	PCI/ISA	R	Status Register A (SRA)
0371h	PCI/ISA	R	Status Register B (SRB)
0372h	PCI/ISA	R/W	Floppy disk controller output register (DOR)
0373h	PCI/ISA	R/W	Tape Drive Register (TSR)
0374h	PCI/ISA	R	Floppy disk controller status register (MSR)
0374h	PCI/ISA	W	Data Rate Select Register (DSR)
0375h	PCI/ISA	R/W	Floppy disk controller data register (FIFO)
0376h	PCI/ISA	-	Reserved
0377h	PCI/ISA	R	Digital input register (DIR)
0377h	PCI/ISA	W	Hard disk status register (CCR)

0374 – 0377h may be used by on-board IDE controller as Secondary IDE Control Block.

0374h	PCI/ISA	-	Reserved.
0375h	PCI/ISA	-	Reserved.
0376h	PCI/ISA	R/W	Alt. Status/ Device control.
0377h	PCI/ISA	R/W	Forward to ISA (floppy).

0378h - 037Fh may be used by on-board peripheral controller as Parallel port 1.

Depends on choice made in Advanced setup.

0378h	PCI/ISA	R/W	Parallel port 1, data
0379h	PCI/ISA	R	Parallel port 1, status Bit 7 0 Busy Bit 6 0 Acknowledge Bit 5 1 Out of paper Bit 4 1 Printer is selected Bit 3 0 Error Bits 2-1 11 Reserved Bit 0 1 EPP timeout
037Ah	PCI/ISA	R/W	Parallel port 1, control Bits 7-6 00 Reserved Bit 5 0 Data port direction, output data to printer 1 Data port direction, input data from printer Bit 4 1 Enable IRQ Bit 3 1 Select printer Bit 2 0 Initialize printer Bit 1 1 Automatic line feed Bit 0 1 Strobe
037Bh	PCI/ISA	R/W	Parallel port 1, EPP address port
037Ch	PCI/ISA	R/W	Parallel port 1, EPP data port 0
037Dh	PCI/ISA	R/W	Parallel port 1, EPP data port 1
037Eh	PCI/ISA	R/W	Parallel port 1, EPP data port 2
037Fh	PCI/ISA	R/W	Parallel port 1, EPP data port 3

03B0h – 03BBh may be used by on-board Video controller.			
03B0h - 03BFh are used by on-board Video controller in monochrome modes.			
03B0h-03B3h		R/W	Reserved for MDA/Hercules
03B4h		R/W	MDA CRTC index register
03B5h		R/W	MDA CRTC data register
03B6h-03B7h		R/W	Reserved for MDA/Hercules
03B8h		R/W	Hercules mode register
03BAh		R	Status register
03BAh		W	Feature control register
03BCh – 03BFh may be used for off-board Parallel port 3. The bit definitions for these addresses are the same as those for addresses 0378h-037Fh.			
03BC-03BFh		R/W	Available for off-board parallel port 3.
03C0h - 03CFh are used by on-board Video controller in color and monochrome modes.			
03C0h		R/W	Attribute controller Index / Data
03C1h		R/W	Attribute/ Alternate controller Data
03C2h		R	Input Status Register
03C2h		W	Miscellaneous Output Register
03C3h		R/W	Video Subsystem enable
03C4h		R/W	Sequencer index
03C5h		R/W	Sequencer data
03C6h		R/W	Color palette mask
03C7h		R	Color palette state
03C7h		W	Color palette read mode index
03C8h		R/W	Color palette write mode index
03C9h		R/W	Color palette data
03CAh		R	Feature Control register
03CCh		R	Miscellaneous output register
03CEh		R/W	Graphics controller index
03CFh		R/W	Graphics controller data
03D0h - 03D3h are used by Flat Panel and Multimedia Extension			
03D0h		R/W	Flat Panel Extensions Index
03D1h		R/W	Flat Panel Extensions Data
03D2h		R/W	Multimedia Extensions Index
03D3h		R/W	Multimedia Extensions Data
03D4h - 03DFh are used by on-board Video controller in color modes.			
03D4h		R/W	CRTC Index
03D5h		R/W	CRTC Data
03D6h		R/W	Extension index
03D7h		R/W	Extension data
03D8h		R/W	CGA mode register
03D9h		R/W	CGA color register
03DAh		R	Status register
03DAh		W	Feature control register
03DBh		W	Clear light pen FF (ignored)
03DCh		W	Set light pen FF (ignored)
03E8h - 03EFh may be used by on-board peripheral controller as Serial port 3. Depends on choice made in Advanced setup. The bit definitions for these addresses are the same as those for addresses 03F8h-03FFh.			
03E8h	PCI/ISA	R	Receiver buffer register, when DLAB is 0
03E8h	PCI/ISA	W	Transmitter buffer register, when DLAB is 0
03E8h	PCI/ISA	R/W	Divisor latch LSB, when DLAB is 1
03E9h	PCI/ISA	R/W	Divisor latch MSB, when DLAB is 1
03E9h	PCI/ISA	R/W	Interrupt enable register, when DLAB is 0
03EAh	PCI/ISA	R	Interrupt identification register
03EAh	PCI/ISA	W	FIFO control register
03EBh	PCI/ISA	R/W	Line control register
03ECh	PCI/ISA	R/W	Modem control register
03EDh	PCI/ISA	R/W	Line status register
03EEh	PCI/ISA	R/W	Modem status register
03EFh	PCI/ISA	R/W	Scratch pad register

03F0h - 03F7h may be used by on-board peripheral controller as Floppy disk controller port 1. Depends on choice made in Advanced setup.			
03F0h	PCI/ISA	R	Status Register A (SRA)
03F1h	PCI/ISA	R	Status Register B (SRB)
03F2h	PCI/ISA	R/W	Floppy disk controller output register Bits 7-6 00 Reserved (should be zeroes) Bit 5 1 Enable motor on floppy drive B Bit 4 1 Enable motor on floppy drive A Bit 3 1 Enable Interrupt and DMA for floppy drives Bit 2 0 Controller reset Bit 1 0 Reserved (should be zero) Bit 0 0 Select floppy drive A 1 Select floppy drive B
03F4h	PCI/ISA	R	Floppy disk controller status register Bit 7 1 Data register is ready Bit 6 0 Transfer from system to controller 1 Transfer from controller to system Bit 5 1 Non-DMA mode Bit 4 1 Floppy disk controller busy Bits 3-2 xx Reserved Bit 1 1 Drive B is busy Bit 0 1 Drive A is busy
03F5h	PCI/ISA	R/W	Floppy disk controller data register (FIFO)
03F7h	PCI/ISA	R	Digital input register Bit 7 n Diskette change line inverted Bits 6-0 nx7 These bits may be driven by the hard disk status register depending on configuration
03F4h – 03F7h may be used by on-board IDE controller as Primary IDE Control Block.			
03F4h	PCI/ISA	-	Reserved.
03F5h	PCI/ISA	-	Reserved.
03F6h	PCI/ISA	R/W	Alt Status / Device control.
03F7h	PCI/ISA	R/W	Forward to ISA (Floppy).
03F8h - 03FFh may be used by on-board peripheral controller as Serial port 1. Depends on choice made in Advanced setup.			
03F8h	PCI/ISA	R	Receiver buffer register (contains the received character). Bit 0, the least significant bit, is received first. Only this register function when DLAB is 0
03F8h	PCI/ISA	W	Transmitter buffer register (contains the character to be sent). Bit 0, the least significant bit, is send first. Only this register function when DLAB is 0
03F8h	PCI/ISA	R/W	Divisor latch LSB, when DLAB is 1. Settings shown below
03F9h	PCI/ISA	R/W	Divisor latch MSB, when DLAB is 1. Settings shown below

Desired Baud rate	Divisor Used	Divisor latch MSB	Divisor latch LSB
50	2304	9	0
75	1536	6	0
110	1047	4	23
150	768	3	0
300	384	1	128
600	192	0	192
1200	96	0	96
2400	48	0	48
4800	24	0	24
9600	12	0	12
19200	6	0	6
38400	3	0	3
56000	2	0	2
115200	1	0	1

03F9h	PCI/ISA	R/W	Interrupt enable register, when DLAB is 0 Bits 7-4 xxxx Reserved Bit 3 1 Modem status interrupt enable Bit 2 1 Receiver line status interrupt enable Bit 1 1 Transmitter holding register empty interrupt enable Bit 0 1 Received data available interrupt enable

03FAh	PCI/ISA	R	Interrupt identification register, information about a pending interrupt is stored here. When the ID register is addressed, the highest priority interrupt is held and no other interrupts are acknowledged until the microprocessor services that interrupt Bits 7-4 xxxx Reserved Bit 3-0 0xx1 No interrupts 0110 Receiver line status (highest priority) 0100 Received data available 1100 Character timeout indication (FIFO mode only) 0010 Transmitter holding register empty 0000 Modem status (lowest priority)
03FAh	PCI/ISA	W	FIFO control register Bits 7-6 - Receive FIFO interrupt trigger level 00 1 byte 01 4 bytes 10 8 bytes 11 14 bytes Bits 5-3 xxx Reserved Bit 2 1 Clears the transmit FIFO, self-clearing bit Bit 1 1 Clears the receive FIFO, self-clearing bit Bit 0 1 Enable transmit and receive FIFOs
03FBh	PCI/ISA	R/W	Line control register Bit 7 - Divisor Latch Access Bit (DLAB) 0 Access receiver buffer, transmitter holding register 1 Access divisor latches Bit 6 1 Set break control. Serial output forced to spacing state and remains there Bit 5 1 Odd parity Bit 4 1 Even parity select Bit 3 1 Parity enable Bit 2 - Number of stop bits per character 0 One stop bit 1 1½ stop bits if 5-bit word length is selected, 2 stop bits if 6,7 or 8-bit word length is selected Bit 1-0 - Number of bits per character 00 5-bit word length 01 6-bit word length 10 7-bit word length 11 8-bit word length
03FCh	PCI/ISA	R/W	Modem control register Bits 7-5 xxx Reserved Bit 4 1 Loop mode enabled. The output from the transmitter shift register is looped back to the receiver shift register input Bit 3 1 Enable PC-AT interrupt (OUT2) Bit 2 1 Force OUT1 active, no function at this bit Bit 1 1 Force Request To Send active Bit 0 1 Force Data Terminal Ready active
03FDh	PCI/ISA	R/W	Line status register Bit 7 1 In FIFO mode, this bit indicates at least one receive error in the FIFO. It is cleared when the CPU reads LSR, if the are no more errors in the FIFO Bit 6 1 Transmitter shift and holding registers empty Bit 5 1 Transmitter holding register empty. The controller is ready to accept a new character Bit 4 1 Break interrupt. The last received character was a break character Bit 3 1 Framing error. The stop bit that follows the last parity or data bit is zero. Bit 2 1 Parity error. The character has incorrect parity Bit 1 1 Overrun error. A character was sent to the receiver buffer before the previous character was read by the CPU Bit 0 1 Data Ready. A complete incoming character has been received and sent to the receiver buffer register
03FEh	PCI/ISA	R/W	Modem status register Bit 7 1 Data Carrier Detect Bit 6 1 Ring Indicator Bit 5 1 Data Set Ready Bit 4 1 Clear To Send Bit 3 1 Delta Data Carrier Detect Bit 2 1 Trailing edge Ring Indicator Bit 1 1 Delta Data Set Ready Bit 0 1 Delta Clear To Send
03FFh	PCI/ISA	R/W	Scratch pad register

0481h-048Bh are used by DMA High Page Registers			
0481h	PCI/ISA	R/W	DMA Channel 2 Address bits [31:24], register cleared on any access to Port 081h
0482h	PCI/ISA	R/W	DMA Channel 3 Address bits [31:24], register cleared on any access to Port 082h
0483h	PCI/ISA	R/W	DMA Channel 1 Address bits [31:24], register cleared on any access to Port 083h
0487h	PCI/ISA	R/W	DMA Channel 0 Address bits [31:24], register cleared on any access to Port 087h
0489h	PCI/ISA	R/W	DMA Channel 6 Address bits [31:24], register cleared on any access to Port 089h
048Ah	PCI/ISA	R/W	DMA Channel 7 Address bits [31:24], register cleared on any access to Port 08Ah
048Bh	PCI/ISA	R/W	DMA Channel 5 Address bits [31:24], register cleared on any access to Port 08Bh
04D0h-04D1h are used by onboard Interrupt Controller			
04D0h	PCI/ISA	R/W	Interrupt Cntrl 1 (IRQ7-3) Edge/level control. Bit 7 0 IRQ7 Edge Sensitivity. If ICW1 – bit 3 is set as level, it overrides this setting. 1 IRQ7 Level sensitivity. Bit 6 0 IRQ6 Edge Sensitivity. If ICW1 – bit 3 is set as level, it overrides this setting. 1 IRQ6 Level sensitivity. Bit 5 0 IRQ5 Edge Sensitivity. If ICW1 – bit 3 is set as level, it overrides this setting. 1 IRQ5 Level sensitivity. Bit 4 0 IRQ4 Edge Sensitivity. If ICW1 – bit 3 is set as level, it overrides this setting. 1 IRQ4 Level sensitivity. Bit 3 0 IRQ3 Edge Sensitivity. If ICW1 – bit 3 is set as level, it overrides this setting. 1 IRQ3 Level sensitivity. Bit 2-0 000 Reserved. Set to 0.
04D1h	PCI/ISA	R/W	Interrupt Cntrl 2 (IRQ15-9) Edge/level control. Bit 7 0 IRQ15 Edge Sensitivity. If ICW1 – bit 3 is set as level, it overrides this setting. 1 IRQ15 Level sensitivity. Bit 6 0 IRQ14 Edge Sensitivity. If ICW1 – bit 3 is set as level, it overrides this setting. 1 IRQ14 Level sensitivity. Bit 5 0 Reserved. Set to 0. Bit 4 0 IRQ12 Edge Sensitivity. If ICW1 – bit 3 is set as level, it overrides this setting. 1 IRQ12 Level sensitivity. Bit 3 0 IRQ11 Edge Sensitivity. If ICW1 – bit 3 is set as level, it overrides this setting. 1 IRQ11 Level sensitivity. Bit 2 0 IRQ10 Edge Sensitivity. If ICW1 – bit 3 is set as level, it overrides this setting. 1 IRQ10 Level sensitivity. Bit 1 0 IRQ9 Edge Sensitivity. If ICW1 – bit 3 is set as level, it overrides this setting. 1 IRQ9 Level sensitivity. Bit 0 0 Reserved. Set to 0.

4.3 Interrupt Usage.

The CS5530A controller provides an ISA compatible interrupt controller with functionality as two 82C59 interrupt controllers. The two controllers are cascaded to provide 13 external interrupts. Onboard devices use most of these, but a few are available through the PC-AT interface or as INTA-D on the PC104+ connector.
The actual interrupt settings depend on the PnP handler; the scheme below indicates the typical settings.

Interrupt	Onboard system parity errors and IOCHCHK signal activation	Onboard Timer 0 Interrupt	Onboard Keyboard Interrupt	Used for Cascading IRQ8-IRQ15	May be used by onboard Serial Port 1	May be used by onboard Serial Port 2 / IrDA Port	May be used by onboard Serial Port 3 (GX1LCD/S only)	May be used by onboard Serial Port 4 (GX1LCD/S only)	May be used by onboard Parallel Port	May be used by onboard Floppy disk Controller	Used by onboard Real Time Clock Alarm	May be used by onboard P/S 2 support	Used for Onboard co-processor support	May be used by primary harddisk controller	May be used by secondary harddisk controller	May be used by onboard USB controller	May be used by onboard Ethernet controller	Available in PC-AT Bus or on PC104+ connector (PCI-bus) as IRQA-IRQD depending on selections in the BIOS	Notes
NMI	•																		
IRQ0		•																	
IRQ1			•																
IRQ2				•															
IRQ3					•	•	•	•										•	1, 2
IRQ4					•	•												•	1, 2
IRQ5							•	•	•									•	1, 2
IRQ6										•								•	1, 2
IRQ7									•									•	1, 2
IRQ8											•								
IRQ9							•									•	•	•	1, 2
IRQ10								•								•	•	•	1, 2
IRQ11								•								•	•	•	1, 2
IRQ12												•						•	1
IRQ13													•						
IRQ14														•				•	1
IRQ15															•			•	1

Notes:

1. Availability of the shaded IRQs depends on the setting in the BIOS. According to the PCI Standard, PCI Interrupts IRQA-IRQD can be shared.
2. These interrupt lines are managed by the PnP handler and are subject to change during system initialisation.

4.4 DMA-channel Usage.

The DMA circuitry incorporates the functionality of two 82C37 DMA controllers with seven programmable channels. The controllers are referenced DMA Controller 1 for channels 0-3 and DMA Controller 2 for channels 4-7. Channel 4 is by default used to cascade the two controllers. Channels 0-3 are hardwired to 8-bit count-by-bytes transfers and channels 5-7 to 16-bit count-by-bytes transfers.
The onboard Cx5530 provides 32-bit address range support with the 16 least significant bits [15:0] in the Current register, bits [23:16] in the Low Page register, and bits [31:24] in the High Page register.

DMA- Channel	May be used by onboard Floppy disk controller	May be used by onboard Parallel Port in ECP mode	Used for cascading	May be used for onboard VSA Sound System in 8bit DMA mode	May be used for onboard VSA Sound System in 16bit DMA mode	Available in PC-AT Bus depending on selections in the BIOS	Notes
DRQ0				•		•	1
DRQ1		•		•		•	1
DRQ2	•					•	1
DRQ3		•		•		•	1
DRQ4			•				
DRQ5					•	•	1
DRQ6					•	•	1
DRQ7					•	•	1

Notes:

1. The availability of the shaded DMA-channels depends on the choices made in the BIOS Advanced setup screen. The DMA-channels are fully usable in PC-AT bus if the corresponding on-board unit is disabled in the setup screen.

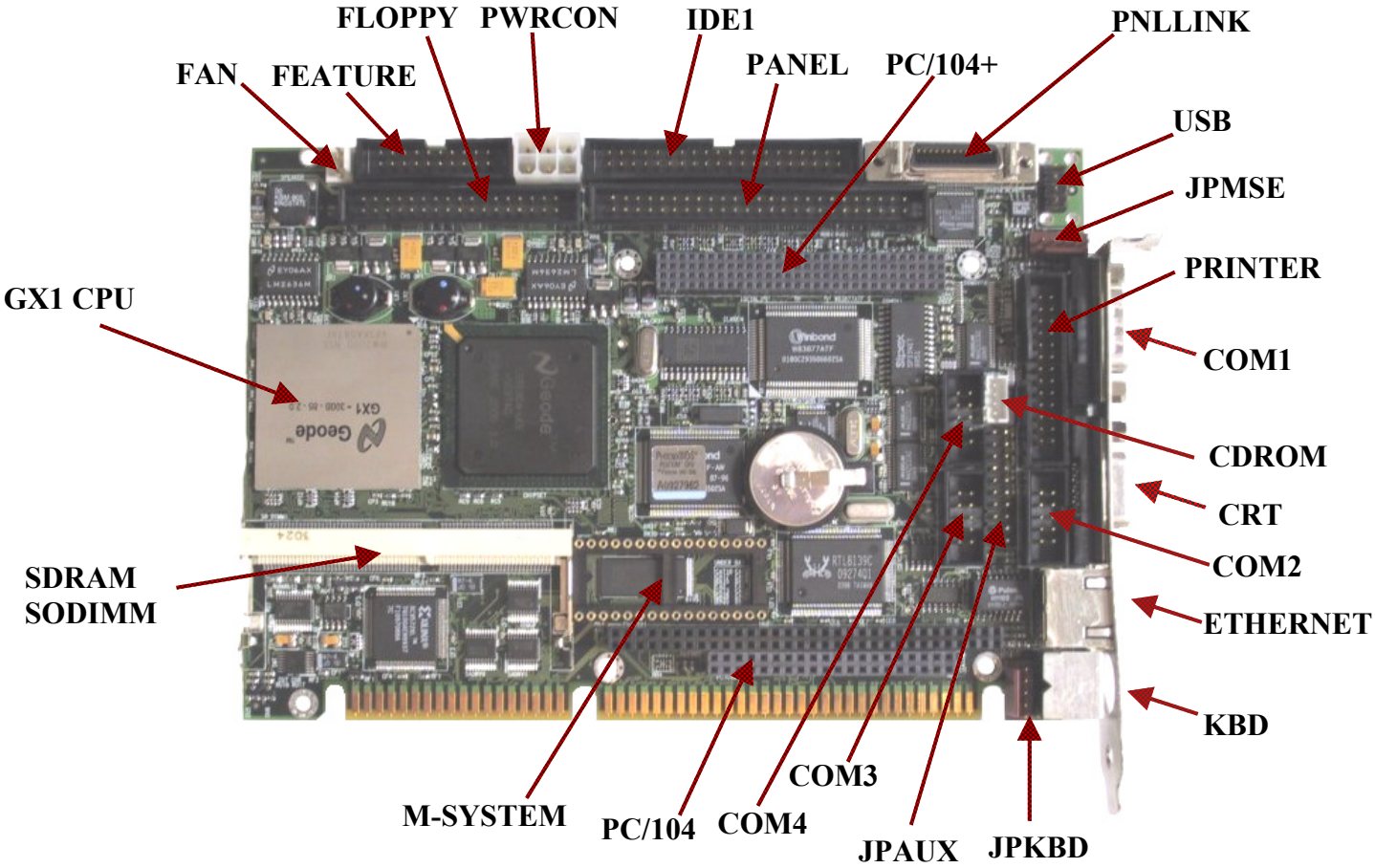
5. Connector Definitions

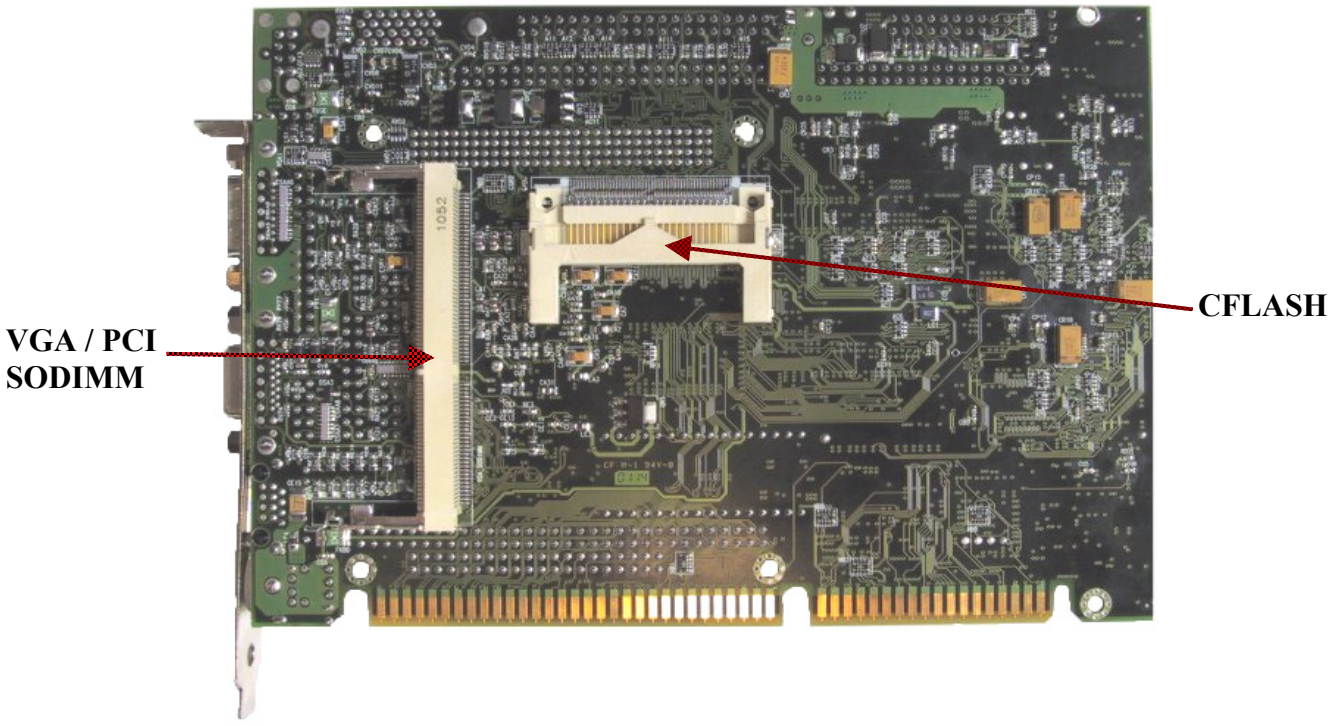
The following sections provide pin definitions and detailed description of all on-board connectors. For a list of internal, mating connectors refer to Mating Connector List.
The connector definitions follow the following notation:

Column name	Description
Pin	Shows the pin-numbers in the connector. The graphical layout of the connector definition tables is made similar to the physical connectors.
Signal	The mnemonic name of the signal at the current pin. The notation "XX#" states that the signal "XX" is active low.
Type	AO : Analog Output. I : Input, TTL compatible if nothing else stated. IO : Input / Output. TTL compatible if nothing else stated. IOT : Bi-directional tristate IO pin. IS : Schmitt-trigger input, TTL compatible. IOC : Input / open-collector Output, TTL compatible. NC : Pin not connected. O : Output, TTL compatible. OC : Output, open-collector or open-drain, TTL compatible. OT : Output with tri-state capability, TTL compatible. PWR : Power supply or ground reference pins.
Ioh/Iol	Ioh: Typical current in mA flowing out of an output pin through a grounded load, while the output voltage is > 2.4 V DC (if nothing else stated). Iol: Typical current in mA flowing into an output pin from a VCC connected load, while the output voltage is < 0.4 V DC (if nothing else stated).
Pull U/D	On-board pull-up or pull-down resistors on input pins or open-collector output pins.
Note	Special remarks concerning the signal.

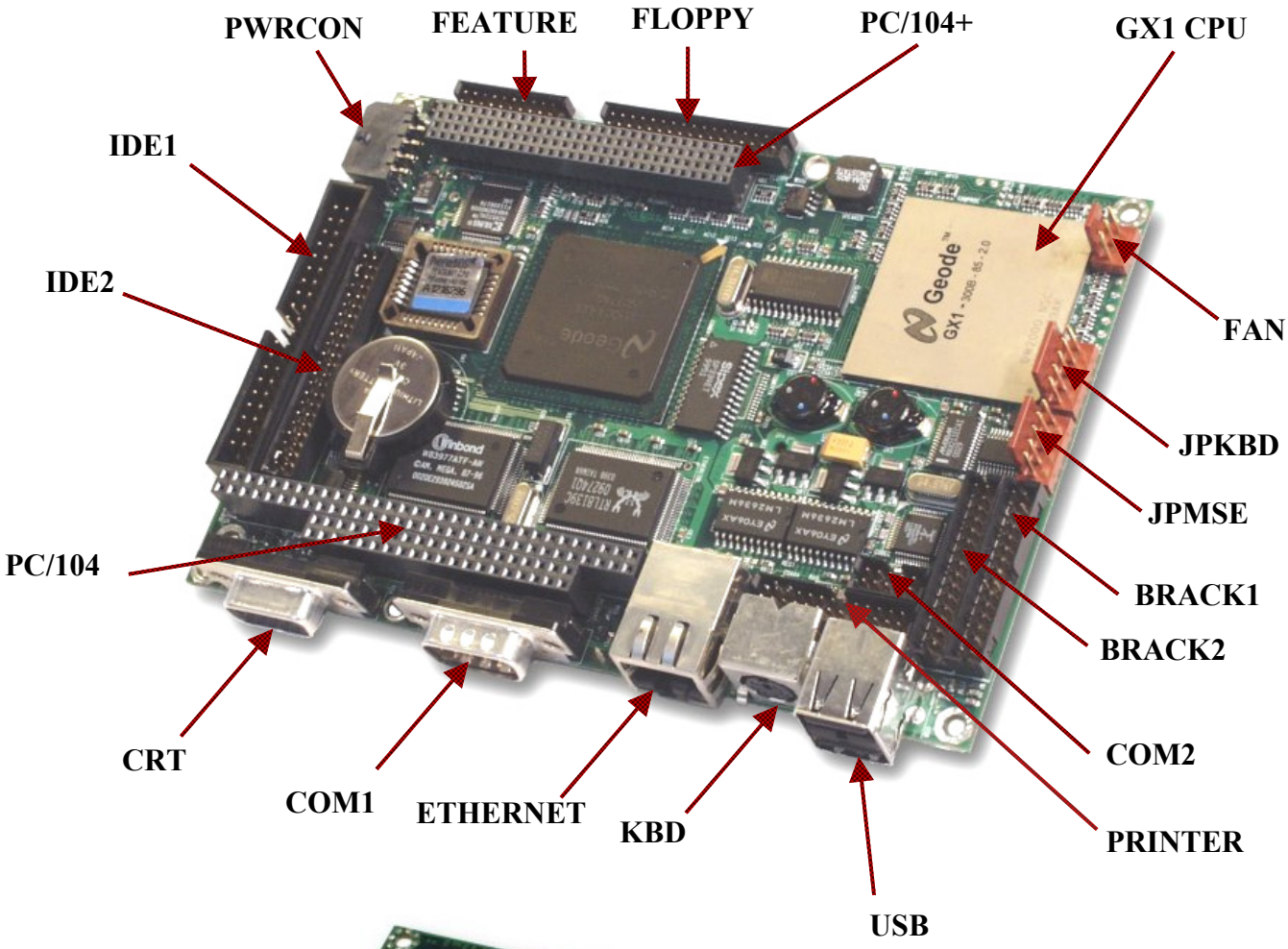
The abbreviation *TBD* is used for specifications which are not available yet or which are not sufficiently specified by the component vendors.

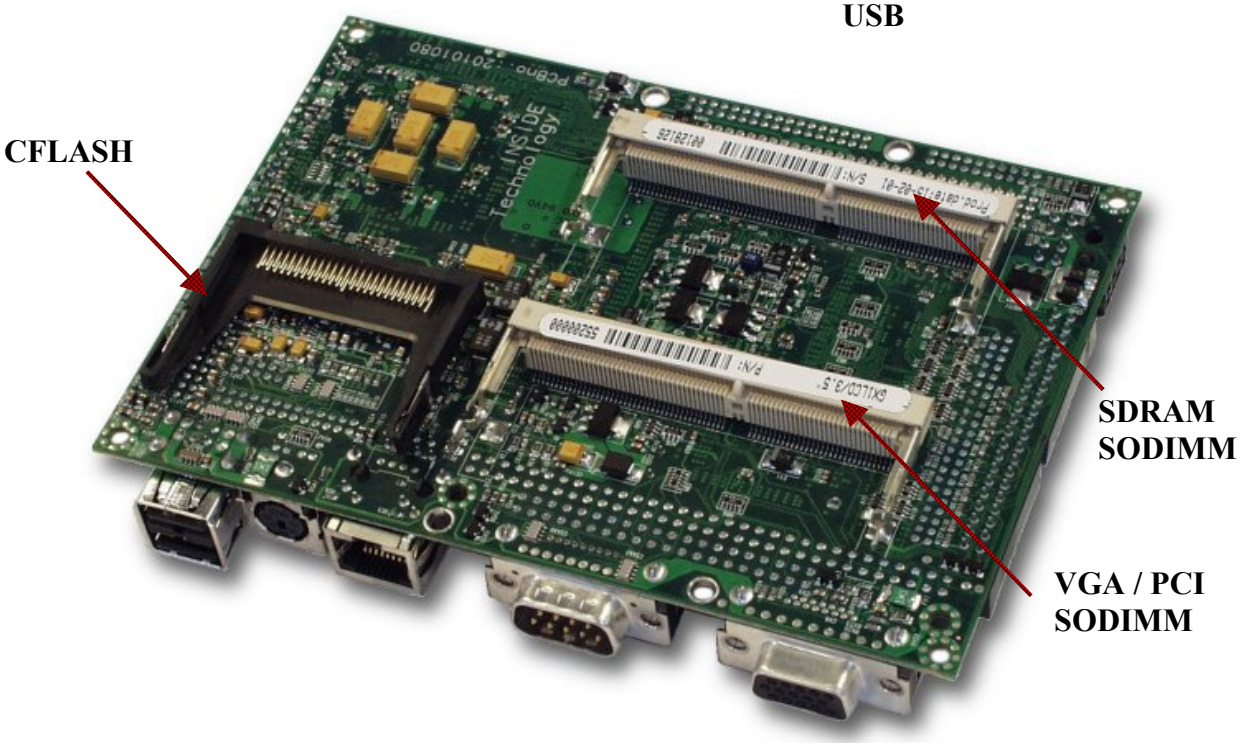
5.1 Connector layout – GX1LCD/S





5.2 Connector layout – GX1LCD/3.5”





5.3 Power Connector (PWRCON)

Different Power connectors are used for the GX1LCD/3.5" and GX1LCD/S Boards.

5.3.1 GX1LCD/S Board

Although power may be provided to the board by means of an ISA backplane, it is always recommended to use the onboard power connector.

Note	Pull U/D	Ioh/Iot	Type	Signal	PIN		Signal	Type	Ioh/Iot	Pull U/D	Note
3				VCCsw	2	1	VCC				2
				GND	4	3	GND				
1				-12V	6	5	+12V				1

Note:
1. +/12V is not used and only directed to the PC104 connector.
2. This pin is used for onboard supply of the onboard 5V circuits.
3. This pin is used for supply of the onboard switch mode regulators.

5.3.2 GX1LCD/3.5 Board

Note	Pull U/D	Ioh/Iot	Type	Signal	PIN		Signal	Type	Ioh/Iot	Pull U/D	Note
				GND	2	1	GND				
3				VCCsw	4	3	VCC				2
4				PSON#	6	5	SB5V				
1				-12V	8	7	+12V				1

Note:
1. +/12V is not used and only directed to the PC104 connector.
2. This pin is used for onboard supply of the onboard 5V circuits.
3. This pin is used for supply of the onboard switch mode regulators.
4. PSON is an output to be used for turning external ATX Power supplies On/Off. This feature is not supported on GX1LCD/3.5" boards with P/Ns: 56220000.

5.3.3 General Power Supply Requirements

The requirements to the supply voltages are as follows:

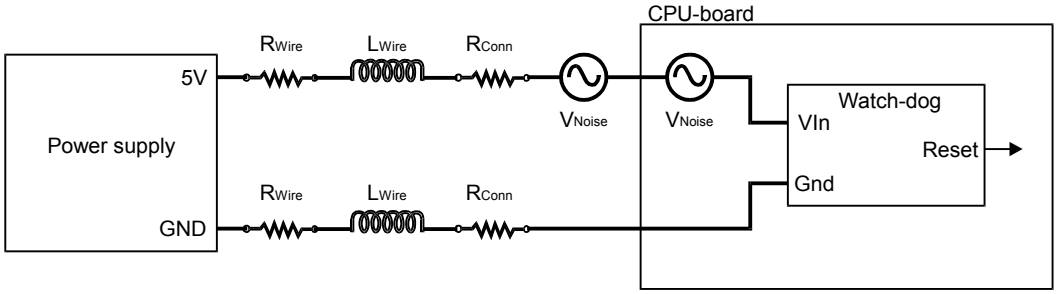
Supply	Min	Max	Note
VCC	4.76V	5.25V	Minimum voltage should be 4.875V for compliance with [1].
+12V	11.4V	12.6V	Should be ±5% for compliance with [1] and [2].
–12V	–12.6V	–11.4V	Should be ±5% for compliance with [1] and [2].

The +12V and –12V are only required if devices attached to the PC104 or PC104+ bus requires ±12V.

On-board switch mode supplies generate the CPU core voltage and 3.3V. The 3.3V supply is available in a number of connectors. The total 3.3V current draw from these connectors may not exceed 1A. Violation of this limit will result in unreliable board operation and may result in permanent damage of the board.

In order to ensure safe operation of the board, the onboard hardware watchdog monitors the supply voltage and asserts reset when the VCC supply is below 4.76V (max). This ensures that the board is running only while the components operate in their specified voltage range. This voltage limit obviously applies to the voltage seen by the supply watch-dog on the board.

In order to meet the minimum VCC requirement, the voltage should be higher at the power supply due to losses from the power supply to the board as illustrated below:



The physical equivalent of the components is as follows:

R_{Conn}	Contact resistance in connectors
R_{Wire}	Wire resistance
L_{Wire}	Inductance of wires
V_{Noise}	Noise in supply introduced by the board, the power supply itself and by other equipment attached to the 5V supply

It is obviously desirable to reduce the contribution of all these components to maintain a voltage above 4.76V at any time. To achieve this, the following guidelines should be observed:

- Use wire with a high copper cross-section area to reduce the resistance and inductance.
- Reduce wire length and number of connectors to a minimum.
- Let power and ground wires follow each other in order to reduce inductance.
- Provide a good voltage margin in order to provide the best possible immunity to load transients and noise generated by the CPU board and other devices attached to the supply. A voltage of 5.0V measured on the board is recommended.

In systems with a high current draw, it should be considered to use power supplies with voltage sense. If the loads additionally have very different connection lengths from a common node and/or very different loads, it should additionally be considered to use power supplies with individual outputs.

5.4 Keyboard and PS/2 mouse connectors

Attachment of a keyboard or PS/2 mouse adapter may be done by means of pinrows (JPKBD, JPMSE) or by means of a combined PS/2 mouse and keyboard connector (KBD).
Both interfaces utilise open-drain signalling with on-board pull-up. Although this interface from a hardware point of view allows multiple devices, it cannot be guaranteed since the keyboard and mouse protocol is not prepared for multiple devices.

Power to the PS/2 mouse and keyboard is provided through a 1.1A fuse. This supply is shared with a 5V supply in the CRT connector.

The signals of the PS/2 mouse interface are:

MSCLK	Bi-directional clock signal used to strobe data/commands from/to the PS/2 mouse.
MSDAT	Bi-directional serial data line used to transfer data from or commands to the PS/2 mouse.

The signals of the keyboard interface are:

KDBCLK	Bi-directional clock signal used to strobe data/commands from/to the PC-AT keyboard.
KBDDAT	Bi-directional serial data line used to transfer data from or commands to the PC-AT keyboard.

The connectors are defined in the following sections.

5.4.1 MINI-DIN combined keyboard and mouse Connector (KBD)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
	1K	/16	IOC	MSCLK	6 5	KBDCLK	IOC	/16	1K	
	-	-	PWR	VCC	4 3	GND	PWR	-	-	
	1K	/16	IOC	MSDAT	2 1	KBDDAT	IOC	/16	1K	

5.4.2 Pin-row Keyboard Connector (JPKBD)

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	KBDCLK	IOC	/16	1K	
2	KBDDAT	IOC	/16	1K	
3	NC	-	-	-	
4	GND	PWR	-	-	
5	VCC	PWR	-	-	

5.4.3 Pin-row PS/2 Mouse Connector (JPMSE)

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	MSCLK	IOC	/16	2K7	
2	MSDAT	IOC	/16	2K7	
3	NC	-	-	-	
4	GND	PWR	-	-	
5	VCC	PWR	-	-	

5.5 Display Connectors

The GX1LCD board family provides two basic types of interfaces to a display: Analog CRT interface and a digital interface typically used with flat panels.

5.5.1 CRT Connector (CRT)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN			Signal	Type	Ioh/Iol	Pull U/D	Note
						6		ANA-GND	PWR	-	-	
	/75R	*	A0	RED	1		11	NC	-	-	-	
						7		ANA-GND	PWR	-	-	
	/75R	*	A0	GREEN	2		12	DDCDAT	IO	TBD	3K3	
						8		ANA-GND	PWR	-	-	
	/75R	*	A0	BLUE	3		13	HSYNC	O	TBD		
						9		VCC	PWR	-	-	1
	-	-	-	NC	4		14	VSYNC	O	TBD		
						10		DIG-GND	PWR	-	-	
	-	-	PWR	DIG-GND	5		15	DDCCLK	IO	TBD	3K3	

Note :

1. VCC supply is shared with keyboard and mouse. The common fuse is 1.1A.

5.5.2 Signal Description - CRT Connector

HSYNC	CRT horizontal synchronisation output.
VSYNC	CRT vertical synchronisation output.
DDCCLK	Display Data Channel Clock. Used as clock signal to/from monitors with DDC interface.
DDCDAT	Display Data Channel Data. Used as data signal to/from monitors with DDC interface.
RED	Analog output carrying the red colour signal to the CRT. For 75 Ohm cable impedance.
GREEN	Analog output carrying the green colour signal to the CRT. For 75 Ohm cable impedance.
BLUE	Analog output carrying the blue colour signal to the CRT. For 75 Ohm cable impedance.
DIG-GND	Ground reference for HSYNC and VSYNC.
ANA-GND	Ground reference for RED, GREEN, and BLUE.

5.5.3 Flat Panel Connector (PANEL)

Note	Type	Signal	Pin		Signal	Type	Note
	PWR	LCDVCC	1	2	LCDVCC	PWR	
		NC	3	4	ENVCC	OT	
	O	CD0S	5	6	GND	PWR	
	OT	DE	7	8	ENBKL	O	
	PWR	GND	9	10	LP	OT	
	OT	FLM	11	12	GND	PWR	
	OT	SHFCLK	13	14	GND	PWR	
	OT	P0	15	16	P1	OT	
	PWR	GND	17	18	P2	OT	
	OT	P3	19	20	GND	PWR	
	OT	P4	21	22	P5	OT	
	PWR	GND	23	24	P6	OT	
	OT	P7	25	26	GND	PWR	
	OT	P8	27	28	P9	OT	
	PWR	GND	29	30	P10	OT	
	OT	P11	31	32	GND	PWR	
	OT	P12	33	34	P13	OT	
	PWR	GND	35	36	P14	OT	
	OT	P15	37	38	GND	PWR	
		NC	39	40	NC		
	OT	P16	41	42	P17	OT	
	OT	P18	43	44	P19	OT	
	PWR	GND	45	46	P20	OT	
	OT	P21	47	48	P22	OT	
	OT	P23	49	50	GND	PWR	

The PANEL connector is only available on GX1LCD/3.5” boards when using a SODIMM LCDADPT module.

5.5.4 Signal Description - Flat Panel Connector

Signal	Description
P23..0	3.3V TFT Flat panel data output for 9, 12, 18 or 24 bit panels. The flat panel data and control outputs are all controlled for secure power-on/off sequencing
SHFCLK	Shift clock. Pixel clock for flat panel data.
LP	Latch Pulse. Flat panel equivalent of HSYNC (horizontal synchronisation).
FLM	First Line Marker. Flat panel equivalent of VSYNC (vertical synchronisation).
DE	Output Display Enable.
ENBKL	Enable backlight signal.
CD0S	General Purpose Control Signal.
ENVCC	Enable VCC. Signal to control the panel power-on/off sequencing. A high level may be used externally to turn on the VCC (5 V or 3V3 DC) to the panel.
LCDVCC	VCC supply to the flat panel. This supply includes power-on/off sequencing. The flat panel supply may be either 5V DC or 3.3V DC depending on the CMOS configuration. Maximum load is 1A at both voltages.

Note: All flat panel signalling are 3.3V level and compliant to the standard TTL high/low voltages. Displays requiring 5V signalling (Non-TTL Compatible) can not be used.

5.5.5 Signal Configuration - Flat Panel Displays

The panel connection with the GX1LCD CS5530A XPRESS Graphics is as follows:

Pin name	Color TFT, 9 Bit 640x480	Color TFT, 9 Bit 1024x768	Color TFT 12 Bit	Color TFT 18 Bit
Pixels/clk	1	2	1	1
P0	-	-	-	-
P1	-	-	-	-
P2	-	B10	-	B0
P3	-	B11	-	B1
P4	-	B12	B0	B2
P5	B0	B00	B1	B3
P6	B1	B01	B2	B4
P7	B2	B02	B3	B5
P8	-	-	-	-
P9	-	-	-	-
P10	-	G10	-	G0
P11	-	G11	-	G1
P12	-	G12	G0	G2
P13	G0	G00	G1	G3
P14	G1	G01	G2	G4
P15	G2	G02	G3	G5
P16	-	-	-	-
P17	-	-	-	-
P18	-	R10	-	R0
P19	-	R11	-	R1
P20	-	R12	R0	R2
P21	R0	R00	R1	R3
P22	R1	R01	R2	R4
P23	R2	R02	R3	R5

When running with simultaneous CRT and TFT display, CRT is only supported in 640x480 and 800x600 modes for the XPRESS Graphics controller (CS5530A).

For both controllers, the principle of attachment of TFT panels is that the bits for red, green and blue use the most significant bits and skip the least significant bits if the display interface width of the TFT panel is insufficient.

5.5.6 Panel Link (PNLLINK)

The Panel Link connector provides a convenient attachment of displays with longer cables or where it is desirable to reduce the emission of the cables.
The pinout defined below provides the following features:

- Complete set of balanced Panellink signals operating at up to 650MHz (resolution up to 1024x768).
- Feed-through of power. Power-supply at the receiver end or additional cables may be omitted for light loads.
- Feed-through of selected RS232 signals from COM1 (onboard Panellink connector on GX1LCD/S only). A mouse or other devices may be utilised without additional cables. This requires RS232 Plug described later.

The pinout is shown below:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	LCDVCC	1	14	+12	PWR	-	-	
	-	-	PWR	LCDVCC	2	15	+12	PWR	-	-	
	-		OT	TX2+	3	16	+12	PWR	-	-	
	-		OT	TX2-	4	17	**DCLK**	IO	-	3K3	1
	-		OT	TX1+	5	18	**DDAT**	IO	-	3K3	1
	-		OT	TX1-	6	19	GND	PWR	-	-	
	-		OT	TX0+	7	20	GND	PWR	-	-	
	-		OT	TX0-	8	21	GND	PWR	-	-	
	-		OT	TXC+	9	22	FCOM0				2
	-		OT	TXC-	10	23	FCOM1				2
	-	-	PWR	GND	11	24	FCOM2				2
	-	-	PWR	GND	12	25	FCOM3				2
	-	-	PWR	+12	13	26	**DFP_PLUG**	I	-	/20K	1

Note:

1. These pins are redefined compared to the 686LCD/s and /MG board range. This may cause a problem with some Panel Link receivers designed for the 686LCD/s or /MG range. Please check with Kontron Technology Support Team.
2. Serial Port lines are only present on GX1LCD/S onboard Panellink connector.

5.5.7 Signal Description - Panel Link (PNLLINK)

TXC+/TXC-	Low voltage swing differential output clock pair. For twisted pair cable with 100 Ohm characteristic balanced impedance.
TX0+/TX0-	Low voltage swing differential output data pair. For twisted pair cable with 100 Ohm characteristic balanced impedance. This pair transmits the flat panel signals : P0..7, LP and FLM.
TX1+/TX1-	Low voltage swing differential output data pair. For twisted pair cable with 100 Ohm characteristic balanced impedance. This pair transmits the flat panel signals : P8..15.
TX2+/TX2-	Low voltage swing differential output data pair. For twisted pair cable with 100 Ohm characteristic balanced impedance. This pair transmits the flat panel signals : P16..23.
LCDVCC	VCC supply to the flat panel. This supply includes onboard power on/off sequencing. The flat panel supply may be either 5 V DC or 3.3 V DC depending on the display configuration in the BIOS setup. Maximum external load is 0.25A (10meter cable).
DFP_PLUG	Signal used to detect if a monitor is attached. The monitor should connect this pin to 5V.

The signals FCOMn provide a feedthrough signals from the COM1 port (GX1LCD/S onboard Panellink connector only). The table below defines these signals for the two COM2 operation modes and with an optional plug:

Signal	Direction	COM1 pin	RS232 mode	RS232 Plug	RS485 mode
FCOM0	In	2	RxD	RxD	RxD-
FCOM1	In (Out)	1	DCD	RTS (out)	RxD+
FCOM2	Out	3	TxD	TxD	TxD+
FCOM3	Out	4	DTR	DTR	TxD-

The *RS232 Plug* column indicates the signal levels with an RS232-plug, which short DCD (pin 1) and RTS (pin 7). The resulting set of signals is sufficient for attachment of most serial mouse devices. This Plug is included in the Kontron Technology standard Panel Link accessory.

5.6 Floppy Disk Connector (FLOPPY)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	GND	1	2	DENSEL0#	OC	/48	-	
	-	-	PWR	GND	3	4	NC	-	-	-	
	-	-	PWR	GND	5	6	DENSEL1#	OC	/48	-	
	-	-	PWR	GND	7	8	INDEX#	IS	-	1K	
	-	-	PWR	GND	9	10	MOTEA#	OC	/48	-	
	-	-	PWR	GND	11	12	DRVB#	OC	/48	-	
	-	-	PWR	GND	13	14	DRVA#	OC	/48	-	
	-	-	PWR	GND	15	16	MOTEB#	OC	/48	-	
	-	-	PWR	GND	17	18	DIR#	OC	/48	-	
	-	-	PWR	GND	19	20	STEP#	OC	/48	-	
	-	-	PWR	GND	21	22	WDATA#	OC	/48	-	
	-	-	PWR	GND	23	24	WGATE#	OC	/48	-	
	-	-	PWR	GND	25	26	TRK0#	IS	-	1K	
	-	-	PWR	GND	27	28	WPT#	IS	-	1K	
	-	-	IS	MEDIA0	29	30	RDATA#	IS	-	1K	
	-	-	PWR	GND	31	32	SIDE1#	OC	/48	-	
	-	-	PWR	GND	33	34	DSKCHG#	IS	-	1K	

Signal Description:

RDATA#	Read Disk Data, active low, serial data input from the floppy disk drive.
WDATA#	Write Disk Data, active low, serial data output to the floppy disk drive.
WGATE#	This output signal enables the head of the selected disk drive to write to the disk.
MOTEA#	This output signal enables the motor in floppy disk drive A.
MOTEB#	This output signal enables the motor in floppy disk drive B.
DRVA#	Active low output signal to select floppy disk drive A.
DRVB#	Active low output signal to select floppy disk drive B.
SIDE1#	This output signal selects side of the disk in the selected drive.
DIR#	This signal controls the direction of the floppy disk drive head movement during a seek operation. A low level request steps through centre.
STEP#	This output signal supplies step pulses to move the head during seek operations.
DENSEL0/1#	This output indicates whether a low data rate (250/300kbps at low level) or a high data rate (500/1000kbps at high level) has been selected.
TRK0#	Floppy Disk Track 0, active low input to indicate that the head of the selected drive is at track 0.
INDEX#	Floppy Disk Index, active low input indicates the beginning of a disk track.
WPT#	Active low input signal indicating that the selected drive contains a write protected disk.
DSKCHG#	Input pin that senses whether the drive door has been opened or the diskette has been changed.

5.7 Harddisk and Compact flash interface

Two harddisk controllers are available on the board – a primary and a secondary controller. Standard harddisks may be attached to the board by means of the 40 pin IDC connector. A compact flash connector on the bottom side of the board may be used for a compact flash disk. For the GX1LCD/3.5" board a 40-pin secondary IDC connector is also available on the board that share the Secondary IDE channel with the compact flash interface.

Each connector has a dedicated controller.

The CS5530A harddisk controller supports Bus master IDE, ultra DMA and standard operation modes. Ultra DMA mode is the fastest with up to 33 MB/Sec bandwidth, to utilise this mode a special driver is required (see Software Manual).

NOTE: For GX1LCD/S boards with board partnumbers: 5532xxxx and 5533xxxx ("x"=don't care) support is not included of Compact flash disk and Secondary harddisk when connected to the board at the same time. Support of either a Compact flash, one Secondary harddisk, or two Secondary harddisks is available on all versions of the GX1LCD/S boards.

The signals used for the harddisk interface are the following:

DA2..DA0	Address lines, used to address the I/O registers in the IDE hard disk.
HDCS1..0#	Hard Disk Chip-Select. HDCS0# selects the primary hard disk.
D15..8	High part of data bus.
D7..0	Low part of data bus.
IOR#	I/O Read.
IOW#	I/O Write.
IORDY1..0#	This signal may be driven by the hard disk to extend the current I/O cycle.
RESET#	Reset signal to the hard disk. The signal is similar to RSTDRV in the PC-AT bus.
IRQ14	Interrupt line from hard disk. Connected directly to PC-AT bus.
DDREQ0	Disk DMA Request might be driven by the IDE hard disk to request bus master access to the PCI bus. The signal is used in conjunction with the PCI bus master IDE function and is not associated with any PC-AT bus compatible DMA channel.
DDACK0#	Disk DMA Acknowledge. Active low signal grants IDE bus master access to the PCI bus.
HDACT#	Signal from hard disk indicating hard disk activity. The signal level depends on the hard disk type, normally active low. The signal is routed directly to the connector JPFEAT.

All of the above signals are compliant to [4].

The pinout of the connectors are defined in the following sections.

5.7.1 IDE Hard Disk Connector (IDE1, IDE2)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	TBD	O	RESET#	1	2	GND	PWR	-	-	
	-	TBD	IO	D7	3	4	D8	IO	TBD	-	
	-	TBD	IO	D6	5	6	D9	IO	TBD	-	
	-	TBD	IO	D5	7	8	D10	IO	TBD	-	
	-	TBD	IO	D4	9	10	D11	IO	TBD	-	
	-	TBD	IO	D3	11	12	D12	IO	TBD	-	
	-	TBD	IO	D2	13	14	D13	IO	TBD	-	
	-	TBD	IO	D1	15	16	D14	IO	TBD	-	
	-	TBD	IO	D0	17	18	D15	IO	TBD	-	
	-	-	PWR	GND	19	20	NC	-	-	-	
	3K3	-	I	DDRQ0	21	22	GND	PWR	-	-	
	-	TBD	O	IOW#	23	24	GND	PWR	-	-	
	-	TBD	O	IOR#	25	26	GND	PWR	-	-	
	1K65	-	I	IORDY0#	27	28	VCC	PWR	-	-	
	-	-	O	DDACK0	29	30	GND	PWR	-	-	
	10K	-	I	IRQ14	31	32	NC				
	-	TBD	O	DA1	33	34	NC				
	-	TBD	O	DA0	35	36	DA2	O	TBD	-	
	-	TBD	O	HDCS0#	37	38	HDCS1#	O	TBD	-	
	-	-	I	HDACT#	39	40	GND	PWR	-	-	

5.7.2 Compact flash Connector (CFLASH)

The pinout of the compact flash connector is shown below. Pin 1 is the marked by and arrow/triangle on the connector.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
2	-	TBD	IO	D3	2	1	GND	PWR	-	-	1
	-	TBD	IO	D5	4	3	D4	IO	TBD	-	
	-	TBD	IO	D7	6	5	D6	IO	TBD	-	
	-	-	PWR	GND	8	7	HDCS0#	O	TBD	-	
	-	-	PWR	GND	10	9	GND	PWR	-	-	
	-	-	PWR	GND	12	11	GND	PWR	-	-	
	-	-	PWR	GND	14	13	VCC	PWR	-	-	
	-	-	PWR	GND	16	15	GND	PWR	-	-	
	-	-	O	DA2	18	17	GND	PWR	-	-	
	-	-	O	DA0	20	19	DA1	O	-	-	
	-	TBD	IO	D1	22	21	D0	IO	TBD	-	
				NC	24	23	D2	IO	TBD	-	
				NC	26	25	NC				
	-	TBD	IO	D12	28	27	D11	IO	TBD	-	
	-	TBD	IO	D14	30	29	D13	IO	TBD	-	
	-	TBD	O	HDCS1#	32	31	D15	IO	TBD	-	
	-	TBD	O	IOR#	34	33	NC			-	
	-	-	PWR	VCC	36	35	IOW#	O	TBD	-	
	-	-	PWR	VCC	38	37	IRQ15	I	-	10K	
				NC	40	39	GND	PWR			
	1K65	-	I	IORDY1#	42	41	RESET#			-	
	-	-	PWR	VCC	44	43	NC				
				NC	46	45	NC				
	-	TBD	IO	D9	48	47	D8	IO	TBD	-	
1	-	-	PWR	GND	50	49	D10	IO	TBD	-	2

Note:

1. Pin is longer than average length of the other pins.
2. Pin is shorter than average length of the other pins.

5.8 Printer Port Connector (PRINTER).

The printer port connector is provided as an ICD26 connector for easy adaptation to the standard DB25 pinout.
The signal definition in standard printer port mode is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	1K	(12)/24	OC(O)	STB#	1	2	AFD#	OC(O)	(12)/24	1K	
	-	12/24	IO	PD0	3	4	ERR#	I	-	1K	
	-	12/24	IO	PD1	5	6	INIT#	OC(O)	(12)/24	1K	
	-	12/24	IO	PD2	7	8	SLIN#	OC(O)	(12)/24	1K	
	-	12/24	IO	PD3	9	10	GND	PWR	-	-	
	-	12/24	IO	PD4	11	12	GND	PWR	-	-	
	-	12/24	IO	PD5	13	14	GND	PWR	-	-	
	-	12/24	IO	PD6	15	16	GND	PWR	-	-	
	-	12/24	IO	PD7	17	18	GND	PWR	-	-	
	1K	-	I	ACK#	19	20	GND	PWR	-	-	
	1K	-	I	BUSY	21	22	GND	PWR	-	-	
	1K	-	I	PE	23	24	GND	PWR	-	-	
	1K	-	I	SLCT	25	26	GND	PWR	-	-	

If the DB25 ribbon cable adapter is used, the pinout will be as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	1K	(12)/24	OC(O)	STB#	1						
						14	AFD#	OC(O)	(12)/24	1K	
	-	12/24	IO	PD0	2						
						15	ERR#	I	-	1K	
	-	12/24	IO	PD1	3						
						16	INIT#	OC(O)	(12)/24	1K	
	-	12/24	IO	PD2	4						
						17	SLIN#	OC(O)	(12)/24	1K	
	-	12/24	IO	PD3	5						
						18	GND	PWR	-	-	
	-	12/24	IO	PD4	6						
						19	GND	PWR	-	-	
	-	12/24	IO	PD5	7						
						20	GND	PWR	-	-	
	-	12/24	IO	PD6	8						
						21	GND	PWR	-	-	
	-	12/24	IO	PD7	9						
						22	GND	PWR	-	-	
	1K	-	I	ACK#	10						
						23	GND	PWR	-	-	
	1K	-	I	BUSY	11						
						24	GND	PWR	-	-	
	1K	-	I	PE	12						
						25	GND	PWR	-	-	
	1K	-	I	SLCT	13						

The interpretation of the signals in standard Centronics mode (SPP) with a printer attached is as follows:

PD7..0	Parallel data bus from PC board to printer. The data lines are able to operate in PS/2 compatible bi-directional mode.
SLIN#	Signal to select the printer sent from CPU board to printer.
SLCT	Signal from printer to indicate that the printer is selected.
STB#	This signal indicates to the printer that data at PD7..0 are valid.
BUSY	Signal from printer indicating that the printer cannot accept further data.
ACK#	Signal from printer indicating that the printer has received the data and is ready to accept further data.
INIT#	This active low output initialises (resets) the printer.
AFD#	This active low output causes the printer to add a line feed after each line printed.
ERR#	Signal from printer indicating that an error has been detected.
PE#	Signal from printer indicating that the printer is out of paper.

The printer port additionally supports operation in the EPP and ECP mode as defined in [3].

5.9 Serial Ports

Up to 4 serial ports are available on the GX1LCD/S board and up to 2 serial ports are available on the GX1LCD/3.5" board.

Depending on the mounting variant the GX1LCD board will include one selectable RS232 or RS422/485 port. The mode is software selectable between operation: RS232 or RS422 mode. Use of external loop-backs additionally provides support for RS485.
The operation mode is software configurable and may be selected in the BIOS setup. It should however be noticed that the power-up default is RS232 mode which means that the port always will be in the RS232 mode during the first seconds after power-up or hardware reset.

Serial port 2 provides a standard RS232 interface, but may also be utilised for IrDA.

Serial ports 3 and 4 are optionally available on GX1LCD/S.

The typical interpretation of the signals in the COM ports in RS232 mode is as follows:

TxD	Serial output. This signal sends serial data to the communication link. The signal is set to a marking state on hardware reset when the transmitter is empty or when loop mode operation is initiated.
RxD	Serial input. This signal receives serial data from the communication link.
DTR	Data Terminal Ready. This signal indicates to the modem or data set that the on-board UART is ready to establish a communication link.
DSR	Data Set Ready. This signal indicates that the modem or data set is ready to establish a communication link.
RTS	Request To Send. This signal indicates to the modem or data set that the on-board UART is ready to exchange data.
CTS	Clear To Send. This signal indicates that the modem or data set is ready to exchange data.
DCD	Data Carrier Detect. This signal indicates that the modem or data set has detected the data carrier.
RI	Ring Indicator. This signal indicates that the modem has received a telephone-ringing signal.

The connector pinout for each operation mode is defined in the following sections.

5.9.1 Serial Port 1 DB9 Connector (COM1) in RS232 Mode

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	GND	5						
						9	RI	I	-	/5K	
	-		O	DTR	4						
						8	CTS	I	-	/5K	
	-		O	TxD	3						
						7	RTS	O		-	
	/5K	-	I	RxD	2						
						6	DSR	I	-	/5K	
	/5K	-	I	DCD	1						

5.9.2 Serial Port 1 DB9 Connector (COM1) in RS422/485 Mode

RS422/485 mode uses differential mode signalling increasing noise immunity. Longer cables and higher transfer rates may be utilised. All differential lines should be terminated in the receiver end with a resistor matching the characteristic differential impedance of the cable. These resistors could be placed in the cable housing. For Setup of the transmitter Enabling signal refer to the software Manual.
The pinout in the RS422 mode is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	GND	5						
						9	RTS-	OT		-	1
1	-		OT	TxD-	4						
						8	CTS+	I		/15K	
1	-		OT	TxD+	3						
						7	RTS+	OT		-	1
	/15K	-	I	RxD-	2						
						6	CTS-	I		/15K	
	/15K	-	I	RxD+	1						

Note :
1. These drivers (TxD and RTS) may be tri-stated so multiple drivers can be used on the same media. The controlling signal may be the RTS, DTR or in a permanently on/off configuration. The signal and polarity is selected in the BIOS setup.

Operation in RS485 mode may be achieved by adding loopbacks from the transmitter to the receiver (Pins 3-1, 4-2, 7-8 and 9-6).

5.9.3 Pin Header Serial Port 2 Connector (COM2)

The RS232 driver of serial port 2 utilises charge pumps requiring only a 5V supply.
The pinout of Serial port 2 is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
		-	I	DCD	1	2	DSR	I	-		
		-	I	RxD	3	4	RTS	O		-	
	-		O	TxD	5	6	CTS	I	-		
	-		O	DTR	7	8	RI	I	-		
	-	-	PWR	GND	9	10	5 V	PWR	-	-	

If the DB9 adapter (ribbon cable) is used, the DB9 pinout will be identical to the pinout of Serial port 1 operating in RS232 mode as defined in section 5.9.1.

5.9.4 Pin Header Serial Port 3&4 Connector (COM3 & COM4)

The connector pinout is identical to the COM2 pinout defined in section 5.9.3.

5.10 Ethernet connector (ETHERNET)

In order to achieve the specified performance of the Ethernet port, Category 5 twisted pair cables must be used.
The pinout of the RJ45 connector is as follows:

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
8		-	-	-	1
7		-	-	-	1
6	RXD-	I	-	-	
5		-	-	-	2
4		-	-	-	2
3	RXD+	I	-	-	
2	TXD-	O	-	-	
1	TXD+	O	-	-	

Note:

1. Pin 7 and 8 are shorted and terminated by 75Ω to a voltage potential which is common to the to the common-mode level of all the connector signals.
2. Pin 4 and 5 are shorted and terminated by 75Ω to a voltage potential which is common to the to the common-mode level of all the connector signals.

Differential mode transmission is used for the transmitter (TXD+/TXD-) and receiver (RXD+/RXD-).

5.11 USB Connector (USB)

The USB interface provides a differential mode serial interface with transfer rates up to 12Mbps. The interface consists of only 4 signals.

Two USB lines are provided which have data signals denoted D0+/- and D1+/-.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN CH0	PIN CH1	Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	GND	4	8	GND	PWR	-	-	
	/15K	0.25/2	IO	D0+	3	7	D1+	IO	0.25/2	/15K	
	/15K	0.25/2	IO	D0-	2	6	D1-	IO	0.25/2	/15K	
1	-	-	PWR	VCC	1	5	VCC	PWR	-	-	1

Note :
1. The USB 5V VCC supply is on-board fused with a 1.1A resetable fuse.

5.11.1 USB Signals

D0+, D0-	Differential bi-directional data signal for USB channel 0. Clock is transmitted along with the data using NRZI encoding. The signalling rate is up to 12MBs.
D1+, D1-	Differential bi-directional data signal for USB channel 1. Clock is transmitted along with the data using NRZI encoding. The signalling rate is up to 12MBs.
VCC	5V VCC supply for external devices. Fused with 1.1A resetable fuse.

5.12 GX1LCD/S Audio and IRDA connector (JPAUX)

The AUX connector contains the signals related to the IRDA interface and the Audio interface.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
			O	SPK_L	1	2	SPK_R	O			
			PWR	GND	3	4	GND	PWR			
	-	-	PWR	VCC	5	6	VCC	PWR	-	-	
	-	12/24	O	IRTX	7	8	IRRX	I	-	-	
	-	-	I	RESERVED	9	10	GPIO	IO	-	-	
	-	-	PWR	GND	11	12	GND	PWR	-	-	
			O	LOUT_R	13	14	LOUT_L	O			
			I	GND	15	16	LIN_L	I			
			I	LIN_R	17	18	GND	PWR			
	-	-	I	MIC	19	20	MIC_BIAS	O	-	-	1

5.12.1 Audio signals

SPK_L, SPK_R	Left and right speaker output. These are the speaker outputs directly from the speaker amplifier. Coupling capacitors must be used in order to avoid DC-currents in the speakers, typically 330uF/10V. If the Sound Bracket is used these are supplied on the PCB. GND should be used as return for each speaker. Maximum power: 0,5W@4Ω load for each channel.
LOUT_R, LOUT_L	Right and left line out signals. Both signals are capacitor coupled and should have GND as return.
LIN_R, LIN_L	Right and left line in signals.
MIC, MIC_BIAS	The MIC signal is used for microphone input. This input is fed to the left microphone channel. MIC_BIAS provides 3.3V supplied through 3.2kΩ with capacitive decoupling to GND. This signal may be used for bias of some microphone types.

5.12.2 IRDA signals

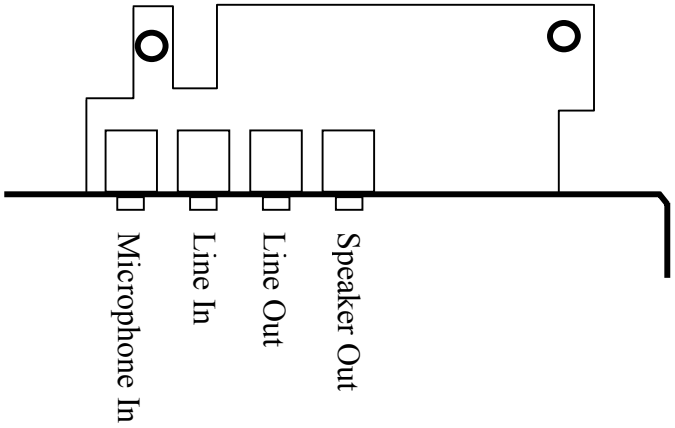
IRTX	Infrared transmitter data output. The infrared module use the UART normally assigned for Serial Port 2 for the IrDA mode.
IRRX	Infrared receiver data input. This pin is used for low data rates (<115KBps) are used.

5.12.3 Other signals

GPIO	General purpose IO.

5.12.4 Audio Bracket

For the 586LCD/Gxm Plus and 686LCD/Gxm board series an Audio bracket is optionally included in the shipment. This bracket routes the Audio signals to four Mini Jacks, one for each of the lines: Microphone Input, Line In, Line Out and Speaker Out.
The figure below shows the positions of the individual functionality in the bracket.



5.13 GX1LCD/S CD-ROM input (CDROM)

CD-rom audio input may be connected to this connector. It may also be used as a secondary line in signal if two inputs are required.

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
4	CD_Right	I	-	-	
3	CD_GND	I	-	-	
2	CD_Left	I	-	-	
1	CD_GND	I	-	-	

CD_Right, CD_Left	Right and left CD audio input lines.
CD_GND	GND for Left and Right CD. This GND level is **not** shorted to the board GND.

5.14 GX1LCD/3.5" Bracket Module Interface

The Bracket Module Interface on the GX1LCD/3.5" Board is made by the two connectors: BRACK1 and BRACK2 which contains signals for support of the following features: Audio, Fan Control, IrDA, and AC97 interface. The signals can be accessed using different Stackable Bracket Modules offered by KONTRON or some of the signals can be wired directly to external connectors / circuits.

5.14.1 Bracket Module Interface (BRACK1)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	AI	MIC_IN	1	2	MIC_BIAS	AI	-	-	
	-	-	PWR	A_GND	3	4	A_GND	PWR	-	-	
	-	-	AO	MONO_OUT	5	6	PHONE_IN	AI	-	-	
	-	-	AI	LINE_IN_L	7	8	LINE_IN_R	AI	-	-	
	-	-	AI	CD_IN_L	9	10	CD_IN_R	AI	-	-	
	-	-	AO	LINE_OUT_L	11	12	LINE_OUT_R	AO	-	-	
	-	-	AO	RAW_LOUT_L	13	14	RAW_LOUT_R	AO	-	-	
	-	-	PWR	CD_GND	15	16	GND	PWR	-	-	
	-	-		NC	17	18	NC		-	-	
	-	-		NC	19	20	NC		-	-	
	-	-	PWR	5V	21	22	SB5V	PWR	-	-	
	-	-	I	NC	23	24	+12V	PWR	-	-	
	-	-		NC	25	26	NC		-	-	
	-	-		NC	27	28	NC		-	-	
	-	-		NC	29	30	NC		-	-	

	Audio input / output.
MIC, MIC_BIAS	The MIC signal is used for microphone input. This input is fed to the MIC1 microphone channel. MIC_BIAS provides 2.25V supplied through a 2.2kΩ resistor. This signal may be used for bias / supply of some microphone types.
PHONE_IN	Input from telephony subsystem speakerphone.
MONO_OUT	Output to telephony subsystem speakerphone.
LINE_IN_L, LINE_IN_R	Right and left line in signals.
CD_IN_L, CD_IN_R	Left and right CD audio input lines.
LINE_OUT_L, LINE_OUT_R	Right and left line out signals. Both signals are capacitor coupled and should have AGND as return.
RAW_LOUT_L, RAW_LOUT_R	Raw right and left line out signals. Both signals are DC coupled and should have capacitors / filter added externally.
AGND	Audio GND, should be used as reference for all audio signals.
CD_GND	GND reference for the CD_IN_L and CD_IN_R signals.

5.14.2 Bracket Module Interface (BRACK2)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-		NC	1	2	NC		-	-	
	-	-		NC	3	4	NC		-	-	
	-	-		NC	5	6	NC		-	-	
	-	-		NC	7	8	NC		-	-	
	-	-	PWR	5V	9	10	GND	PWR	-	-	
	-	-	O	AC_CLK	11	12	NC		-	-	
	-	TBD	O	AC_RST#	13	14	AC_SYNC	O	TBD	/100K	
	/100K	TBD	O	SDATO	15	16	BIT_CLK	I	-	-	
	/100K	-	I	SDATI	17	18	EAPD	O	TBD	-	
		-	-	NC	19	20	SB3V3	PWR	-	-	
	-	-	PWR	3V3	21	22	BSERCLK	I/O	4/12	75K	
	-	TBD	O	PCIRST#	23	24	BSERDAT	I/O	4/12	75K	
	-	8/8	O	IRTX	25	26	IRRX	I	-	-	
	-	-		NC	27	28	RESERVED	I	-	TBD	
	-	-		NC	29	30	NC		-	-	

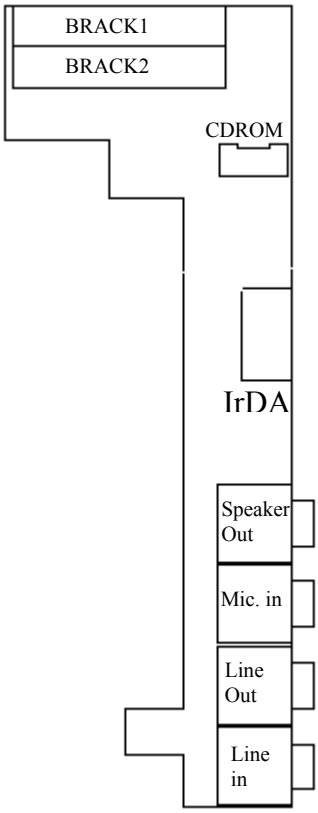
	AC97 Interface.
	The AC97 interface can with external codec circuits like AC3 surround sound applications.
AC_SYNC	48 kHz signal, which is used to synchronise CODEC's.
SDATO	Serial data output to CODEC's.
SDATI	Serial data input from CODEC's.
AC_RST#	Hardware reset signal for CODEC'c.
AC_CLK	24.576 MHz clock signal, which can be used for external primary CODEC'c.
EAPD	External Amplifier Power Down, output signal to external amplifier. This is not supported currently.
	Infrared Communication.
IRTX, IRRX	Infrared transmit output / receive input. When selecting "IR" mode for Serial port 2 in the BIOS, IrDA communication up to 115KBps is supported.
	Other signals
PCIRST#	Reset signal from PCI-bus.
BSERCLK, BSERDAT	Serial I^2C bus signals for used on bracket modules.

5.14.3 GX1LCD/3.5” Bracket Modules

Sound /IrDA Bracket Module

The Sound/IrDA Bracket Module offers CDROM input, Speaker Out, Microphone in, Line In and Out as well as IrDA transmitter/ receiver are included on the bracket module.

Connector Definition



The Speaker Out connector can typically supply 200 mW per channel of continuous average power to an 8R load with 0.1% (THD).

The Microphone input is single-ended supporting most common types of microphones. Phantom power is supplied to the connector (2.25V).

5.15 Fan connector (FAN)

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
3	TAC	PWR	-	-	
2	VCC	PWR	-	-	
1	GND	PWR	-	-	

Signal description:

VCC	+5V Supply for Fan
GND	GND Return
TAC	Tacho input for measuring Fan rotation.

5.16 Feature Connector (FEATURE)

The feature connector provides a number of signals to monitor and change the board status and operation. In addition to this are 8 general-purpose inputs/outputs.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	VCC/VTR	1	2	EXTRST#	I	-	2K2	
	-	4/8	O	PWRGD#	3	4	RESERVED		-	-	
	1K	-	I	EXTREQ#	5	6	PWRON#	OC	/24	1K	
	-	-	O	EXTSPK	7	8	BUTIN	I	-	/1K	
	-	HD	O	HDACT#	9	10	GND	PWR	-	-	
	/10K	2/4	IO	GPIO0	11	12	GPIO1	IO	2/4	/10K	
	/10K	4/8	IO	GPIO2	13	14	GPIO3	IO	2/4	/10K	
	/10K	2/4	IO	GPIO4	15	16	GPIO5	IO	2/4	/10K	
	/10K	2/4	IO	GPIO6	17	18	GPIO7	IO	2/4	/10K	
	-	-	PWR	EXTBATT	19	20	GND	PWR	-	-	

The function of the signals is as follows:

EXTRST#	External reset input. A logic low level at this pin will reset the entire CPU board.
PWRGD#	Indicate whatever the board is reset due to power fault, supervision reset or by external reset. High: The board is reset. Low: The board is not reset due to one of the above-mentioned causes.
EXTREQ#	External Request Switch. This active low input signal can activate NMI-, SMI- or a standard AT-Bus IRQ-interrupt. This feature requires a vendor code.
EXTSPK	An external speaker may be connected between this pin and ground. The speaker impedance must be 8 ohms or higher. This signal provides the sound of the PC-speaker and not for the XPRESS/SB16 audio, which is available in JPAUX or BRACK1. For improved sound 'quality', an amplifier or speaker with higher impedance (150Ω or more) should be used.
HDACT#	Hard Disk Activity. This pin is connected directly to the HDACT# signal in the JPIDE connector. The signal is fed through a 330R series resistor for direct connection of a LED
GPIO7..0	General Purpose Inputs / Outputs. These Signals may be controlled through use of Kontron API software or by using direct I/O access as described in the SW manual.
EXTBATT	An external primary cell battery can be connected between this pin and GND. The battery will not be recharged. The battery voltage should be within the range : 2.5 - 4.0 V DC. Typical current is 1 µA.
VCC	5 V DC supply output for connection to LEDs or switches. No more than 100 mA DC may be drawn from this pin.
PWRON#	Active low output signal that could be used to turn power supply ON. The signal will go low when BUTIN is pulsed high. This feature is not supported on boards with Board P/N 55210000, 55220000, 55310000, and 55320000.
BUTIN	This signal can be used to turn external ATX power supply ON/OFF by supplying low level pulse to this pin. This feature is not supported on boards with Board P/N 55210000, 55220000, 55310000, and 55320000.

5.17 ISA bus connectors

5.17.1 PC104 Connector (PC104XT & PC104AT)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	GND	B32	A32			GND	PWR	-	-	
	-	-	PWR	GND	B31	A31			SA0	IO	8/8	-	
	-	8/8	O	OSC	B30	A30			SA1	IO	8/8	-	
	-	-	PWR	VCC	B29	A29			SA2	IO	8/8	-	
	-	2/5	OT	BALE	B28	A28			SA3	IO	8/8	-	
	-	-	-	NC			C19	D19	GND	PWR	-	-	
	-	2/5	OT	TC	B27	A27			SA4	IO	8/8	-	
	10K	2/5	IO	SD15			C18	D18	GND	PWR	-	-	
	-	2/5	O	DACK2#	B26	A26			SA5	IO	8/8	-	
	10K	5/2	IO	SD14			C17	D17	MASTER#	I		330R	2
	10K	/2	I	IRQ3	B25	A25			SA6	IO	8/8	-	
	10K	5/2	IO	SD13			C16	D16	VCC	PWR	-	-	
	10K	/2	I	IRQ4	B24	A24			SA7	IO	8/8	-	
	10K	5/2	IO	SD12			C15	D15	DRQ7	I	-	10K	
	10K	/2	I	IRQ5	B23	A23			SA8	IO	8/8	-	
	10K	5/2	IO	SD11			C14	D14	DACK7#	O	5/2	-	
	10K	/2	I	IRQ6	B22	A22			SA9	IO	8/8	-	
	10K	5/2	IO	SD10			C13	D13	DRQ6	I	-	10K	
	10K	/2	I	IRQ7	B21	A21			SA10	IO	8/8	-	
	10K	5/2	IO	SD9			C12	D12	DACK6#	O	5/2	-	
	-	5/2	O	SYSCLK	B20	A20			SA11	IO	8/8	-	
	10K	5/2	IO	SD8			C11	D11	DRQ5	I	-	10K	
1	330R		NC	REFRESH#	B19	A19			SA12	IO	8/8	-	
	10K	5/2	IO	MEMW#			C10	D10	DACK5#	O	5/2	-	
	10K	-	I	DRQ1	B18	A18			SA13	IO	8/8	-	
	10K	5/2	IO	MEMR#			C9	D9	DRQ0	I	-	10K	
	-	5/2	O	DACK1#	B17	A17			SA14	IO	8/8	-	
	-	5/2	IO	LA17			C8	D8	DACK0#	O	5/2	-	
	10K	-	I	DRQ3	B16	A16			SA15	IO	8/8	-	
	-	5/2	IO	LA18			C7	D7	IRQ14	I	-	10K	
	-	5/2	O	DACK3#	B15	A15			SA16	IO	5/2	-	
	-	5/2	IO	LA19			C6	D6	IRQ15	I	-	10K	
	10K	5/2	IO	IOR#	B14	A14			SA17	IO	5/2	-	
	-	5/2	IO	LA20			C5	D5	IRQ12	I	-	10K	
	10K	5/2	IO	IOW#	B13	A13			SA18	IO	2/5	-	
	-	5/2	IO	LA21			C4	D4	IRQ11	I	-	10K	
	10K	5/2	OT	SMEMR#	B12	A12			SA19	IO	5/2	-	
	-	5/2	IO	LA22			C3	D3	IRQ10	I	-	10K	
	10K	5/2	OT	SMEMW#	B11	A11			AEN	OT	5/2	-	
	-	5/2	IO	LA23			C2	D2	IOCS16#	IOC	5/2	330R	
	-	-	PWR	GND	B10	A10			IOCHRDY	IOC	-	1K	
	-	5/2	IO	SBHE#			C1	D1	MEMCS16#	IOC	/2	330R	
	-	-	PWR	+ 12 V	B9	A9			SD0	IO	5/2	10K	
	-	-	PWR	GND			C0	D0	GND	PWR	-	-	
	330R	-	IOC	OWS#	B8	A8			SD1	IO	5/2	10K	
	-	-	PWR	- 12 V	B7	A7			SD2	IO	5/2	10K	
	10K	-	I	DRQ2	B6	A6			SD3	IO	5/2	10K	
	-	-	PWR	- 5 V	B5	A5			SD4	IO	5/2	10K	
	10K	-	I	IRQ9	B4	A4			SD5	IO	5/2	10K	
	-	-	PWR	VCC	B3	A3			SD6	IO	5/2	10K	
	-	24/24	O	RESETDRV	B2	A2			SD7	IO	5/2	10K	
	-	-	PWR	GND	B1	A1			IOCHCHK#	IOC	-	1K	

5.17.2 PC-AT Edge Connector

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN C	PIN S	Signal	Type	Ioh/Iol	Pull U/D	Note
	1K	-	IOC	IOCHCHK#	A1	B1	GND	PWR	-	-	
	10K	5/2	IO	SD7	A2	B2	RESETDRV		24/24	-	
	10K	5/2	IO	SD6	A3	B3	VCC	PWR	-	-	
	10K	5/2	IO	SD5	A4	B4	IRQ9	I	-	10K	
	10K	5/2	IO	SD4	A5	B5	- 5 V	PWR	-	-	
	10K	5/2	IO	SD3	A6	B6	DRQ2	I	-	10K	
	10K	5/2	IO	SD2	A7	B7	- 12 V	PWR	-	-	
	10K	5/2	IO	SD1	A8	B8	OWS#	IOC	-	330R	
	10K	5/2	IO	SD0	A9	B9	+ 12 V	PWR	-	-	
	1K	-	IOC	IOCHRDY	A10	B10	GND	PWR	-	-	
	-	5/2	OT	AEN	A11	B11	SMEMW#	OT	5/2	10K	
	-	5/2	IO	SA19	A12	B12	SMEMR#	OT	5/2	10K	
	-	5/2	IO	SA18	A13	B13	IOW#	IO	5/2	10K	
	-	5/2	IO	SA17	A14	B14	IOR#	IO	5/2	10K	
	-	5/2	IO	SA16	A15	B15	DACK3#	O	5/2	-	
	-	8/8	IO	SA15	A16	B16	DRQ3	I	-	10K	
	-	8/8	IO	SA14	A17	B17	DACK1#	O	5/2	-	
	-	8/8	IO	SA13	A18	B18	DRQ1	I	-	10K	
	-	8/8	IO	SA12	A19	B19	REFRESH#	NC	-	330R	1
	-	8/8	IO	SA11	A20	B20	SYSCLK	O	5/2	-	
	-	8/8	IO	SA10	A21	B21	IRQ7	I	-	10K	
	-	8/8	IO	SA9	A22	B22	IRQ6	I	-	10K	
	-	8/8	IO	SA8	A23	B23	IRQ5	I	-	10K	
	-	8/8	IO	SA7	A24	B24	IRQ4	I	-	10K	
	-	8/8	IO	SA6	A25	B25	IRQ3	I	-	10K	
	-	8/8	IO	SA5	A26	B26	DACK2#	O	5/2	-	
	-	8/8	IO	SA4	A27	B27	TC	OT	5/2	-	
	-	8/8	IO	SA3	A28	B28	BALE	OT	5/2	-	
	-	8/8	IO	SA2	A29	B29	VCC	PWR	-	-	
	-	8/8	IO	SA1	A30	B30	OSC	O	8/8	-	
	-	8/8	IO	SA0	A31	B31	GND	PWR	-	-	
		COMPONENT SIDE			**C**	**S**	**SOLDER SIDE**				
	-	5/2	IO	SBHE#	C1	D1	MEMCS16#	IOC	-	330R	
	-	5/2	IO	LA23	C2	D2	IOCS16#	IOC	-	330R	
	-	5/2	IO	LA22	C3	D3	IRQ10	I	-	10K	
	-	5/2	IO	LA21	C4	D4	IRQ11	I	-	10K	
	-	5/2	IO	LA20	C5	D5	IRQ12	I	-	10K	
	-	5/2	IO	LA19	C6	D6	IRQ15	I	-	10K	
	-	5/2	IO	LA18	C7	D7	IRQ14	I	-	10K	
	-	5/2	IO	LA17	C8	D8	DACK0#	O	5/2	-	
	10K	5/2	IO	MEMR#	C9	D9	DRQ0	I	-	10K	
	10K	5/2	IO	MEMW#	C10	D10	DACK5#	O	5/2	-	
	10K	5/2	IO	SD8	C11	D11	DRQ5	I	-	10K	
	10K	5/2	IO	SD9	C12	D12	DACK6#	O	5/2	-	
	10K	5/2	IO	SD10	C13	D13	DRQ6	I	-	10K	
	10K	5/2	IO	SD11	C14	D14	DACK7#	O	5/2	-	
	10K	5/2	IO	SD12	C15	D15	DRQ7	I	-	10K	
	10K	5/2	IO	SD13	C16	D16	VCC	PWR	-	-	
	10K	5/2	IO	SD14	C17	D17	MASTER#	NC	-	330R	2
	10K	5/2	IO	SD15	C18	D18	GND	PWR	-	-	

1. Refresh is not supported.
2. Master mode is not supported.

5.17.3 ISA signal description

ADDRESS.

LA23..17	The address signals LA23..17 define the selection of a 128kB section of memory space within the 16MB address range of the 16 bit data bus. These signals are active high. The validity of the MEMCS16# depends on these signals only. These address lines are presented to the system with tri-state drivers. The permanent master drives these lines except when an alternate master cycle occurs; in this case the temporary master drives these lines. The LA signals are not defined for I/O accesses.
SA19..0	The address signals SA..0 define the selection with the granularity of one byte within the 1MB section of memory defined by the LA address lines. The address lines SA19..17 that are coincident with LA19..17 are defined to have the same value as LA19..17 for all memory cycles. These signals are active high. These address lines are presented to the system with tri-state drivers. The permanent master drives these lines except when an alternate master cycle occurs; in this case the temporary master drives these lines. SA7..0.
SBHE#	This signal is an active low signal, that indicates that a byte is being transferred on the upper byte (SD15..8) of the 16 bit bus. All bus masters will drive this line with a tri-state driver.

DATA.

SD15..8	These signals are defined for the high order byte of the 16 bit data bus. Memory or I/O transfers on this part of the bus are defined when SBHE# is active.
SD7..0	These signals are defined for the low order byte of the 16 bit data bus being the only bus for 8 bit PC-AT/PC104 adapter boards. Memory or I/O transfers on this part of the data bus are defined for 8 bit operations with even or odd addresses and for 16 bit operations for odd addresses only. The signals SA0 and SBHE# are used to define the data present on this bus as defined below:

SBHE#	SA0	SD15-SD8	SD7-SD0	Action
0	0	ODD	EVEN	Word transfer
0	1	ODD	ODD	Byte transfer on SD15-SD8
1	0	-	EVEN	Byte transfer on SD7-SD0
1	1	-	ODD	Byte transfer on SD7-SD0

COMMANDS.

BALE	This is an active high signal used to latch valid addresses from the current bus master on the falling edge of BALE. During DMA and alternate master cycles, BALE is forced high for the duration of the transfer. The permanent master drives BALE with a totem-pole driver.
IOR#	This is an active low signal driven by the current master to indicate an I/O read operation. I/O mapped devices using this strobe for selection should decode addresses SA15..0 and AEN. Additionally, DMA devices will use IOR# in conjunction with $DACK_n$# to decode a DMA transfer from the I/O device. The current bus master will drive this line with a tri-state driver.
IOW#	This is an active low signal driven by the current master to indicate an I/O write operation. I/O mapped devices using this strobe for selection should decode addresses SA15..0 and AEN. Additionally, DMA devices will use IOR# in conjunction with $DACK_n$# to decode a DMA transfer from the I/O device. The current bus master will drive this line with a tri-state driver.
SMEMR#	This is an active low signal driven by the permanent master to indicate a memory read operation in the first 1MB of system memory. Memory mapped devices using this strobe should decode addresses SA19..0 only. If an alternate master drives MEMR#, the permanent master will drive SMEMR# delayed by internal logic. The permanent master ties this line to VCC through a pull-up resistor to ensure that it is inactive during the exchange of bus masters.
SMEMW#	This is an active low signal driven by the permanent master to indicate a memory write operation in the first 1MB of system memory. Memory mapped devices using this strobe should decode addresses SA19..0 only. If an alternate master drives MEMR#, the permanent master will drive SMEMR# delayed by internal logic. The permanent master ties this line to VCC through a pull-up resistor to ensure that it is inactive during the exchange of bus masters.
MEMR#	This is an active low signal driven by the current master to indicate a memory read operation. Memory mapped devices using this strobe should decode addresses LA23..17 and SA19..0. All bus masters will drive this line with a tri-state driver. The permanent master ties this line to VCC through a pull-up resistor to ensure that it is inactive during the exchange of bus masters.
MEMW#	This is an active low signal driven by the current master to indicate a memory write operation. Memory mapped devices using this strobe should decode addresses LA23..17 and SA19..0. All bus masters will drive this line with a tri-state driver. The permanent master ties this line to VCC through a pull-up resistor to ensure that it is inactive during the exchange of bus masters.

TRANSFER RESPONSE.

IOCS16#	This is an active low signal driven by an I/O-mapped PC-AT/PC104 adapter indicating that the I/O device located at the address is a 16 bit device. This open collector signal is driven, based on SA15..0 only (not IOR# and IOW#) when AEN is not asserted.
MEMCS16#	This is an active low signal driven by a memory mapped PC-AT/PC104 adapter indicating that the memory device located at the address is a 16 bit device. This open collector signal is driven, based on LA23..17 only.
0WS#	This signal is an active low open-collector signal asserted by a 16 bit memory mapped device causing an early termination of the current transfer. It should be gated with MEMR# or MEMW# and is not valid during DMA transfers. IOCHRDY precedes 0WS#.
IOCHRDY	This is an active high signal driven inactive by the target of either a memory or an I/O operation to extend the current cycle. This open collector signal is driven based on the system address and the appropriate control strobe. IOCHRDY precedes 0WS#.
IOCHCK#	This is an active low signal driven active by a PC-AT/PC104 adapter detecting a fatal error during bus operation. When this open collector signal is driven low it will typically cause a SMI.

CONTROLS.

SYSCLK	This clock oscillates at 8.33MHz and is generated by the 5530.
OSC	This is a clock signal with a 14.31818 MHz ± 50 ppm frequency and a 50 ± 5% duty cycle. The signal is driven by the permanent master.
RESETDRV	This active high signal indicates that the adapter should be brought to an initial reset condition. This signal will be asserted by the permanent master on the bus for at least 100 ms at power-up or watchdog time-out to ensure that adapters in the system are properly reset. When active, all adapters should turn off or tri-state all drivers connected to the bus.

INTERRUPTS.

IRQ3..7, IRQ9..12, IRQ14..15	These signals are active high signals, which indicate the presence of an interrupting PC-AT/PC104 bus adapter. Unused interrupts should be masked.

BUS ARBITRATION.

DRQ0..3, DRQ5..7	These signals are active high signals driven by a DMA bus adapter to indicate a request for a DMA bus operation. DRQ0..3 request 8 bit DMA operations, while DRQ5..DRQ7 request 16 bit operations. All bus DMA adapters will drive these lines with a tri-state driver. The permanent master monitors these signals to determine which of the DMA devices, if any are requesting the bus.
DACK0#..3#, DACK5#..7#	These signals are active low signals driven by the permanent master to indicate that a DMA operation can begin. They are continuously driven by a totem pole driver for DMA channels attached.
AEN	This signal is an active high totem pole signal driven by the permanent master to indicate that the DMA controller drives the address lines. The assertion of AEN disables response to I/O port addresses when I/O command strobes are asserted. AEN being asserted, only the device with active $DACK_n$# should respond.
REFRESH#	This is an active low signal driven by the current master to indicate a memory refresh operation. Refresh is not supported.
TC	This active high signal is asserted during a read or write command indicating that the DMA controller has reached a terminal count for the current transfer. $DACK_n$# must be presented by the bus adapter to validate the TC signal.
MASTER#	ISA Bus-mastering is not supported

5.18 PC104+ PCI connector

5.18.1 PC104+ PCI Connector

The PC104+ connector provides a complete PCI interface with multiple copies of selected signals for up to 4 PC104+ boards to be used. Three of these boards may utilise the PCI bus mastering capability.
The 3.3V supply in the connector is only for low power boards. The total 3.3V current draw from the board should not exceed 1A at any time. This current draw includes current draw from the panel connector (JPLCD). External PCI component must be designed to work in a 3.3V signaling environment as defined in [2] and [5] (Universal board).
On the GX1LCD/S board Pin A1 is closest to the CS5530A chipset. On the GX1LCD/3.5" board Pin A1 is closest to the PWRCON connector.

Pin	A	B	C	D
1	GND	Reserved	+5V	AD00
2	+5V	AD02	AD01	+5V
3	AD05	GND	AD04	AD03
4	C/BE0	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	+5V	AD10	GND
7	AD14	AD13	GND	AD12
8	+3.3V	C/BE1	AD15	+3.3V
9	SERR	GND	SB0	PAR
10	GND	PERR	+3.3V	SDONE
11	STOP	+3.3V	LOCK	GND
12	+3.3V	TRDY	GND	DEVSEL
13	FRAME	GND	IRDY	+3.3V
14	GND	AD16	+3.3V	C/BE2
15	AD18	+3.3V	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3V	AD23	AD22	+3.3V
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C/BE3	VI/O	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5V	AD28	AD27
22	+5V	AD30	GND	AD31
23	REQ0	GND	REQ1	VI/O
24	GND	REQ2	+5V	GNT0
25	GNT1	VI/O	GNT2	GND
26	+5V	CLK0	GND	CLK1
27	CLK2*	+5V	CLK3*	GND
28	GND	INTD	+5V	RST
29	+12V	INTA	INTB	INTC
30	-12V	Reserved	Reserved	GND

* Clk2 and Clk3 share the same clock driver pin.
For a detailed description of PCI bus transactions, refer to [5].

5.18.2 Signal Description – PC104+ Connector

SYSTEM PINS.

CLK	Clock provides timing for all transactions on PCI and is an input to every PCI device. All other PCI signals, except RST#, INTA#, INTB#, INTC#, and INTD#, are sampled on the rising edge of CLK and all other timing parameters are defined with respect to this edge. PCI operates at 33 MHz.
RST#	Reset is used to bring PCI-specific registers, sequencers, and signals to a consistent state. What effect RST# has on a device beyond the PCI sequencer is beyond the scope of this specification, except for reset states of required PCI configuration registers. Anytime RST# is asserted, all PCI output signals must be driven to their benign state. In general, this means they must be asynchronously tri-stated. SERR# (open drain) is floated. REQ# and GNT# must both be tri-stated (they cannot be driven low or high during reset). To prevent AD, C/BE#, and PAR signals from floating during reset, the central resource may drive these lines during reset (bus parking) but only to a logic low level–they may not be driven high. RST# may be asynchronous to CLK when asserted or deasserted. Although asynchronous, deassertion is guaranteed to be a clean, bounce-free edge. Except for configuration accesses, only devices that are required to boot the system will respond after reset.

ADDRESS AND DATA.

AD[31::00]	Address and Data are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. PCI supports both read and write bursts. The address phase is the clock cycle in which FRAME# is asserted. During the address phase AD[31::00] contain a physical address (32 bits). For I/O, this is a byte address; for configuration and memory, it is a DWORD address. During data phases AD[07::00] contain the least significant byte (lsb) and AD[31::24] contain the most significant byte (msb). Write data is stable and valid when IRDY# is asserted and read data is stable and valid when TRDY# is asserted. Data is transferred during those clocks where both IRDY# and TRDY# are asserted.
C/BE[3::0]#	Bus Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3::0]# define the bus command. During the data phase C/BE[3::0]# are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. C/BE[0]# applies to byte 0 (lsb) and C/BE[3]# applies to byte 3 (msb).
PAR	Parity is even parity across AD[31::00] and C/BE[3::0]#. Parity generation is required by all PCI agents. PAR is stable and valid one clock after the address phase. For data phases, PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. (PAR has the same timing as AD[31::00], but it is delayed by one clock.) The master drives PAR for address and write data phases; the target drives PAR for read data phases.

INTERFACE CONTROL PINS.

FRAME#	Cycle Frame is driven by the current master to indicate the beginning and duration of an access. FRAME# is asserted to indicate a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is deasserted, the transaction is in the final data phase or has completed.
IRDY#	Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates that valid data is present on AD[31::00]. During a read, it indicates the master is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
TRDY#	Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed on any clock both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that valid data is present on AD[31::00]. During a write, it indicates the target is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
STOP#	Stop indicates the current target is requesting the master to stop the current transaction.
LOCK#	Lock indicates an atomic operation that may require multiple transactions to complete. When LOCK# is asserted, non-exclusive transactions may proceed to an address that is not currently locked. A grant to start a transaction on PCI does not guarantee control of LOCK#. Control of LOCK# is obtained under its own protocol in conjunction with GNT#. It is possible for different agents to use PCI while a single master retains ownership of LOCK#. If a device implements Executable Memory, it should also implement LOCK# and guarantee complete access exclusion in that memory. A target of an access that supports LOCK# must provide exclusion to a minimum of 16 bytes (aligned). Host bridges that have system memory behind them should implement LOCK# as a target from the PCI bus point of view and optionally as a master.
IDSEL	Initialization Device Select is used as a chip select during configuration read and write transactions.
DEVSEL#	Device Select, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.

ARBITRATION PINS (BUS MASTERS ONLY).

REQ#	Request indicates to the arbiter that this agent desires use of the bus. This is a point to point signal. Every master has its own REQ# which must be tri-stated while RST# is asserted.
GNT#	Grant indicates to the agent that access to the bus has been granted. This is a point to point signal. Every master has its own GNT# which must be ignored while RST# is asserted.

While RST# is asserted, the arbiter must ignore all REQ# lines since they are tri-stated and do not contain a valid request. The arbiter can only perform arbitration after RST# is deasserted. A master must ignore its GNT# while RST# is asserted. REQ# and GNT# are tri-state signals due to power sequencing requirements when 3.3V or 5.0V only add-in boards are used with add-in boards that use a universal I/O buffer.

ERROR REPORTING PINS.

The error reporting pins are required by all devices and maybe asserted when enabled:

PERR#	Parity Error is only for the reporting of data parity errors during all PCI transactions except a Special Cycle. The PERR# pin is sustained tri-state and must be driven active by the agent receiving data two clocks following the data when a data parity error is detected. The minimum duration of PERR# is one clock for each data phase that a data parity error is detected. (If sequential data phases each have a data parity error, the PERR# signal will be asserted for more than a single clock.) PERR# must be driven high for one clock before being tri-stated as with all sustained tri-state signals. There are no special conditions when a data parity error may be lost or when reporting of an error may be delayed. An agent cannot report a PERR# until it has claimed the access by asserting DEVSEL# (for a target) and completed a data phase or is the master of the current transaction.
SERR#	System Error is for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic. If an agent does not want a non-maskable interrupt (NMI) to be generated, a different reporting mechanism is required. SERR# is pure open drain and is actively driven for a single PCI clock by the agent reporting the error. The assertion of SERR# is synchronous to the clock and meets the setup and hold times of all bused signals. However, the restoring of SERR# to the deasserted state is accomplished by a weak pullup (same value as used for s/t/s) which is provided by the system designer and not by the signaling agent or central resource. This pull-up may take two to three clock periods to fully restore SERR#. The agent that reports SERR#s to the operating system does so anytime SERR# is sampled asserted.

INTERRUPT PINS (OPTIONAL).

Interrupts on PCI are optional and defined as "level sensitive," asserted low (negative true), using open drain output drivers. The assertion and deassertion of INTx# is asynchronous to CLK. A device asserts its INTx# line when requesting attention from its device driver. Once the INTx# signal is asserted, it remains asserted until the device driver clears the pending request. When the request is cleared, the device deasserts its INTx# signal. PCI defines one interrupt line for a single function device and up to four interrupt lines for a multi-function device or connector. For a single function device, only INTA# may be used while the other three interrupt lines have no meaning.

INTA#	Interrupt A is used to request an interrupt.
INTB#	Interrupt B is used to request an interrupt and only has meaning on a multi-function device.
INTC#	Interrupt C is used to request an interrupt and only has meaning on a multi-function device.
INTD#	Interrupt D is used to request an interrupt and only has meaning on a multi-function device.

Since most devices are single function and, therefore, can only use INTA# on the device, the interrupts are distributed evenly among the interrupt controller’s input pins. For the device in the PCI slot to function, the routing in the slots has to follow the specifications as outlined in the PC/104+ Specification Version 1.0 February 1997.

The table below specifies the distribution for the four modules that can be plugged on the PC104+ Connector. Note that AD20-23 are used for IDSEL for the individual boards.

Module Slot	REQ*	GNT*	CLK	IDSEL	ID Address	INT0*	INT1*	INT2*	INT3*
1	REQ0*	GNT0*	CLK0	IDSEL0	AD20	INTA*	INTD*	INTC*	INTB*
2	REQ1*	GNT1*	CLK1	IDSEL1	AD21	INTB*	INTA*	INTD*	INTC*
3	REQ2*[1]	GNT2*[1]	CLK2	IDSEL2	AD22	INTC*	INTB*	INTA*	INTD*
4	REQ2*[1]	GNT2*[1]	CLK3	IDSEL3	AD23	INTD*	INTC*	INTB*	INTA*

Note 1: Because module slots 3 and 4 share REQ2/GNT2, they cannot both be bus master devices.

6. Mating Connector List

Below is a list of the internal mounted and the mating connectors for the GX1LCD board.

Connector (Reference)	Connector Vendor / Part-number	Mating Connector Vendor / Part-number
GX1LCD/S PWR Connector (PWRCON)	Molex / 39-29-0063	Molex 5557 / 39-01-2060 Molex 5556 / 39-00-0056
GX1LCD/3.5" PWR Connector (PWRCON)	Molex / 43045-0801	Molex 43025-0800 Molex 43030-0002
Keyboard / PS/2 Pinrows (JPKBD, JPMSE)	Molex / 22-29-2051	Molex 6471 / 22-01-2055 Molex 4809 / 08-55-0110
Flat Panel Connector (PANEL)	Molex / 70246- 5021	Leoco / 2540S 50UB1 Leoco / 2540S 50SRB1
Panel Link (PNLLINK)	3M / 10226- 6212VC	3M / 10126-6000EC 3M / 10326-A200-00
GX1LCD/S Floppy (FLOPPY)	Molex / 70246- 3421	Leoco / 2540S 34UB1 Leoco / 2540S 34SRB1
GX1LCD/3.5" Floppy (FLOPPY)	Molex / 87331-3420	Leoco / 2066S-34-0000 34 x Leoco / 2065TPB0000
Primary IDE Channel (IDE1)	Molex / 70246- 4021	Leoco / 2540S 40UB1 Leoco / 2540S 40SRB1
GX1LCD/3.5" Secondary IDE Channel (IDE2)	Molex / 87331-4420	AMP / 1-111623-0
GX1LCD/S Printer Port (PRINTER)	Molex / 70246- 2621	Leoco / 2540S 26UB1 Leoco / 2540S 26SRB1
GX1LCD/3.5" Printer Port (PRINTER)	Molex / 87331-2620	Molex / 51110-2651 26 x Molex / 50394-8052
GX1LCD/S Serial Port 2 Header (COM2, 3, 4)	Molex / 70246- 1021	Leoco / 2540S 10UB1 Leoco / 2540S 10SRB1
GX1LCD/3.5" Serial Port 2 Header (COM2)	Molex / 87331-1020	Molex / 51110-1060 10 x Molex / 50394-8052
GX1LCD/S USB Connector (USB)	Molex / 10- 96- 7085	Leoco / 2655S 8 0000 Leoco / 2653TPBU002
Fan Connector (FAN)	Molex / 22- 29- 2031	Leoco / 2530S030013 Leoco / 2533TCBU000
GX1LCD/S Audio and IrDA (JPAUX)	Molex / 10- 96- 7205	Etec / BE2-020-S131-11*
GX1LCD/S CDROM Connector (CDROM)	Leoco / 2011P04V000	Leoco / 2010S040000 Leoco / 2033TPB0000

GX1LCD/S Feature Port (FEATURE)	Molex / 70246- 2021	Leoco / 2540S 20UB1 Leoco / 2540S 20SRB1
GX1LCD/3.5” Feature Port (FEATURE)	Molex / 87331-2020	Molex / 51110-2051 20 x Molex / 50394-8052
PC104 (PC104XT, PC104AT)	Samtec / ESW-132-12-G-D Samtec / ESW-120-12-G-D	Samtec / ESW-132-44-G-D* Samtec / ESW-120-44-G-D*
PC104+ PCI Connector	Samtec / ESQT-130-03-M-Q-368	*
Bracket spacer (BRACK1, BRACK2)	Molex / 87331-3020	Samtec / SQT-115-02-L-D*

* Exact Part-number will depend on the specific application.

7. Warranty

Kontron Technology warrants its products to be free from defects in material and workmanship during the warranty period. If a product proves to be defective in material or workmanship during the warranty period, Kontron Technology will, at its sole option, repair or replace the product with a similar product.
Replacement Product or parts may include remanufactured or refurbished parts or components.

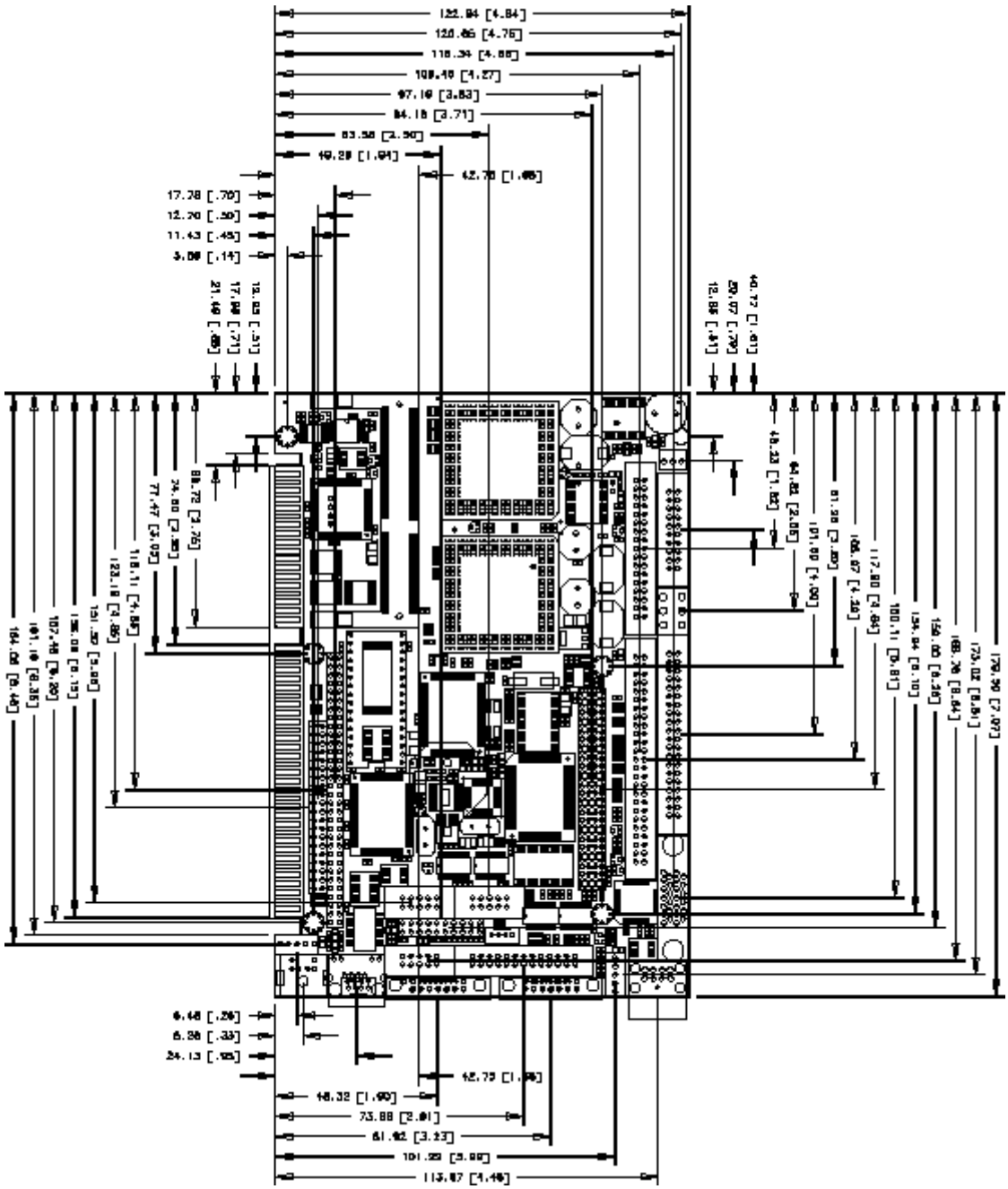
The warranty does not cover:

1. Damage, deterioration or malfunction resulting from:
   A. Accident, misuse, neglect, fire, water, lightning, or other acts of nature, unauthorised product modification, or failure to follow instructions supplied with the product.
   B. Repair or attempted repair by anyone not authorised by Kontron Technology.
   C. Causes external to the product, such as electric power fluctuations or failure.
   D. Normal wear and tear.
   E. Any other causes which does not relate to a product defect.
2. Removal, installation, and set-up service charges.

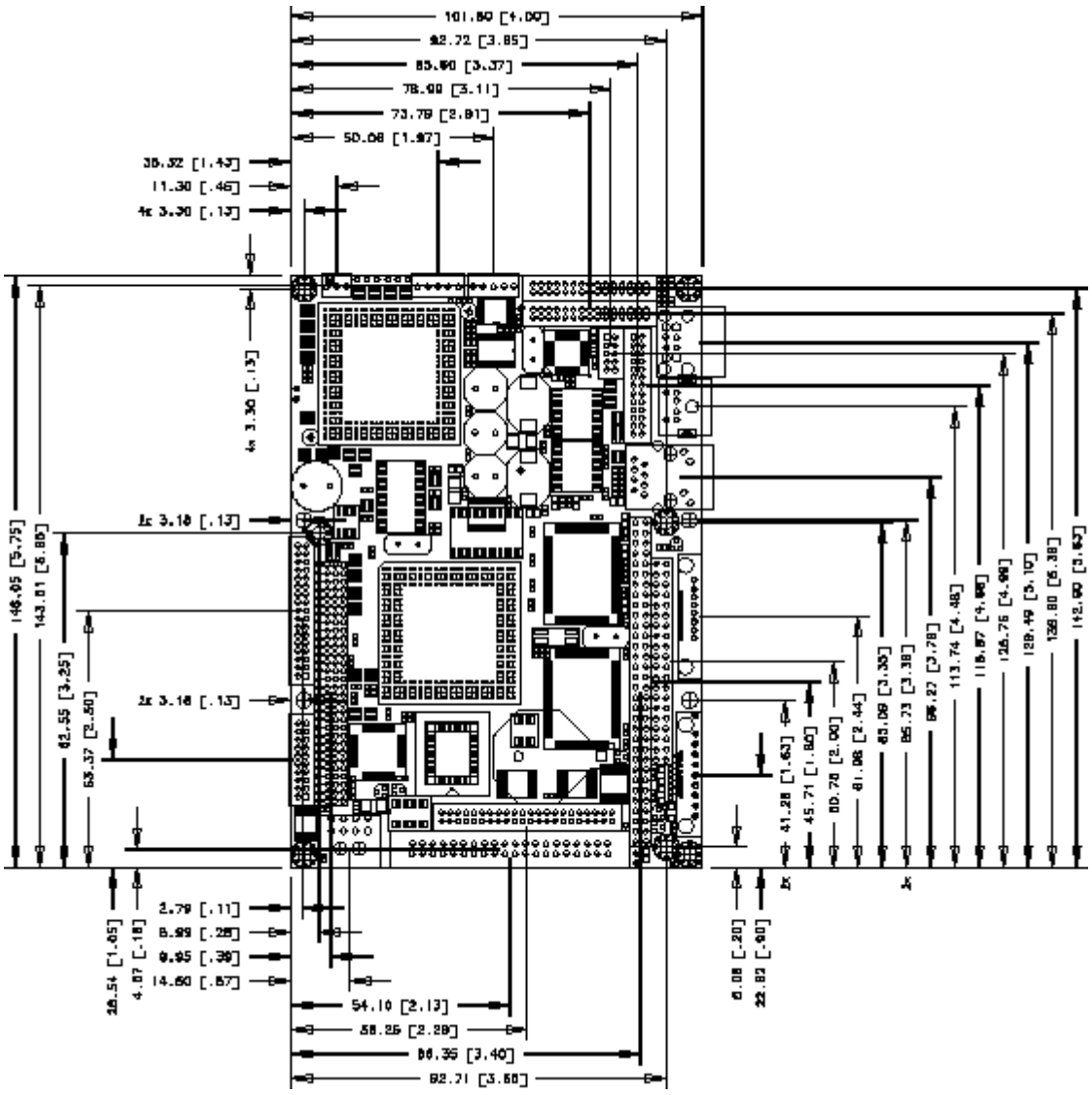
Exclusion of damages:

KONTRON TECHNOLOGY LIABILITY IS LIMITED TO THE COST OF REPAIR OR REPLACEMENT OF THE PRODUCT. KONTRON TECHNOLOGY SHALL NOT BE LIABLE FOR:
1. DAMAGE TO OTHER PROPERTY CAUSED BY ANY DEFECTS IN THE PRODUCT, DAMAGES BASED UPON INCONVENIENCE, LOSS OF USE OF THE PRODUCT, LOSS OF TIME, LOSS OF PROFITS, LOSS OF BUSINESS OPPORTUNITY, LOSS OF GOODWILL, INTERFERENCE WITH BUSINESS RELATIONSHIPS, OR OTHER COMMERCIAL LOSS, EVEN IF ADVISED OF THEIR POSSIBILITY OF SUCH DAMAGES.
2. ANY OTHER DAMAGES, WHETHER INCIDENTAL, CONSEQUENTIAL OR OTHERWISE.
3. ANY CLAIM AGAINST THE CUSTOMER BY ANY OTHER PARTY.

8. Measurement Drawing (GX1LCD/S)



9. Measurement Drawing (GX1LCD/3.5”)



References

[1] IEEE Personal Computer BUS Standard P996. Draft D2.02 13. July 1990. This standard is an attempt to standardise the ISA bus introduced by IBM. The draft has not been approved, but is however the *official* ISA bus specification.

[2] PC/104-*Plus* Specification version 1.0 February 1997

[3] IEEE std. 1284-1996: Standard signalling method for a Bidirectional Parallel Peripheral Interface for Personal Computers. December 2. 1994.

[4] ATA-4 specification.

[5] PCI Local Bus Specification. Revision 2.1 June 1. 1995. PCI Special interests group.
[6] IEEE std. 802.3, 1998 Edition.

Additional details about specific functions or components of the board refer to the components datasheet or contact Kontron Technology support line.