» User Guide «

SMARC sAT30 User Guide

Document revision 1.0

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1 User Information

1.1 About This Document

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2 Introduction

The SMARC® (Ultra Low Power – Computer on Module) sAT30 is a versatile small form factor Computer-On-Module that requires low power and provides high performance at low cost. The module connector has 314 edge fingers that mate with a low profile 314 pin 0.5mm pitch right angle connector (this connector is sometimes identified as an 321 pin connector, but 7 pins are lost to the key).

Featuring NVIDIA's Tegra T30 System-on-Chip, Kontron's SMARC sAT30 offers LVDS, Parallel LCD, HDMI Display, Gigabit Ethernet, PCIe, SATA, USB, USB OTG, Camera support and superior graphics performance in a cost effective, low power, miniature package. Kontron's SMARC sAT30 thin and robust design makes it an ideal building block for reliable system design.

Caution! The SMARC sAT30 module is ESD sensitive equipment. Users must observe precautions for handling electrostatic discharge sensitive devices.

2.1 Feature Set Overview

- SMARC compliant in an 82mm x 50mm form factor.
- NVIDIA Tegra 3 quad-core ARM Cortex A9 SoC
  - Up to 1.3GHz operation (Quad core operation, restricted temperature range).
  - Up to 1.2 GHz operation (Quad core, over 0 – 60 °C temp range, with appropriate heat sink).
  - Up to 1.4 GHz operation (Single core mode).
- Up to 2GB of DDR3 SDRAM support.
- On-board NAND flash (eMMC) support up to 64GB.
- On-board Intel I210 (Springville) GbE controller.
- Single channel 18bit LVDS display support (24 bit / 18 bit compatible as well).
- 24 bit parallel LCD display support.
- HDMI output.
- 1.8V Module I/O support.
- GPIO support.
- SDIO support.
- I2S support.
- I2C support.
- Two Serial Camera interfaces (CSI).
- Two PCIe ports.
- USB and USB (On-The-Go®) OTG support.
- Watch Dog Timer (WDT) support.
- UART support.
- SATA support.

2.2 Software Support / Hardware Abstraction

The Kontron sAT30 Module is supported by Kontron BSPs (Board Support Package). The first sAT30 BSP targets Linux support and is available under Kontron part number 771-242-00. BSPs for other operating systems are planned. Check with your Kontron contact for the latest BSPs.

This manual goes into a lot of detail on I/O particulars – information is provided on exactly how the various SMARC edge fingers tie into the NVIDIA SoC and to other Module hardware. This is provided for reference and context. Most of the I/O particulars are covered and abstracted in the BSP and it should generally not be necessary for sAT30 users to deal with I/O at the register level.

2.3 Document and Standards References

2.3.1 External Industry Standard Documents

- ***CSI-2 (Camera Serial Interface version 2)*** The CSI-2 standard is owned and maintained by the MIPI Alliance (Mobile Industry Processor Alliance) (www.mipi.org).
- ***D-PHY*** CSI-2 physical layer standard – owned and maintained by the MIPI Alliance (www.mipi.org).
- ***eMMC (Embedded Multi-Media Card)*** the eMMC electrical standard is defined by JEDEC JESD84-B45 and the mechanical standard by JESD84-C44 (www.jedec.org).
- ***GbE MDI (Gigabit Ethernet Medium Dependent Interface)*** defined by IEEE 802.3. The 1000Base-T operation over copper twisted pair cabling is defined by IEEE 802.3ab (www.ieee.org).
- ***HDMI Specification***, Version 1.3a, November 10, 2006 © 2006 Hitachi and other companies (www.hdmi.org).
- ***The I2C Specification,*** Version 2.1, January 2000, Philips Semiconductor (now NXP) (www.nxp.com).
- ***I2S Bus Specification,*** Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) (www.nxp.com).
- ***JTAG (Joint Test Action Group)*** defined by IEEE 1149.1-2001 - IEEE Standard Test Access Port and Boundary Scan Architecture (www.ieee.org).
- ***MXM3 Graphics Module Mobile PCI Express Module Electromechanical Specification,*** Version 3.0, Revision 1.1, © 2009 NVIDIA Corporation (www.mxm-sig.org).
- ***PICMG® EEEP Embedded EEPROM Specification,*** Rev. 1.0, August 2010 (www.picmg.org).
- ***PCI Express Specifications*** (www.pci-sig.org).
- ***Serial ATA Revision 3.1***, July 18, 2011, Gold Revision, © Serial ATA International Organization (www.sata-io.org).
- ***SD Specifications Part 1 Physical Layer Simplified Specification,*** Version 3.01, May 18, 2010, © 2010 SD Group and SD Card Association (Secure Digital) (www.sdcard.org).
- ***SPDIF*** (aka S/PDIF) (Sony Philips Digital Interface) - IEC 60958-3.
- ***SPI Bus*** – "Serial Peripheral Interface" – de-facto serial interface standard defined by Motorola. A good description may be found on Wikipedia (http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus).
- ***USB Specifications*** (www.usb.org).

2.3.2 Kontron Documents

- ***Ultra Low Power – Computer On Module Hardware Specification***, version 1.2, September 19, 2012. © Kontron 2012.
- ***Ultra Low Power – Computer On Module "Evaluation Carrier" User Manual***, Version 1.0, September 10, 2012. © Kontron 2012.
- ***Ultra Low Power – Computer On Module "Evaluation Carrier" Quick Start Manual***, Version 1.0, September 10, 2012. © Kontron 2012.

2.3.3 Kontron Schematics

The following schematic numbers are listed for reference. The Module schematic is not usually available outside of Kontron, without special permission. The other schematics may be available, under NDA or otherwise. Contact your Kontron representative for more information. The SMARC Evaluation Carrier schematic is particularly useful as an example of the implementation of various interfaces on a Carrier board.

- ***sAT30 Module***, KAI 501-141, latest revision.
- ***SMARC Evaluation Carrier (KARMA Eval Carrier)*** Board Schematic, KAI 501-146, latest revision.
- ***eMMC Mezzanine*** Schematic, KAI 501-151, latest revision.
- ***KLAS*** Schematic, Hyundai 1366 x 768 Single Ch. LVDS, KAI 501-162, latest revision.
- ***KLAS*** Schematic, NEC 1280 x 768 Single Ch. LVDS, KAI 501-163, latest revision.
- ***KLAS*** Schematic, Dual Channel LVDS 40 pin VESA Standard, KAI 501-165, latest revision.

2.3.4 NVIDIA Hardware Documents

- ***NVIDIA T30 Design Guidelines*** DG-05576-001_v10, Version 10, March 06, 2012.
- ***NVIDIA T30 Datasheet*** DS-05160-001_v04, Version 4.0, January 31, 2012.

2.3.5 NVIDIA Software Documents

- ***NVIDIA T30 Technical Reference manual*** DP-05644-001_v03, Version 0.3, November 25, 2011
- ***Tegra Linux Driver Package Developers Guide*** PG_06076-R15, Version R15, June 11, 2012 (Contained in Tegra_Linux_Driver_Package_Documents_R15.tar)
- ***Tegra Linux Driver Package Software Features*** DA-06018-R15, Version R15, June 11, 2012 (Contained in Tegra_Linux_Driver_Package_Documents_R15.tar).
- ***Tegra_Linux_Driver_Package_Release_Notes_R15*** RN_05071-R15, Version R15, June 11, 2012.

2.3.6 Kontron Software BSP

- ***Kontron BSP for SMARC sAT30 Module*** - Kontron part number 771-242-00.

3 Specifications

3.1 Functional Block Diagram

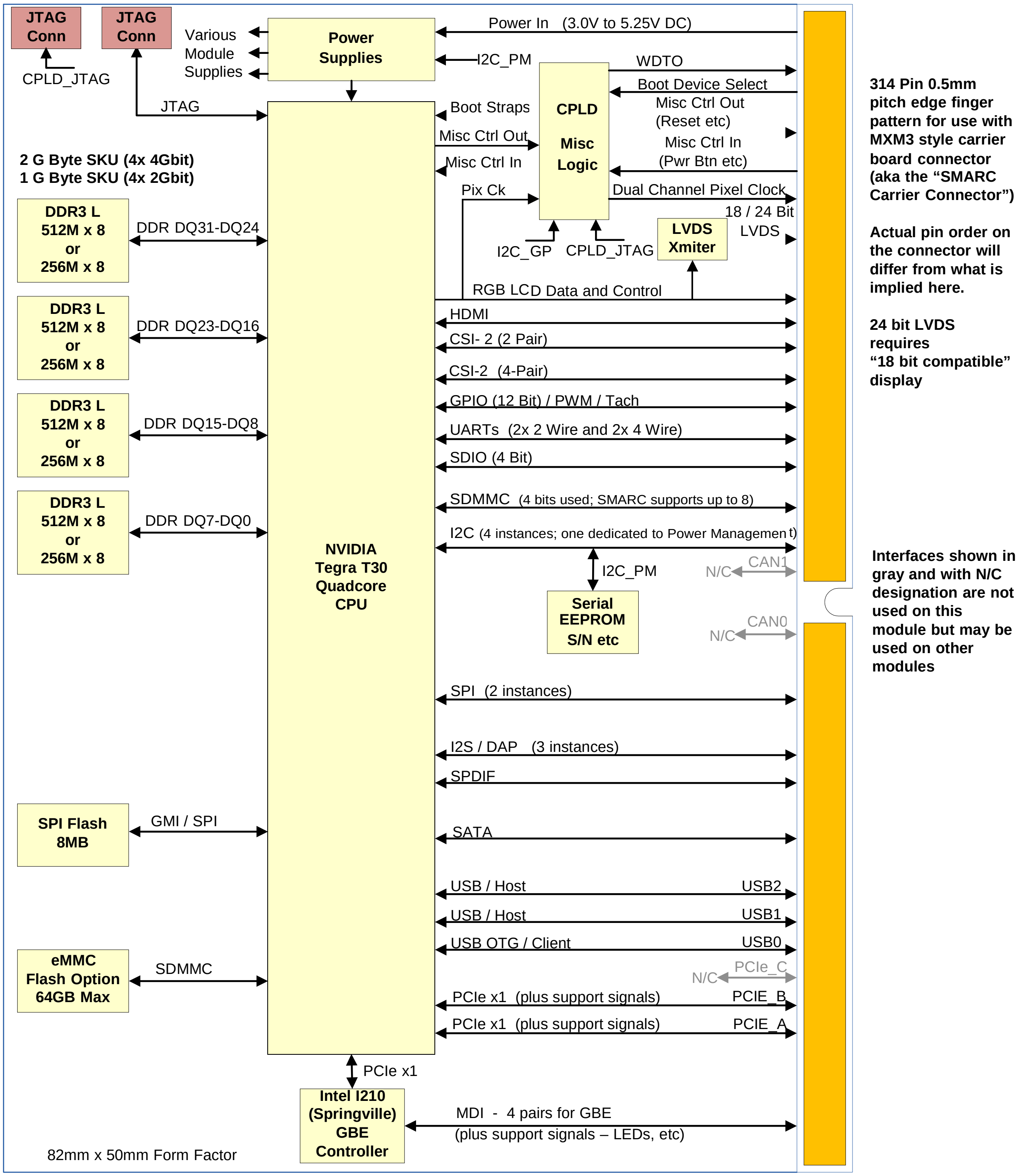

Figure 1: SMARC sAT30 Block Diagram

3.2 SMARC sAT30 General Functions

This section lists the complete feature set supported by the SMARC sAT30 module.

3.2.1 SMARC sAT30 Feature Set

The following table summarizes the SMARC features implemented on the sAT30, vs. the maximum possible allowed in the SMARC specification. All mandatory features required by the SMARC specification are implemented in the sAT30 Module.

SMARC Feature specification	SMARC Specification Maximum Number Possible	SMARC sAT30 Feature support	SMARC sAT30 Feature support instances
LVDS Display support	1	Yes	1
Parallel LCD support	1	Yes	1
HDMI Display support	1	Yes	1
CSI Camera support (Dual and Quad lanes)	2	Yes	2 (Both support dual lane only; Quad lane is not supported)
Parallel Camera support	2	No	0
USB Interface	3	Yes	3
PCIe Interface	3	Yes	2
SATA Interface	1	Yes	1
GbE Interface	1	Yes	1
SDIO Interface	1	Yes	1
SDMMC Interface	1	Yes (4-bit is used)	1
SPI Interface	2	Yes	2
I2S Interface	3	Yes	3
I2C Interface	5	Yes	5
CAN	2	No	0
AFB	1	No	0
I/O Voltage (1.8V) level support		Yes	
I/O Voltage (3.3V) level support		No	

3.2.2 Form Factor

The SMARC sAT30 module complies with the SMARC General Specification module size requirements in an 82mm x 50mm form factor.

3.2.3 CPU

The SMARC sAT30 module implements NVIDIA's Tegra T30 quad-core ARM processor:

» 40nm Tegra T30 Cortex A9 Quad core.

» Up to 1.2 GHz (Quad core mode, over 0-60 ^{0}C operating temperature range, with heatsink).

» Up to 1.3 GHz (Quad core mode, restricted temperature range).

» Up to 1.4 GHz (Single core mode).

» 1 Cache -32 KB Instruction cache (I-Cache) and 32 KB Data cache (D-Cache) per core L2 Cache controller configured with 1MByte of cache RAM.

» Power optimized companion CPU core MSelect Data Routing Module Programmable clock generator for power and performance tuning.

» 24.5 x 24.5 mm package.

» Allowable CPU junction temperature range: -25 ^{0}C to 90 ^{0}C

NVIDIA graphics support, GeForce Graphics Processor:

» HDTV capable.

» Video Decode Processor supported standards - H.264, VC-1, MPEG4, H.263, DiVX, XviD and MPEG-2.

» Video Encode Processor supported standards - H.264, MPEG4, H.263 and JPEG.

» OpenGL ES 2.0.

» Dual display pipelines.

3.2.4 Module Memory

The SMARC sAT30 module supports 1GB and 2GB total DDR3L memory, through two separate orderable SKU's:

» **51001-1016-12-4** 1GB DDR3LV Dram; 16 GB eMMC Flash; 1.2 GHz Quadcore Commercial Grade T30 SoC

» **51001-2016-12-4** 2GB DDR3LV Dram; 16 GB eMMC Flash; 1.2 GHz Quadcore Commercial Grade T30 SoC

Additional SKUs may become available. SKU variations would include alternative eMMC options, including possibly no on-Module eMMC. Check with your Kontron contact or on the Kontron web site for updated information.

3.2.5 On-board Storage

The SMARC sAT30 module supports an 8MB SPI flash memory device. The module also supports an eMMC flash option up to 64GB. The standard SKUs support 16 GB eMMC flash.

3.2.6 Clocks

A 32.768 KHz clock is required for the Tegra T30 CPU RTC (Real Time Clock) and PMC (Power Management Controller). This clock is provided by Power Management Unit (PMU).

The Tegra T30 CPU is provided with a 12 MHz clock using a crystal in normal oscillation mode (On-chip Oscillator).

3.2.7 LVDS Serialized LCD Display Interface

LVDS LCD operation is not native to the NVIDIA Tegra SoC. The Module LVDS output is created on the Module from the Tegra 24 bit LCD parallel data path. This is evident in the block diagram above (**Figure 1: SMARC sAT30 Block Diagram**). The LVDS color packing used on the Module is in the "18 bit color compatible mode" (more details on this can be found later in this section and in the ***Ultra Low Power – Computer On Module Hardware Specification***). The display connection may be 18 bit or 24 bit, but if a 24 bit connection is used, then the display must be capable of accepting an "18 bit color packing". This is sometimes alternatively referred to as "6 bit pack" (it's 6 bits per color, or 18 bits total …). For single channel LVDS, a display resolution up to approximately 1280 x 1024 may be supported (approximate" because factors such as Carrier Board trace lengths, routing quality, cable length and quality, Carrier EMI and ESD suppression device selections and display timing particulars can affect the maximum resolution achieved). For high resolution displays (1280 x 1024 and higher), a Carrier Board based dual channel LVDS transmitter operating from the Module parallel data path should be used instead. This is described in a later section.

For flat panel use, parallel LCD data and control information (Red, Green and Blue color data, Display Enable, Vertical Synch and Horizontal Synch) are serialized onto a set of LVDS differential pairs. The information is packed into frames that are 7 bits long. For 18 bit color depths, the data and control information utilize three LVDS channels (18 data bits + 3 control bits = 21 bits; hence 3 channels with 7 bit frames) plus a clock pair. For 24 bit color depths, four LVDS channels are used (24 data bits + 3 control bits + 1 unused bit = 28 bits, or 4 x 7) plus a clock pair. The LVDS clock is transmitted on a separate LVDS pair. The LVDS clock period is 7 times longer than the pixel clock period. The LVDS clock edges are off from the 7 bit frame boundaries by 2 pixel periods. Unfortunately, there are two different 24 bit color mappings in use. The more common one, sometimes referred to as "24 bit standard color mapping" is not compatible with 18 bit panels, as it places the most significant RGB color data on the 4th LVDS data pair – the pair that is not used on 18 bit panels. There is a less common "24 bit / 18 bit compatible" mapping that puts the least significant color bits of the 24 bit set onto the 4th LVDS pair and allows 24 bit color depths.

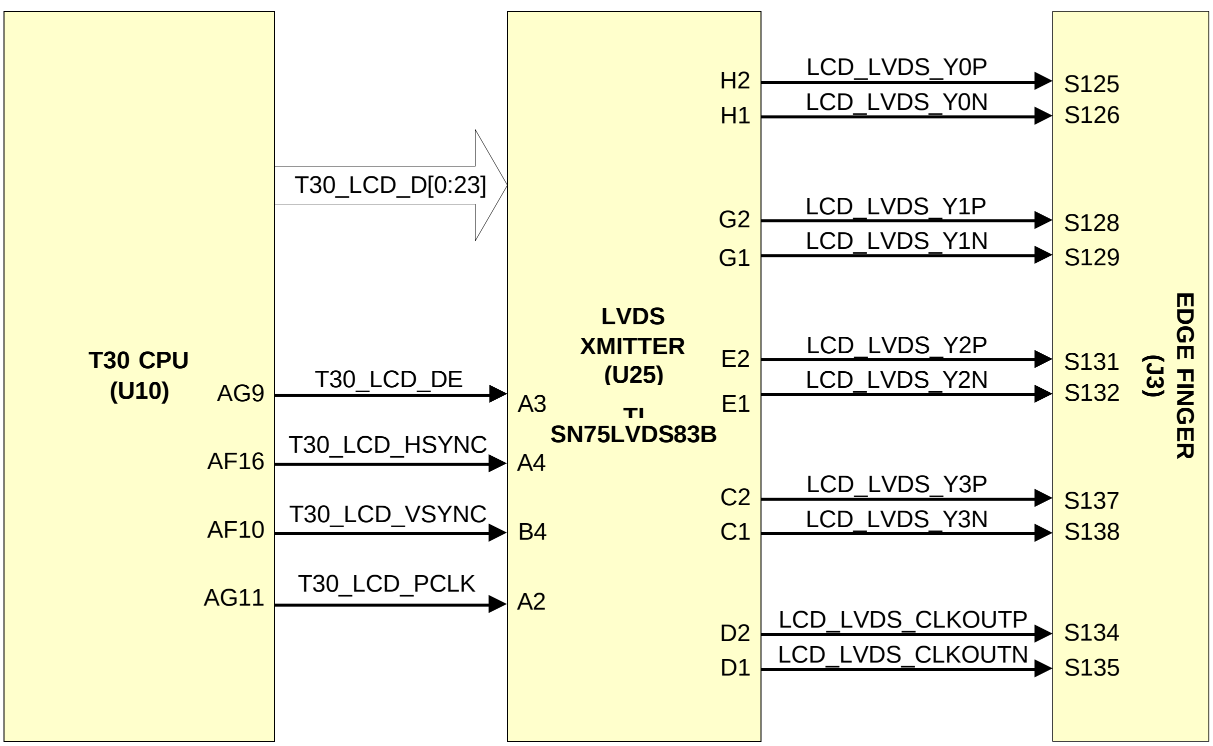

Figure 2: T30 Module LVDS LCD Implementation

The following table details exactly how the NVIDIA Tegra parallel LCD pins are mapped to the on-Module Texas Instruments SN75LVDS83B LVDS transmitter. For 18 bit displays, LVDS channels 0, 1, 2 are used. For 24 bit displays (that accept 18 bit color packing), channels 0, 1, 2 and 3 are used.

NVIDIA T30 CPU		LVDS Transmitter (TI SN75LVDS83B)		Net names	LVDS Channel	Transmit Bit Order	18 Bit standard Color mapping	24 Bit/18 bit compatible Color mapping
Pin #	Pin Name	Pin #	Pin Name					
AK12	LCD_D6	K5	D7	T30_LCD_D [6]	0	1	G0	G2
AH15	LCD_D17	J4	D6	T30_LCD_D [17]		2	R5	R7
AF13	LCD_D16	K3	D4	T30_LCD_D [16]		3	R4	R6
AE18	LCD_D15	J3	D3	T30_LCD_D [15]		4	R3	R5
AD12	LCD_D14	K2	D2	T30_LCD_D [14]		5	R2	R4
AC12	LCD_D13	K1	D1	T30_LCD_D [13]		6	R1	R3
AF9	LCD_D12	J2	D0	T30_LCD_D [12]		7	R0	R2
AF12	LCD_D1	D5	D18	T30_LCD_D [1]	1	1	B1	B3
AE8	LCD_D0	E5	D15	T30_LCD_D [0]		2	B0	B2
AJ12	LCD_D11	F6	D14	T30_LCD_D [11]		3	G5	G7
AK9	LCD_D10	G6	D13	T30_LCD_D [10]		4	G4	G6
AD15	LCD_D9	G5	D12	T30_LCD_D [9]		5	G3	G5
AG8	LCD_D8	J6	D9	T30_LCD_D [8]		6	G2	G4
AG16	LCD_D7	K6	D8	T30_LCD_D [7]		7	G1	G3
AG9	LCD_DE	A3	D26	T30_LCD_DE	2	1	DE	DE
AF10	LCD_VS	B4	D25	T30_LCD_VS		2	VS	VS
AF16	LCD_HS	A4	D24	T30_LCD_HS		3	HS	HS
AK10	LCD_D5	A6	D22	T30_LCD_D [5]		4	B5	B7
AK16	LCD_D4	B5	D21	T30_LCD_D [4]		5	B4	B6
AK15	LCD_D3	B6	D20	T30_LCD_D [3]		6	B3	B5
AD10	LCD_D2	C6	D19	T30_LCD_D [2]		7	B2	B4

NVIDIA T30 CPU		LVDS Transmitter (TI SN75LVDS83B)		Net names	LVDS Channel	Transmit Bit Order	18 Bit standard Color mapping	24 Bit/18 bit compatible Color mapping
Not Used	Not Used	A5	D23	Not Used		1	Not Used	Not Used
AE10	LCD_D19	D6	D17	T30_LCD_D [19]		2	Not Used	B1
AE9	LCD_D18	E6	D16	T30_LCD_D [18]		3	Not Used	B0
AH9	LCD_D21	H6	D11	T30_LCD_D [21]	**3**	4	Not Used	G1
AH13	LCD_D20	H4	D10	T30_LCD_D [20]		5	Not Used	G0
AK13	LCD_D23	K4	D5	T30_LCD_D [23]		6	Not Used	R1
AE13	LCD_D22	J1	D27	T30_LCD_D [22]		7	Not Used	R0
AG11	LCD_PCLK	A2	CLKIN	T30_LCD_PCLK				

3.2.8 Parallel LCD Display Interface

The NVIDIA Tegra parallel 24 bit LCD interface is brought to the Module edge connector. The interface runs at the 1.8V Module I/O voltage. This voltage swing may be used directly with 1.8V capable Carrier Board LVDS transmitters, such as the TI SN75LVDS83B. The 1.8V signaling may not be suitable for direct connection to a parallel flat panel. Generally speaking, only small panels, with screen diagonals of 5" or less, are available with a 1.8V interface. Larger parallel LCD panels are likely to use 3.3V signaling and a set of voltage translators / buffers would be needed on the Carrier.

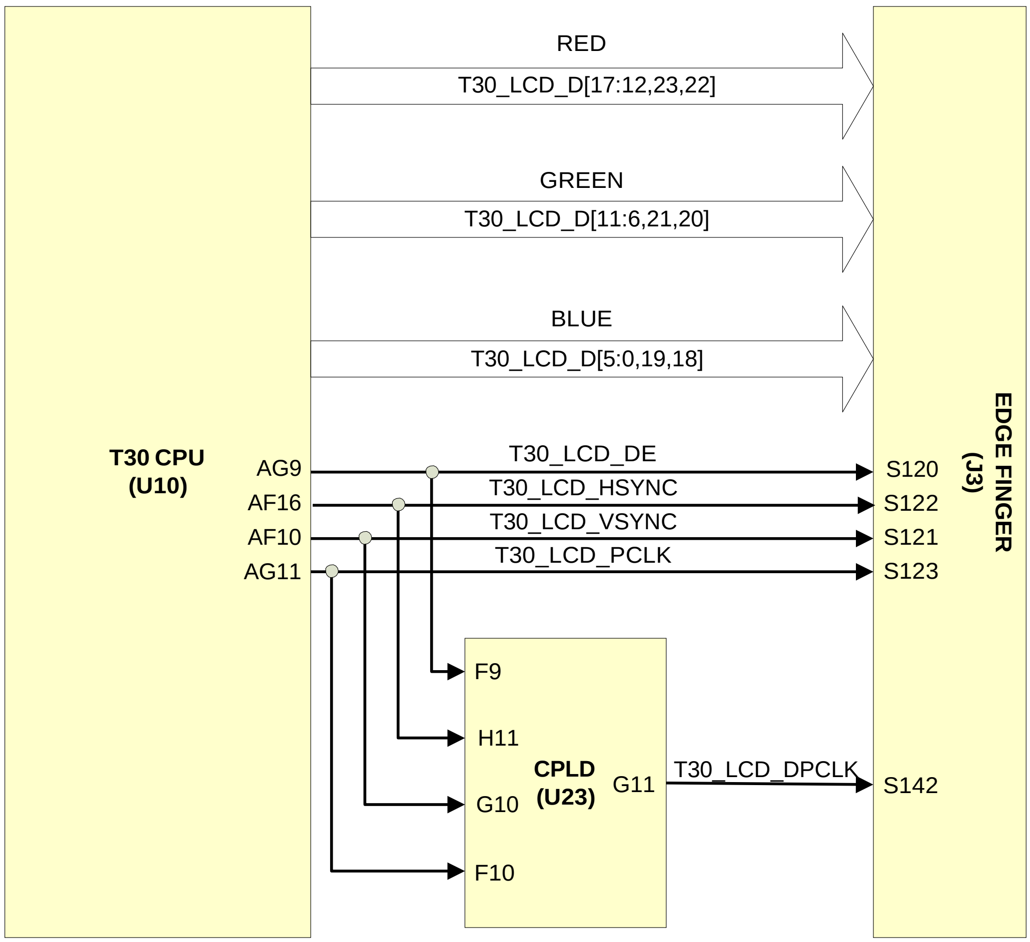

Figure 3: T30 Module Parallel LCD Implementation

The mapping of the NVIDIA Tegra parallel LCD balls to the SMARC edge connector is shown in the table below. Note that the NVIDIA pin names and the SMARC pin names have different assumptions about color mappings, which can make things confusing. Basically, NVIDIA maps the 18 bits or R, G, B for 6 bit color depth to D17:0. For NVIDIA, the extra bits used for a 24 bit color implementation come out on NVIDIA D23:18. The SMARC has a different convention: Red is D23:16; Blue is D15:8 and Green is D7:0. For 24 bit implementations, all bits are used. For 18 bit implementations, in SMARC, the least significant bits (Red D17:16, Green D9:8, Blue D1:0) are dropped.

NVIDIA T30 CPU		SMARC sAT30 Edge finger		Net Name	Color	24 bit Color map
Pin #	Pin Name	Pin #	Pin Name			
AH15	LCD_D17	S118	LCD_D23	T30_LCD_D[17]	RED	R7
AF13	LCD_D16	S117	LCD_D22	T30_LCD_D[16]		R6
AE18	LCD_D15	S116	LCD_D21	T30_LCD_D[15]		R5
AD12	LCD_D14	S115	LCD_D20	T30_LCD_D[14]		R4
AC12	LCD_D13	S114	LCD_D19	T30_LCD_D[13]		R3
AF9	LCD_D12	S113	LCD_D18	T30_LCD_D[12]		R2
AK13	LCD_D23	S112	LCD_D17	T30_LCD_D[23]		R1
AE13	LCD_D22	S111	LCD_D16	T30_LCD_D[22]		R0
AJ12	LCD_D11	S109	LCD_D15	T30_LCD_D[11]	GREEN	G7
AK9	LCD_D10	S108	LCD_D14	T30_LCD_D[10]		G6
AD15	LCD_D9	S107	LCD_D13	T30_LCD_D[9]		G5
AG8	LCD_D8	S106	LCD_D12	T30_LCD_D[8]		G4
AG16	LCD_D7	S105	LCD_D11	T30_LCD_D[7]		G3
AK12	LCD_D6	S104	LCD_D10	T30_LCD_D[6]		G2
AH9	LCD_D21	S103	LCD_D9	T30_LCD_D[21]		G1
AH13	LCD_D20	S102	LCD_D8	T30_LCD_D[20]		G0
AK10	LCD_D5	S100	LCD_D7	T30_LCD_D[5]	BLUE	B7
AK16	LCD_D4	S99	LCD_D6	T30_LCD_D[4]		B6
AK15	LCD_D3	S98	LCD_D5	T30_LCD_D[3]		B5
AD10	LCD_D2	S97	LCD_D4	T30_LCD_D[2]		B4
AF12	LCD_D1	S96	LCD_D3	T30_LCD_D[1]		B3
AE8	LCD_D0	S95	LCD_D2	T30_LCD_D[0]		B2
AE10	LCD_D19	S94	LCD_D1	T30_LCD_D[19]		B1
AE9	LCD_D18	S93	LCD_D0	T30_LCD_D[18]		B0

NVIDIA T30 CPU		SMARC sAT30 Edge finger		Net Name	Color	24 bit Color map
AG11	LCD_PCLK	S123	LCD_PCK	T30_LCD_PCLK		
AG9	LCD_DE	S120	LCD_DE	T30_LCD_DE		
AF16	LCD_HS	S122	LCD_HS	T30_LCD_HSYNC		
AF10	LCD_VS	S121	LCD_VS	T30_LCD_VSYNC		
		S142	LCD_DUAL_PCK	T30_LCD_DPCLK		

The LCD_DUAL_PCK signal is used to latch odd and even pixels into separate latches on the Carrier board, for high resolution displays, either for parallel LCD implementations or dual channel LVDS. The LCD_DUAL_PCK is derived on the Module from the LCD_PCK pixel clock. The LCD_DUAL_PCK is one-half the frequency of the LCD_PCK clock. The Module hardware ensures that the dual pixel clock is phased correctly with the display field. The LCD_DUAL_PCK rising edge is used to latch odd pixels and the falling edge to latch even pixels. The upper leftmost pixel in the display image is pixel 1 (an odd pixel), followed by pixel 2 (an even pixel) and so on. LCD_DUAL_PCK is generated using the module’s CPLD.

3.2.9 Carrier Based 24 bit Color Depth LVDS

The Module parallel LCD path may be used to implement single or dual channel Carrier Board LVDS transmitter(s). The color packing may be 24 bit or 18 bit. Since 18 bit single channel color packing is already available from the Module LVDS, only 24 bit color packing is described in this section.

A single channel implementation uses one SN75LVDS83B (or equivalent) LVDS transmitter. A dual channel implementation uses two transmitters – one for the odd pixels and one for the even pixels. The input to the two transmitters is the same for both parts (they are wired in parallel). The odd and even pixels are separated out from the input data by the rising and falling edges of the LCD_DUAL_PCK.

The following pins on the transmitter are used slightly differently in the single and dual channel cases:

Pixel Clock Input (Ball A2, Pin Name CLKIN)	For single channel implementations, connect to the SMARC LCD_PCK pin (S123) For dual channel implementations, connect to the SMARC LCD_DUAL_PCK pin (S142)
Clock Edge Select (Ball D4, Pin Name CLKSEL)	For single channel implementations: provide for resistor strapping options to tie this high or low. The default strapping should be low, which sets the TI LVDS transmitter to latch data in on the falling edge of the LCD_PCK. For dual channel implementations, provide for strapping options to tie the CLKSEL pins high or low. The two transmitters should have separate strapping options (or one set of strapping options and an inverter to set the CLKSEL pin on the 2nd transmitter to the opposite edge). The first transmitter, for odd pixels, should be set to latch the data on the rising edge of LCD_DUAL_PCK. The second transmitter, for even pixels, should be set to latch the data on the falling edge of the LCD_DUAL_PCK.

The following table shows how the sAT30 LCD pins should be mapped to a particular LVDS transmitter, the TI SN75LVDS83B, for standard LVDS 24 bit color packing, single and dual channel. The chart shows pin numbers for the BGA version of the part. The TSSOP version can be used as well, although the pin numbering is different. The pin names remain the same. Transmitters from other vendors may be used as well. For dual channel implementations, the same data path pin mapping is used for both channels (i.e. the LVDS transmitter LCD parallel data inputs are to be connected in parallel).

SMARC sAT30 Edge finger		LVDS Transmitter (TI SN75LVDS83B)		LVDS Channel	Transmit bit Order	24 bit standard color mapping
Pin #	Pin Name	Pin #	Pin Name			
S102	LCD_D8	K5	D7		1	G0
S116	LCD_D21	J4	D6		2	R5
S115	LCD_D20	K3	D4		3	R4
S114	LCD_D19	J3	D3	**0**	4	R3
S113	LCD_D18	K2	D2		5	R2
S112	LCD_D17	K1	D1		6	R1
S111	LCD_D16	J2	D0		7	R0
S94	LCD_D1	D5	D18		1	B1
S93	LCD_D0	E5	D15		2	B0
S107	LCD_D13	F6	D14		3	G5
S106	LCD_D12	G6	D13	**1**	4	G4
S105	LCD_D11	G5	D12		5	G3
S104	LCD_D10	J6	D9		6	G2
S103	LCD_D9	K6	D8		7	G1
S120	LCD_DE	A3	D26		1	DE
S121	LCD_VS	B4	D25		2	VS
S122	LCD_HS	A4	D24		3	HS
S98	LCD_D5	A6	D22	**2**	4	B5
S97	LCD_D4	B5	D21		5	B4
S96	LCD_D3	B6	D20		6	B3
S95	LCD_D2	C6	D19		7	B2
N/C	N/C	A5	D23	**3**	1	Not Used

SMARC sAT30 Edgefinger		LVDS Transmitter (TI SN75LVDS83B)		LVDS Channel	Transmit bit Order	24 bit standard color mapping
S100	LCD_D7	D6	D17		2	B7
S99	LCD_D6	E6	D16		3	B6
S109	LCD_D15	H6	D11		4	G7
S108	LCD_D14	H4	D10		5	G6
S118	LCD_D23	K4	D5		6	R7
S117	LCD_D22	J1	D27		7	R6
S123 S142	LCD_PCK LCD_DUAL_PCK	A2	CLKIN			Single Channel Only Dual Channel Only

3.2.10 High-Definition-Multimedia-Interface (HDMI) Interface

The SMARC sAT30 module supports a single HDMI interface with a resolution up to 1920x1080 pixels. HDMI signals are exposed on the SMARC sAT30 edge connector as shown below:

SMARC sAT30 Edge finger		NVIDIA T30 CPU		Net Name	Notes
Pin #	Pin Name	Pin #	Pin Name		
HDMI Differential Signals					
P98	HDMI_D0+	AH4	HDMI_TXD0P	HDMI_TXD0_P	HDMI Differential Data pair 0 output
P99	HDMI_D0-	AJ4	HDMI_TXD0N	HDMI_TXD0_N	
P95	HDMI_D1+	AJ6	HDMI_TXD1P	HDMI_TXD1_P	HDMI Differential Data pair 1 output
P96	HDMI_D1-	AH6	HDMI_TXD1N	HDMI_TXD1_N	
P92	HDMI_D2+	AJ7	HDMI_TXD2P	HDMI_TXD2_P	HDMI Differential Data pair 2 output
P93	HDMI_D2-	AK7	HDMI_TXD2N	HDMI_TXD2_N	
P101	HDMI_CK+	AK4	HDMI_TXCP	HDMI_TXCLK_P	HDMI Differential clock output
P102	HDMI_CK-	AK3	HDMI_TXCN	HDMI_TXCLK_N	
HDMI Support signals					
P104	HDMI_HPD	AG13	HDMI_INT	HDMI_HPD_AP	HDMI Hot Plug Detect input
P105	HDMI_CTRL_CK	AG14	DDC_SCL	HDMI_DDC_SCL_1V8	HDMI dedicated I2C Clock
P106	HDMI_CTRL_DAT	AJ10	DDC_SDA	HDMI_DDC_SDA_1V8	HDMI dedicated I2C Data
P107	HDMI_CEC	AC18	HDMI_CEC	HDMI_CEC	Not used

The Carrier board must do voltage translation for the DDC and HPD signals, as well as ESD protection on all the HDMI signals. The Carrier board ESD protection is important as HDMI is a hot-pluggable interface. A device such as the Texas Instruments TPD12S016 is recommended. The Kontron SMARC Evaluation Board schematic (KAI 501-146) is useful as an implementation example.

3.2.11 Camera Serial Interfaces (CSI) Interface

The SMARC sAT30 module supports two dual lane CSI interfaces (named CSI0 and CSI1 according to the SMARC Hardware specification). The SMARC four-lane CSI interface option is not supported. The camera interface requirements are bound to the performance of the interfaces native to the NVIDIA Tegra T30 SoC.

CSI interface signals are exposed on the SMARC sAT30 edge connector as shown below:

SMARC sAT30 Edge finger		NVIDIA T30 CPU		Net Name	Notes
Pin #	Pin Name	Pin #	Pin Name		
CSI0 Camera Interface					
S11	CSI0_D0+/PCAM_D12	AD2	CSI_D1AP	CSI0_D0A_P	CSI0 Differential data pair0 in
S12	CSI0_D0-/ PCAM_D13	AD3	CSI_D1AN	CSI0_D0A_N	
S14	CSI0_D1+/PCAM_D14	AE3	CSI_D2AP	CSI0_D1A_P	CSI0 Differential data pair1 in
S15	CSI0_D1-/PCAM_D15	AE2	CSI_D2AN	CSI0_D1A_N	
S8	CSI0_CK+/PCAM_D10	AD4	CSI_CLKAP	CSI0_CK_P	CSI0 Differential clock in
S9	CSI0_CK-/PCAM_D11	AC4	CSI_CLKAN	CSI0_CK_N	
CSI1 Camera Interface					
P7	CSI1_D0+/PCAM_D2	AE1	CSI_D1BP	CSI1_D0B_P	CSI1 Differential data pair0 in
P8	CSI1_D0-/PCAM_D3	AD1	CSI_D1BN	CSI1_D0B_N	
P10	CSI1_D1+/PCAM_D4	AH1	CSI_D2BP	CSI1_D1B_P	CSI1 Differential data pair1 in
P11	CSI1_D1-/PCAM_D5	AH2	CSI_D2BN	CSI1_D1B_N	
P13	CSI1_D2+/PCAM_D6				Not used
P14	CSI1_D2-/PCAM_D7				
P16	CSI1_D3+/PCAM_D8				Not used
P17	CSI1_D3-/PCAM_D9				
P3	CSI1_CK+ / PCAM_D0	AG2		CSI1_CK_P	CSI1 Differential clock in
P4	CSI1_CK-/PCAM_D1	AG3		CSI1_CK_N	
CSI Camera support signals					
S6	CAM_MCK	AD5	CAM_MCLK	CAM_MCLK	Master CLK out
S5	I2C_CAM_CK	AG5	CAM_I2C_SCL	I2C_CAM_CLK	I2C Camera support clock

SMARC sAT30 Edge finger		NVIDIA T30 CPU		Net Name	Notes
S7	I2C_CAM_DAT	AH7	CAM_I2C_SDA	I2C_CAM_DAT	I2C Camera support data
S57	PCAM_ON_CSI0#				Left open to support the CSI0 (Serial camera) selection
S58	PCAM_ON_CSI1#				Left open to support the CSI1 (Serial camera) selection
P108	GPIO0 / CAM0_PWR#	J30	KB_COL00	GPIO0/ CAM0_PWR#	Camera 0 Power Enable, active low output.
P109	GPIO1 / CAM1_PWR#	N26	KB_COL01	GPIO1/ CAM1_PWR#	Camera 1 Power Enable, active low output
P110	GPIO2 / CAM0_RST#	V25	KB_COL02	GPIO2/ CAM0_RST#	Camera 0 Reset, active low output
P111	GPIO3 / CAM1_RST#	K28	SDMMC3_DAT 7	GPIO3/ CAM1_RST#	Camera 1 Reset, active low output

3.2.12 USB Interfaces

The Kontron sAT30 module supports three USB ports (USB 0:2). Per the SMARC specification, the Kontron sAT30 module supports a USB "On-The-Go" (OTG) port capable of functioning either as a client or host device, on the ULP-COM USB0 port. The sAT30 module also supports two additional USB2.0 host ports, on SMARC USB1 and USB2.

USB interface signals are exposed on the SMARC sAT30 edge connector as shown below:

SMARC sAT30 Edge finger		NVIDIA T30 CPU		Net Name	Notes
Pin #	Pin Name	Pin #	Pin Name		
USB0 Port					
P60	USB0+	W2	USB1_DP	T30_USB0_DP	USB0 port data pair
P61	USB0-	W3	USB1_DN	T30_USB0_DN	
P63	USB0_VBUS_DET	W5	USB1_VBUS	V_3V3_VBUS (5V tolerant, in spite of the net name)	USB host power detection, when this port is used as a device.
P64	USB0_OTG_ID	T7	USB1_ID		USB OTG ID input, active high
USB1 Port					
P65	USB1+	T5	USB2_DP	T30_USB1_DP	USB1 port data pair
P66	USB1-	T6	USB2_DN	T30_USB1_DN	
USB2 Port					
P69	USB2+	V2	USB3_DP	T30_USB2_DP	USB2 port data pair
P70	USB2-	V3	USB3_DN	T30_USB2_DN	

The SMARC Hardware specification defines USBx_EN_OC# (where x is 0, 1 and 2 for use with USB0, USB1 and USB2) pins as multifunction pins to use for power enable of USBx ports, as well as for over current indication. The SMARC sAT30 complies with this definition. These nets are provided with pull up resistors on the Module. The Module CPLD contains the glue logic required for this implementation.

The sAT30 Module USB power enable and over current indication logic implementation is shown in the following block diagram. There are 10K pull-up resistors on the Module on the SMARC USBx_EN_OC# lines. The CPLD outputs driving the USBx_EN_OC# lines are open-drain. The Carrier board USB power switch, if present, is enabled by virtue of the 10K Module pull-up to 3.3V.

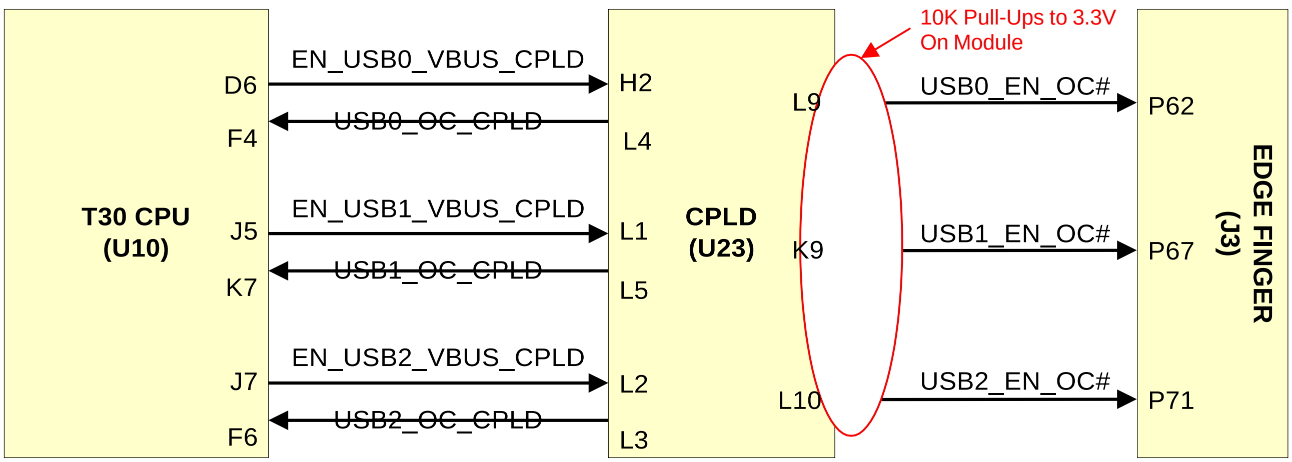

Figure 4: External USB Port Power Distribution Logic Implementation

USB port power enable and over current logic implementation between the T30 CPU and CPLD is shown in the following table:

NVIDIA T30 CPU		CPLD		Net Name	Notes
Pin #	Pin Name	Pin #	Pin Name		
D6	GMI_CS4#	H2	IO_H2	EN_USB0_VBUS_CPLD	USB Port0 power enable
J5	GMI_CS6#	L1	IO_L1	EN_USB1_VBUS_CPLD	USB Port1 power enable
J7	GMI_CS7#	L2	IO_L2	EN_USB2_VBUS_CPLD	USB Port2 power enable
F4	GMI_AD09	L4	IO_L4	USB0_OC_CPLD#	USB Port0 over current indication signal
K7	GMI_CS1#	L5	IO_L5	USB1_OC_CPLD#	USB Port1 over current indication signal
F6	GMI_CS2#	L3	IO_L3	USB2_OC_CPLD#	USB Port2 over current indication signal

USB port power enable and over current logic implementation between the CPLD and SMARC sAT30 edge connector is shown in the table below:

CPLD		SMARC sAT30 Edge Finger		Net Name	Notes
Pin #	Pin Name	Pin #	Pin Name		
L9	IO_L9	P62	USB0_EN_OC#	EN_USB0_VBUS_OC#	USB Port0 power enable/over current indication signal
K9	IO_K9	P67	USB1_EN_OC#	EN_USB1_VBUS_OC#	USB Port1 power enable/over current indication signal
L10	IO_L10	P71	USB2_EN_OC#	EN_USB2_VBUS_OC#	USB Port2 power enable/over current indication signal

Power distribution for external USB plug-in peripherals (USB memory sticks, cameras, keyboards, mice, etc.) is typically handled by USB power switches such as the Texas Instruments TPS2052B, Micrel MIC2026-1 or similar devices on the Carrier board. The Enable pin on the Carrier board USB power switch must be active – high and the Over-Current pin (OC#) must be open drain, active low (these are commonly available). No pull-up is required on the USB power switch Enable or OC# line; they are tied together on the Carrier and fed to the Module USBx_EN_OC# pin. The pull-up is on the Module.

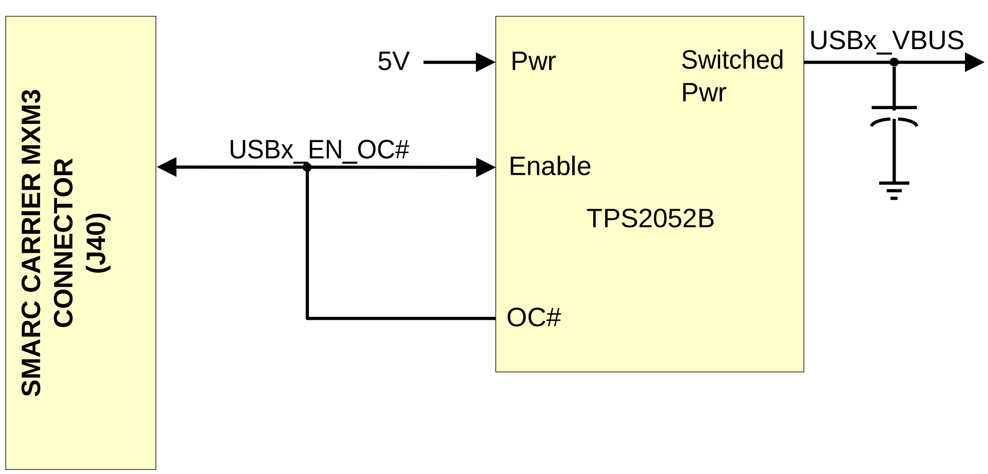

Figure 5: USB Power Distribution Implementation on Carrier

3.2.13 PCIe Interfaces

The SMARC sAT30 module supports two external PCIe x 1 interfaces, designated PCIE_A and PCIE_B in the SMARC specification. Of the three the NVIDIA T30 CPU PCIe interfaces, one is used on the Module for the GbE controller, described in Section 3.2.13 Gigabit Ethernet Controller (GbE) Interface. Two are used for SMARC external PCIe interfaces.

PCIe interface signals are exposed on the SMARC sAT30 edge connector as shown below:

SMARC sAT30 Edge Finger		NVIDIA T30 CPU		Net Name	Notes
Pin #	Pin Name	Pin #	Pin Name		
PCIe_Link A					
P89	PCIE_A_TX+	AF21	PEX_L4_TXP	PCIEA_TX_P	Differential PCIe Link A transmit data pair 0. Series decoupling caps are provided in the Module.
P90	PCIE_A_TX-	AG21	PEX_L4_TXN	PCIEA_TX_N	
P86	PCIE_A_RX+	AH24	PEX_L4_RXP	PCIEA_RX_P	Differential PCIe Link A receive data pair 0. Series coupling caps are ***not*** provided in the Module.
P87	PCIE_A_RX-	AJ24	PEX_L4_RXN	PCIEA_RX_N	
P83	PCIE_A_REFCK+	AB23	PEX_CLK2P	PCIEA_REF_CLK_P	Differential PCIe Link A reference clock output
P84	PCIE_A_REFCK-	AB24	PEX_CLK2N	PCIEA_REF_CLK_N	
P78	PCIE_A_CKREQ#	AD26	PEX_L1_CLKREQ	PCIEA_CLK_REQ#	PCIe Port A clock request input
P74	PCIE_A_PRSNT#	AD24	PEX_L1_PRSNT	PCIEA_PRSNT#	PCIe Port A present input
P75	PCIE_A_RST#	AG27	PEX_L1_RST	T30_PCIEA_RST#	PCIe Port B reset output, active low. Provision is provided to connect pin P75 to GMI_AD15 (F1) through a 0 ohm resistor, R303 (R303 should not be installed)
PCIe_Link B					
S90	PCIE_B_TX+	AF18	PEX_L0_TXP	PCIEB_TX_P	Differential PCIe Link B transmit data pair 0. Series decoupling caps are provided in the Module.
S91	PCIE_B_TX-	AG18	PEX_L0_TXN	PCIEB_TX_N	

SMARC sAT30 Edge Finger		NVIDIA T30 CPU		Net Name	Notes
S87	PCIE_B_RX+	AH19	PEX_L0_RXP	PCIEB_RX_P	Differential PCIe Link B receive data pair 0. Series coupling caps are ***not*** provided in the Module.
S88	PCIE_B_RX-	AJ19	PEX_L0_RXN	PCIEB_RX_N	
S84	PCIE_B_REFCK+	AK27	PEX_CLK1P	PCIEB_REF_CLK_P	Differential PCIe Link B reference clock output
S85	PCIE_B_REFCK-	AK28	PEX_CLK1N	PCIEB_REF_CLK_N	
P77	PCIE_B_CKREQ#	AG24	PEX_L0_CLKREQ		PCIe Port B clock request input
P73	PCIE_B_PRSNT#	AD25	PEX_L0_PRSNT		PCIe Port B present input, active low
S76	PCIE_B_RST#	AG26	PEX_L0_RST#		PCIe Port B reset output, active low
PCIe_Link C					
S81	PCIE_C_TX+				Not used
S82	PCIE_C_TX-				
S78	PCIE_C_RX+				Not used
S79	PCIE_C_RX-				
P80	PCIE_C_REFCK+				Not used
P81	PCIE_C_REFCK-				
P76	PCIE_C_CKREQ#				Not used
PCIe_Link C					
P72	PCIE_C_PRSNT#				Not used
S77	PCIE_C_RST#				Not used
PCIe Wake					
S146	PCIE_WAKE#	AF22	PEX_WAKE#	PCIE_WAKE#	PCIe wake up interrupt to host

3.2.14 SATA Interface

The SMARC sAT30 module supports one SATA port.

SATA interface signals are exposed on the SMARC sAT30 edge connector as shown below:

SMARC sAT30 Edge finger		NVIDIA T30 CPU		Net Name	Notes
Pin #	Pin Name	Pin #	Pin Name		
P48	SATA_TX+	AE16	SATA_L0_TXP	T30_SATA_TX_P	Differential SATA 0 transmit data Pair. Series decoupling caps are provided in the Module.
P49	SATA_TX-	AD16	SATA_L0_TXN	T30_SATA_TX_N	
P51	SATA_RX+	AD19	SATA_L0_RXP	T30_SATA_RX_P	Differential SATA 0 receive data Pair. Series decoupling caps are provided in the Module.
P52	SATA_RX-	AE19	SATA_L0_RXN	T30_SATA_RX_N	
S54	SATA_ACT#	A3	GMI_CS3#	SATA_ACT_LED#	Active low SATA activity indicator

3.2.15 Gigabit Ethernet Controller (GbE) Interface

The SMARC sAT30 module supports one GbE interface. This is accomplished by using the Intel I210 (Springville) GbE MAC+PHY using one of the T30 SoC's PCIe interfaces. This is diagrammed below. The PCIe coupling caps are not shown in the diagram.

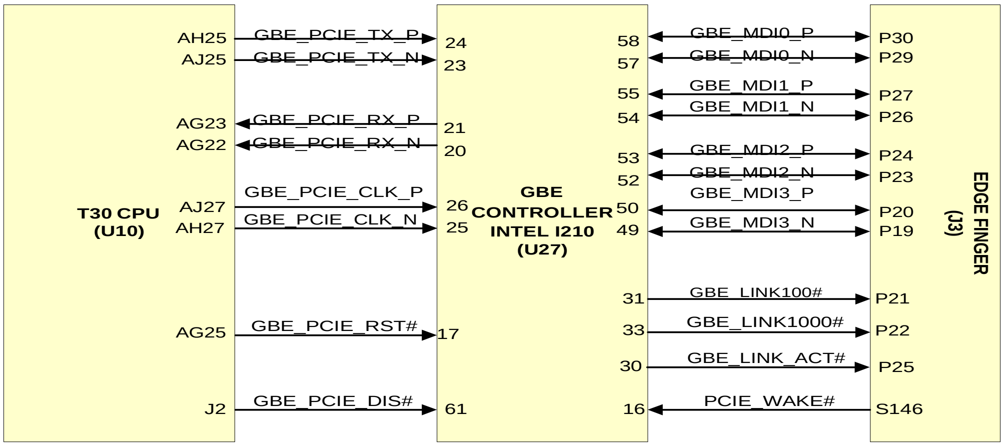

Figure 6 GbE Controller Implementation

The following table details the Tegra to I210 connection details.

NVIDIA T30 CPU		Intel I210		Net Name	Notes
Pin #	Pin Name	Pin #	Pin Name		
AH25	PEX_L5_TXP	24	PE_RX+	GbE_PCIE_TX_P	Differential PCIe GbE transmit data pair
AJ25	PEX_L5_TXN	23	PE_RX-	GbE_PCIE_TX_N	
AG23	PEX_L5_RXP	21	PE_TX+	GbE_PCIE_RX_P	Differential PCIe GbE receive data pair
AG22	PEX_L5_RXN	20	PE_TX-	GbE_PCIE_RX_N	
AJ27	PEX_CLK3P	26	PECLK+	GbE_PCIE_CLK_P	Differential PCIe GbE reference clock
AH27	PEX_CLK3N	25	PECLK-	GbE_PCIE_CLK_N	
AG25	PEX_L2_RST#	17	PE_RST#	GbE_PCIE_RST#	PCIe GbE reset input
J2	GMI_AD14	61	SDP1	GbE_PCIE_DIS#	INTEL I210 PCIe interface disable

The details of the Intel I210 mapping to the SMARC Edge fingers are shown here:

SMARC sAT30 Edge finger		Intel 210		Net Name	Notes
Pin #	Pin Name	Pin #	Pin Name		
P30	GbE_MDI0+	58	MDI0+	GbE_MDI0_P	Bi-directional transmit/receive pair 0 to magnetics
P29	GbE_MDI0-	57	MDI0-	GbE_MDI0_N	
P27	GbE_MDI1+	55	MDI1+	GbE_MDI1_P	Bi-directional transmit/receive pair 1 to magnetics
P26	GbE_MDI1-	54	MDI1-	GbE_MDI1_N	
P24	GbE_MDI2+	53	MDI2+	GbE_MDI2_P	Bi-directional transmit/receive pair 2 to magnetics
P23	GbE_MDI2-	52	MDI2-	GbE_MDI2_N	
P20	GbE_MDI3+	50	MDI3+	GbE_MDI3_P	Bi-directional transmit/receive pair 3 to magnetics
P19	GbE_MDI3-	49	MDI3-	GbE_MDI3_N	
P21	GbE_LINK100#	31	LED0	GbE_LINK100#	Link speed indication LED for 100Mbps – open drain
P22	GbE_LINK1000#	33	LED1	GbE_LINK1000#	Link speed indication LED for 1000Mbps – open drain
P25	GbE_LINK_ACT#	30	LED2	GbE_LINK_ACT#	Link/activity LED – open drain
S146	PEX_WAKE#	16	PE_WAKE#	PCIE_WAKE#	PCIe GbE wake signal

3.2.16 SDIO Interface

The SMARC sAT30 module supports a 4bit SDIO interface, per the SMARC specification. The SDIO interface uses 3.3V signaling, per the SMARC spec and for compatibility with commonly available SDIO cards.

SDIO interface signals are exposed on the SMARC sAT30 edge connector as shown below:

SMARC sAT30 Edge finger		NVIDIA T30 CPU		Net Name	Notes
Pin #	Pin Name	Pin #	Pin Name		
P39	SDIO_D0	K1	SDMMC1_DAT0	SDIO_D[0]	SDIO Data
P40	SDIO_D1	K2	SDMMC1_DAT1	SDIO_D[1]	
P41	SDIO_D2	K3	SDMMC1_DAT2	SDIO_D[2]	
P42	SDIO_D3	K4	SDMMC1_DAT3	SDIO_D[3]	
P34	SDIO_CMD	N6	SDMMC1_CMD	SDIO_CMD	SDIO Command signal
P36	SDIO_CK	M6	SDMMC1_CLK	SDIO_CLK	SDIO Clock signal
P33	SDIO_WP	K5	CLK2_OUT	SDIO_WP	SDIO write protect signal
P35	SDIO_CD#	M5	GPIO_PV2	SDIO_CD#	SDIO card detect
P37	SDIO_PWR_EN	M1	GPIO_PV3	SDIO_PWR_EN	SD card power enable

The SDIO card power should be switched on the Carrier board and the SDIO lines should be ESD protected. The SMARC Evaluation Carrier schematic is useful as an implementation reference.

3.2.17 SDMMC Interface for Carrier eMMC

The SMARC sAT30 module supports a 4bit SDMMC interface that may be used with a Carrier based eMMC device. The SMARC specification provides for an SDMMC data path that may be up to 8 bits wide. Only the lower 4 bits are used in the sAT30 implementation. EMMC devices that may be used with this interface are required to be able to operate in 1 bit, 4 bit or 8 bit modes. The signaling level is at the Module I/O voltage level of 1.8V.

SDMMC interface signals are exposed on the SMARC sAT30 edge connector as shown below:

SMARC sAT30 Edge finger		NVIDIA T30 CPU		Net Name	Notes
Pin #	Pin Name	Pin #	Pin Name		
S26	SDMMC_D0	L27	SDMMC3_DAT0	T3_SDMMC[0]	SDMMC Data
S27	SDMMC_D1	J26	SDMMC3_DAT1	T3_SDMMC[1]	
S28	SDMMC_D2	J28	SDMMC3_DAT2	T3_SDMMC[2]	
S29	SDMMC_D3	K26	SDMMC3_DAT3	T3_SDMMC[3]	
S30	SDMMC_D4				Not used
S31	SDMMC_D5				Not used
S32	SDMMC_D6				Not used
S33	SDMMC_D7				Not used
S35	SDMMC_CK	G30	SDMMC3_CLK	T3_SDMMC3_CLK	SDMMC Clock
S36	SDMMC_CMD	J29	SDMMC3_CMD	T3_SDMMC3_CMD	SDMMC Command
S37	SDMMC_RST#	K24	SDMMC3_DAT6	WF_RST#	Reset signal to Carrier eMMC flash

3.2.18 SPI Interfaces

The SMARC sAT30 module supports three T30 SPI interfaces. One is used on the Module for an 8MB SPI device. Two are available off-Module for general purpose use.

SPI interface signals are exposed on the SMARC sAT30 edge connector as shown below:

SMARC sAT30 Edge finger		NVIDIA T30 CPU		Net Name	Notes
Pin #	Pin Name	Pin #	Pin Name		
SPI0					
P43	SPI0_CS0#	J24	SPI1_CS0#	T3_SPI1_CS0#	SPI0 Master Chip Select 0 output
P31	SPI0_CS1#	N4	ULPI_STP	T3_SPI1_CS1#	SPI0 Master Chip Select 1 output
P44	SPI0_CK	B28	SPI1_SCK	T3_SPI1_SCK	SPI0 Master Clock output
P45	SPI0_DIN	F28	SPI1_MISO	T3_SPI1_MISO	SPI0 Master Data input (input to CPU, output from SPIdevice)
P46	SPI0_DO	F29	SPI1_MOSI	T3_SPI1_MOSI	SPI0 Master Data output (output from CPU, input to SPIdevice)
SPI1					
P54	SPI1_CS0#	G28	SPI2_CS0#	T3_SPI2_CS0	SPI1 Master Chip Select 0 output
P55	SPI1_CS1#	F25	SPI2_CS1#	T3_SPI2_CS1#	SPI1 Master Chip Select 1 output
P56	SPI1_CK	D29	SPI2_SCK	T3_SPI2_SCK	SPI1 Master Clock output
P57	SPI1_DIN	D30	SPI2_MISO	T3_SPI2_MISO	SPI1 Master Data input (input to CPU, output from SPI device)
P58	SPI1_DO	B27	SPI2_MOSI	T3_SPI2_MOSI	SPI1 Master Data output (output from CPU, input to (SPI device)

3.2.19 I2S Interfaces

The SMARC sAT30 module supports three off-Module I2S (DAP) interfaces. The default SMARC audio interface is I2S0 and the Kontron sAT30 bootloader implements this. The other I2S ports may be used for audio (if the bootloader is re-configured for this) or may be used for other devices that accept an I2S interface.

I2S interface signals are exposed on the SMARC sAT30 edge connector as shown below:

SMARC sAT30 Edge finger		NVIDIA T30 CPU		Net Name	Notes
Pin #	Pin Name	Pin #	Pin Name		
I2S0					
S39	I2S0_LRCK	C29	DAP2_FS	DAP2_FS	Left& Right audio synchronization clock
S40	I2S0_SDOUT	G27	DAP2_DOUT	DAP2_DOUT	Digital audio Output
S41	I2S0_SDIN	F27	DAP2_DIN	DAP2_DIN	Digital audio Input
S42	I2S0_CK	C28	DAP2_SCLK	DAP2_SCLK	Digital audio clock
I2S1					
S43	I2S1_LRCK	R4	DAP3_FS	DAP1_FS	Left& Right audio synchronization clock
S44	I2S1_SDOUT	M3	DAP3_DOUT	DAP1_DOUT	Digital audio Output
S45	I2S1_SDIN	N3	DAP3_DIN	DAP1_DIN	Digital audio Input
S46	I2S1_CK	R6	DAP3_SCLK	DAP1_SCLK	Digital audio clock
I2S2					
S50	I2S2_LRCK	AA24	DAP4_FS	DAP0_FS	Left& Right audio synchronization clock
S51	I2S2_SDOUT	W28	DAP4_DOUT	DAP0_DOUT	Digital audio Output
S52	I2S2_SDIN	AA29	DAP4_DIN	DAP0_DIN	Digital audio Input
S53	I2S2_CK	AA26	DAP4_SCLK	DAP0_SCLK	Digital audio clock
Audio Master clock					
S38	AUDIO_MCK	C27	CLK1_OUT	AUDIO_MCLK	Master clock output to Audio codec

3.2.20 SPDIF Interface

The SMARC sAT30 module supports one SPDIF interface.

SPDIF interface signals are exposed on the SMARC sAT30 edge connector as shown below:

SMARC sAT30 Edge finger		NVIDIA T30 CPU		Net Name	Notes
Pin #	Pin Name	Pin #	Pin Name		
S59	SPDIF_OUT	A28	SPDIF_OUT	SPDIF_OUT	Digital Audio Output
S60	SPDIF_IN	H27	SPDIF_IN	SPDIF_IN	Digital Audio Input

3.2.21 Asynchronous Serial Ports

The SMARC sAT30 module supports four UARTs (SER0:3). UARTs SER0 and SER2 supports flow control signals (RTS, CTS). UARTs SER1 and SER3 do not support flow control. When working with Linux for Tegra (L4T), SER 1 is used for T30 CPU debugging.

The sAT30 asynchronous serial port signals have a 1.8V level signal swing. They can be converted to RS232 level and polarity signals by using a suitable RS232 transceiver. There are transceivers available that accept a 1.8V signal level: some examples include the Texas Instruments TRS3253E, the Maxim MAX3218 and the Linear Technology LTC2801. Note that RS232 transceivers invert the signal; a logic '1' is a negative voltage (-3.0V to -15V) and a logic '0' a positive voltage (3.0V to 15V) on the RS232 line. Asynchronous serial ports interface signals are exposed on the SMARC sAT30 edge connector as shown below:

SMARC sAT30 Edge finger		NVIDIA T30 CPU		Net Name	Notes
Pin #	Pin Name	Pin #	Pin Name		
SER0					
P129	SER0_TX	W25	UART2_TXD	SER0_TXD	Asynchronous serial port data out
P130	SER0_RX	AB28	UART2_RXD	SER0_RXD	Asynchronous serial port data in
P131	SER0_RTS#	AB26	UART2_RTS#	SER0_RTS	Request to Send handshake line for SER0
P132	SER0_CTS#	AA25	UART2_CTS#	SER0_CTS	Clear to Send handshake line for SER0
SER1					
P134	SER1_TX	R3	ULPI_DATA0	SER1_TXD	Asynchronous serial port data out
P135	SER1_RX	V1	ULPI_DATA1	SER1_RXD	Asynchronous serial port data in
SER2					
P136	SER2_TX	AC27	UART3_TXD	SER2_TXD	Asynchronous serial port data out
P137	SER2_RX	W27	UART3_RXD	SER2_RXD	Asynchronous serial port data in
P138	SER2_RTS#	AB29	UART3_RTS#	SER2_RTS	Request to Send handshake line for SER2
P139	SER2_CTS#	W29	UART3_CTS#	SER2_CTS	Clear to Send handshake line for SER2
SER3					
P140	SER3_TX	M2	ULPI_CLK	SER3_TXD	Asynchronous serial port data out
P141	SER3_RX	M4	ULPI_DIR	SER3_RXD	Asynchronous serial port data in

3.2.22 I2C Interface

There are five I2C buses defined in the SMARC specification: PM (Power Management), LCD (Liquid Crystal Display), GP (General Purpose), CAM (Camera) and HDMI. The sAT30 supports multiple masters and slaves in fast mode (400 KHz operation). A high speed mode (3.4 MHz) option also exists, although many I2C peripherals may have trouble with this. The I2C interface signals are exposed on the SMARC sAT30 edge connector as shown below:

SMARC sAT30 Edge finger		NVIDIA T30 CPU		Net Name	Notes
Pin #	Pin Name	Pin #	Pin Name		
PM I2C					
P121	I2C_PM_CK	M24	PWR_I2C_SCL	PWR_I2C_SCL_1V8	Power management I2C bus clock
P122	I2C_PM_DAT	N27	PWR_I2C_SDA	PWR_I2C_SDA_1V8	Power management I2C bus data
GP I2C					
S48	I2C_GP_CK	G5	GEN2_I2C_SCL	GEN2_I2C_SCL_1V8	General purpose I2C bus clock
S49	I2C_GP_DAT	G7	GEN2_I2C_SDA	GEN2_I2C_SDA_1V8	General purpose I2C bus data
CAM I2C					
S5	I2C_CAM_CK	AG5	CAM_I2C_SCL	I2C_CAM_CLK	I2C Camera support clock
S7	I2C_CAM_DAT	AH7	CAM_I2C_SDA	I2C_CAM_DAT	I2C Camera support data
LCD I2C					
S139	I2C_LCD_CK	AB25	GEN1_I2C_SCL	LCD_DDC_CLK	LCD display I2C bus clock
S140	I2C_LCD_DAT	V29	GEN1_I2C_SDA	LCD_DDC_DATA	LCD display I2C bus data
HDMI I2C					
P105	HDMI_CTRL_CK	AG14	DDC_SCL	HDMI_DDC_SCL_1V8	HDMI dedicated I2C Clock
P106	HDMI_CTRL_DAT	AJ10	DDC_SDA	HDMI_DDC_SDA_1V8	HDMI dedicated I2C Data

All five I2C busses originate in the multi-master capable I2 controllers within the T30 SoC. The only I2C devices on the sAT30 Module are on the I2C PM bus. Those devices and their address details are listed in the following table:

#	Device	Description	Ref Des	Address (7 bit)	Address (8 bit)		Notes
					Read	Write	
I2C_PM Bus							
1	TI TPS65911C	PMU	U7	0x2D	0x5B	0x5A	General purpose usage address
				0x12	0x25	0x24	Voltage scaling address
2	On Semi NCT72	Thermal Sensor	U5	0x4C	0x99	0x98	2 temperatures can be read: CPU Thermal diode +board ambient
3	Atmel AT24C32D	EEPROM	U9	0x50	0xA1	0xA0	General purpose parameter EEPROM Serial number, etc in PICMG EEEP format
4	TI TPS62361	Buck Regulator	U8	0x60	0xC1	0xC0	CPU Core Voltage Regulator

As the name implies (PM == "Power Management), this I2C bus is used by low level software for system power management. Two of the Module power regulators are attached to this bus and various voltage levels and options are continuously modified over this interface. So – use care if accessing this interface.

3.3 SMARC sAT30 Debug

3.3.1 Serial Port for Linux Debug

SMARC module has 4 serial output ports, SER0, SER1, SER2 and SER3. Out of these 4 serial ports, SER1 is set as the serial debug port use with Linux for Tegra (aka L4T). SER1 is exposed (along with all other serial ports available on the module) in the SMARC Evaluation Carrier.

SER1 pin out of the SMARC sAT30 is shown below:

NVIDIA T30 CPU		SMARC sAT30 Connector Pin		Net Name	Notes
Pin #	Pin Name	Pin #	Pin Name		
R3	ULPI_DATA0	P134	SER1_TX	SER1_TXD	Asynchronous serial port data out
V1	ULPI_DATA1	P135	SER1_RX	SER1_RXD	Asynchronous serial port data in

3.3.2 T30 CPU JTAG

A JTAG connector is provided on board for the debugging purpose. Connector Reference Designator: J2 is used for this purpose. Pin out details are provided in section 4.2.1 "Connector J2-T30 CPU JTAG".

3.4 Mechanical Specifications

3.4.1 Module Dimensions

The SMARC sAT30 complies with SMARC Hardware Specification in a 82mm x 50mm form factor.

3.4.2 Height on Top

Caution! 3.1 mm maximum (without PCB) whereas the SMARC specification defines as 3mm as the maximum.

3.4.3 Height on Bottom

Caution! 1.45 mm maximum (without PCB) whereas the SMARC specification defines as 1.3mm as the maximum.

3.4.4 Layout Diagrams

Top side major component (IC and Connector) information is shown in Figure 7 and 8: SMARC sAT30 Top side components.

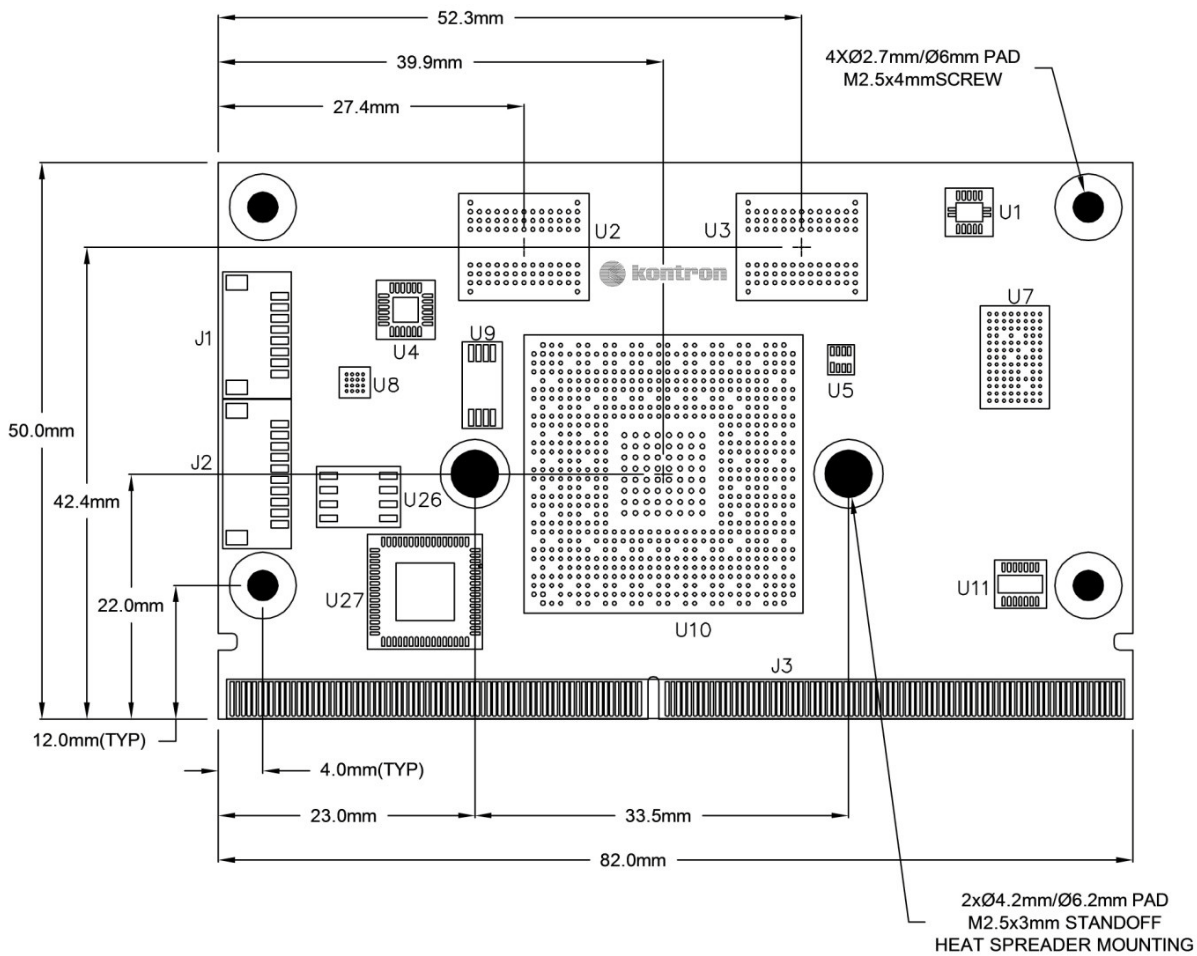

Figure 7: SMARC sAT30 Top Side Components

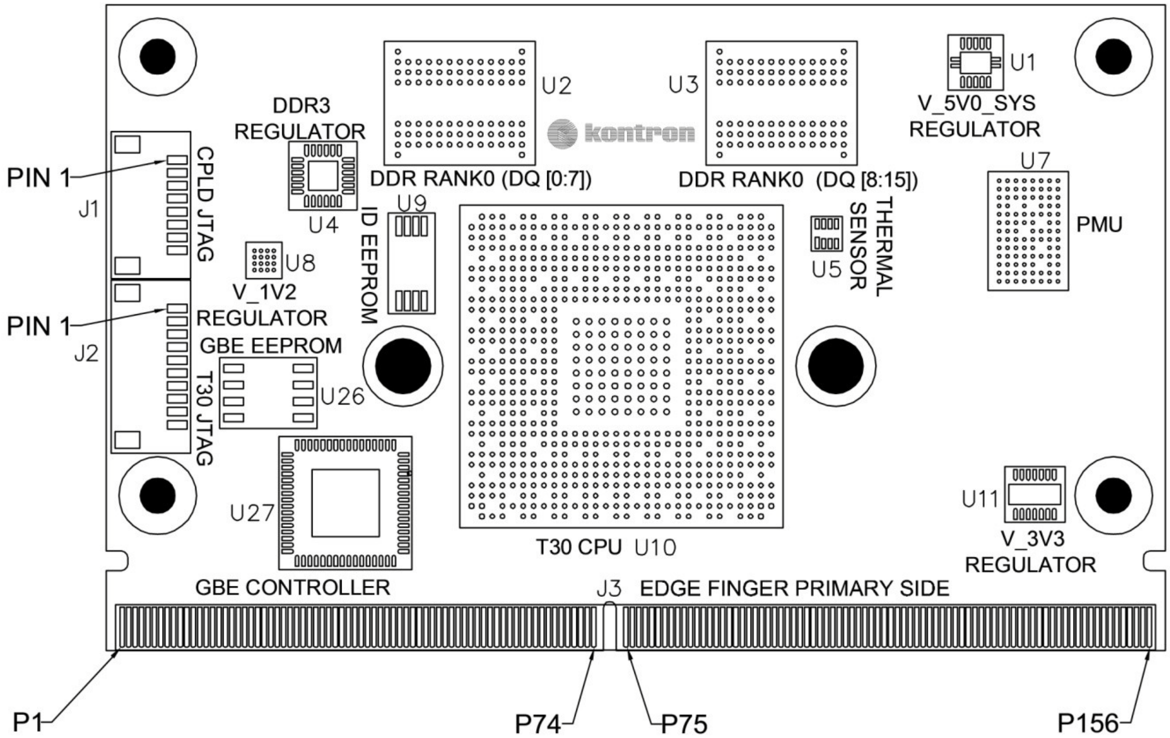

Figure 8: SMARC sAT30 Top Side Components (Labeled)

Bottom side major component (IC & Connector) information is shown in Figure 8: SMARC sAT30 Bottom Side Components. SMARC sAT30 height information is shown in Figure 9: SMARC sAT30 Edge View below:

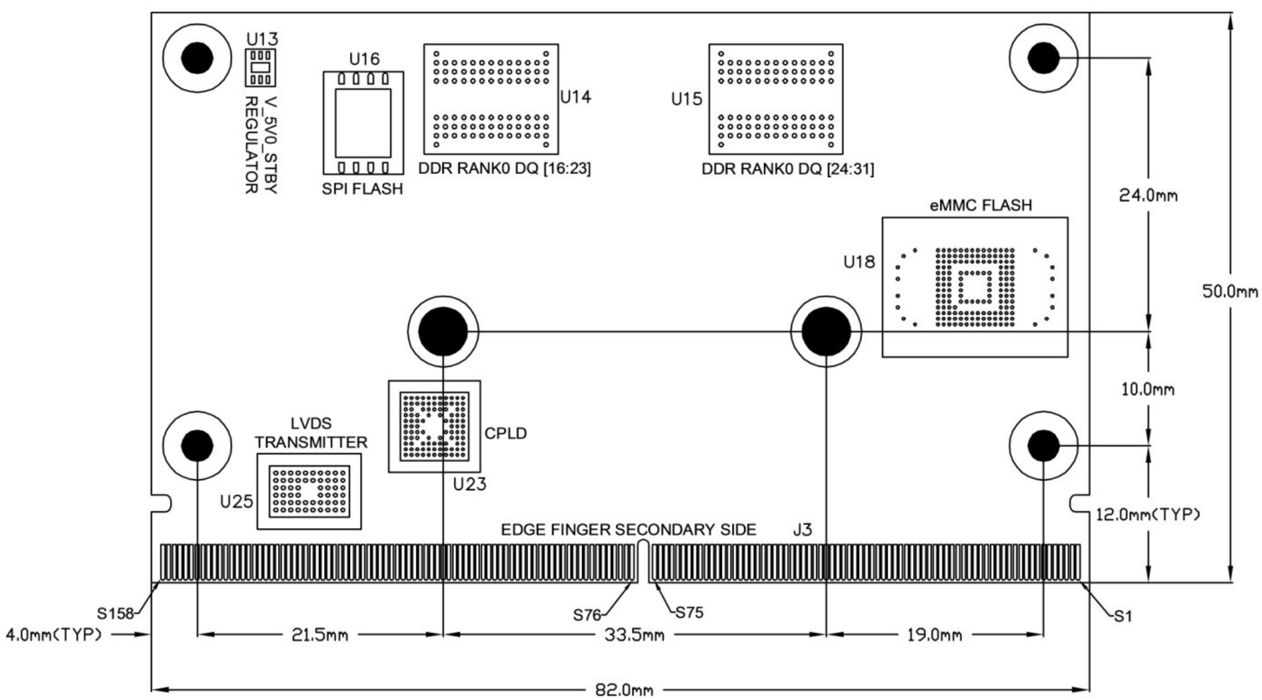

Figure 9: SMARC sAT30 Bottom Side Components

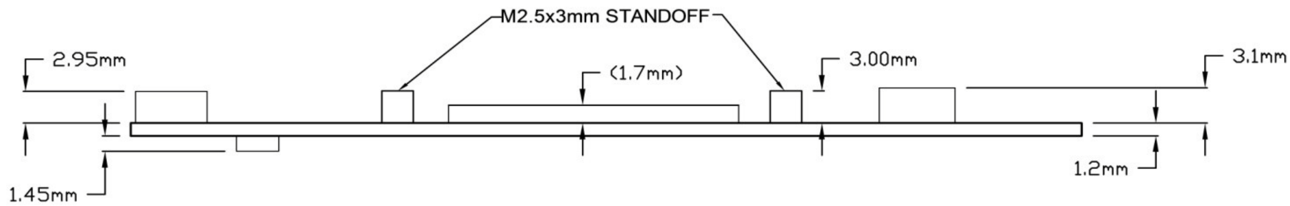

Figure 10: SMARC sAT30 Edge View

3.4.5 Module Assembly Hardware

The SMARC sAT30 module is attached to the carrier with four M2.5 screws. A 4mm length screw is usually used. The attachment holes are located on the corners of the module. Attachment holes have a 6mm diameter pad, 2.7 mm dia drill hole as shown Figure 7: SMARC sAT30 Top side components.

3.4.6 Module Cooling Solution Attachment

Two Penn Engineering and Manufacturing (PEM) (www.pemnet.com) "SMTSO" surface mount standoffs with M2.5 internal threads and 3mm stand-off height are soldered into the Module top side, adjacent to the Tegra SoC. They are provided for the attachment of a heat spreader or heat sink, independent of the corner mounting holes. The PEM SMTSO parts have excellent pull- strength and the Module PCB will deform before the standoffs can be pulled out.

The heat sink/heat spreader mounting holes are shown in Figure 7: SMARC sAT30 Top side components. The Heat Spreader is secured to the Module with two 6mm flathead M2.5 screws.

For a large-area heat spreader or heat sink, the corner holes should be used as well, with suitable standoffs.

3.5 Electrical Specification

3.5.1 Supply Voltage

The SMARC sAT30 module operates over an input voltage range of 3.1V to 5.25V. Power is provided from the carrier through 10 power pins as defined by the SMARC specification.

Caution! The SMARC specification states that the input voltage range should extend down to 3.0V. The sAT30 lower limit is determined by a non-volatile register setting in the TI PMU used.

3.5.2 RTC/Backup Voltage

3.0V RTC backup power is provided through the VDD_RTC pin from the carrier board. This connection provides back up power to the module PMU.

3.5.3 No Separate Standby Voltage

The SMARC sAT30 does not have a standby power rail. Standby operation is powered through the main supply voltage rail, as defined in the SMARC specification.

3.5.4 Module I/O Voltage

The SMARC sAT30 module complies with the default I/O voltage (1.8V) level defined by SMARC Hardware specification. Module pin S158 (VDD_IO_SEL#) is tied low on the Module, per the SMARC specification, indicating a 1.8V I/O voltage level.

3.5.5 Power Consumption

Power figures are given in the table below for the Module power consumption in various situations. These are Module power figures. Off-Module power consumption (e.g. display backlight, display power, Carrier board devices) is not included here. What is included in these power figures: everything on the Module – the Tegra SoC, the DDR3L DRAM, the eMMC memory, the Module SPI, the Module power supplies, the Module LVDS transmitter, the GBE controller and miscellaneous Module circuits. The figures below given below are subject to change.

State / Activity	CPU Freq	Module Power	USB Enabled?	PCIe + GBE Enabled?	SATA Enabled?	Notes
Active state (Linux Desktop)	1.2 GHz QC	1.6W	Yes	Yes	Yes	
Active state MPEG4 decode	1.2 GHz QC	5.5W	Yes	Yes	Yes	
Active state Stress Test	1.2 GHz QC	7.0W	Yes	Yes	Yes	All 4 cores @ 100% load
Active State MPEG4 decode	1.2 GHz QC	4.0W	Yes	No	No	
Active State MPEG4 decode	1.2 GHz QC	3.0W	Yes	No	No	"Power Save" mode enabled
Sleep State	LP1	585mW	Yes	Yes	Yes	
Deep Sleep State	LP0	310mW	Yes	Yes	Yes	
Sleep State	LP1	535mW	Yes	No	No	
Deep Sleep State	LP0	280mW	Yes	No	No	

There are many options, configurable in software. And there are trade-offs: for example, the "Power Save" option does save power and the response to events such as keyboard and mouse activity can be sluggish. Evaluation units are available from Kontron to allow users to check out some of these tradeoffs.

3.6 Environmental Specification

3.6.1 Operating Temperature

The SMARC sAT30 module operates from 0°C to 60°C air temperature, with a passive heat sink arrangement. Higher ambient temperature performance may be achieved with a passive or active cooling solution and will depend on system level thermal properties.

3.6.2 Humidity

Operating: 10% to 90% RH (non-condensing).

Non-operating: 5% to 95% RH (non-condensing).

3.6.3 RoHS Compliance

The SMARC sAT30 module is compliant to the 2002/95/EC RoHS directive.

4 Connectors

4.1 SMARC sAT30 Edge Connector Pin Mapping

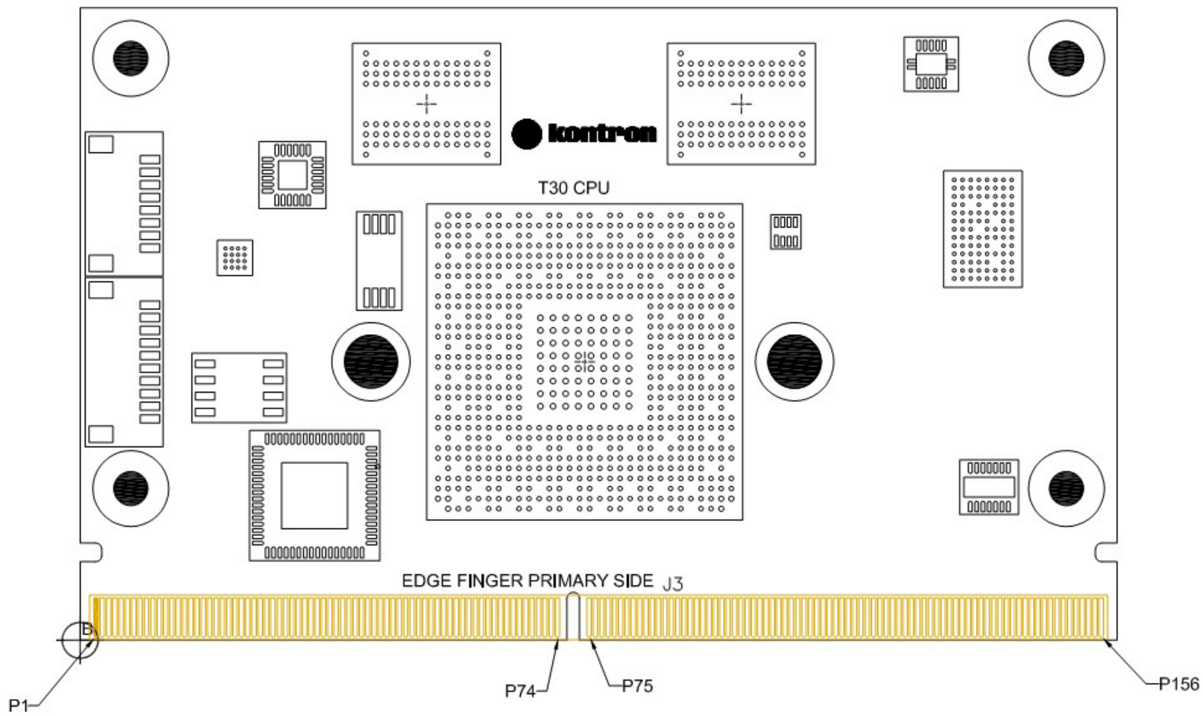

Figure 11: SMARC sAT30 edge finger primary pins

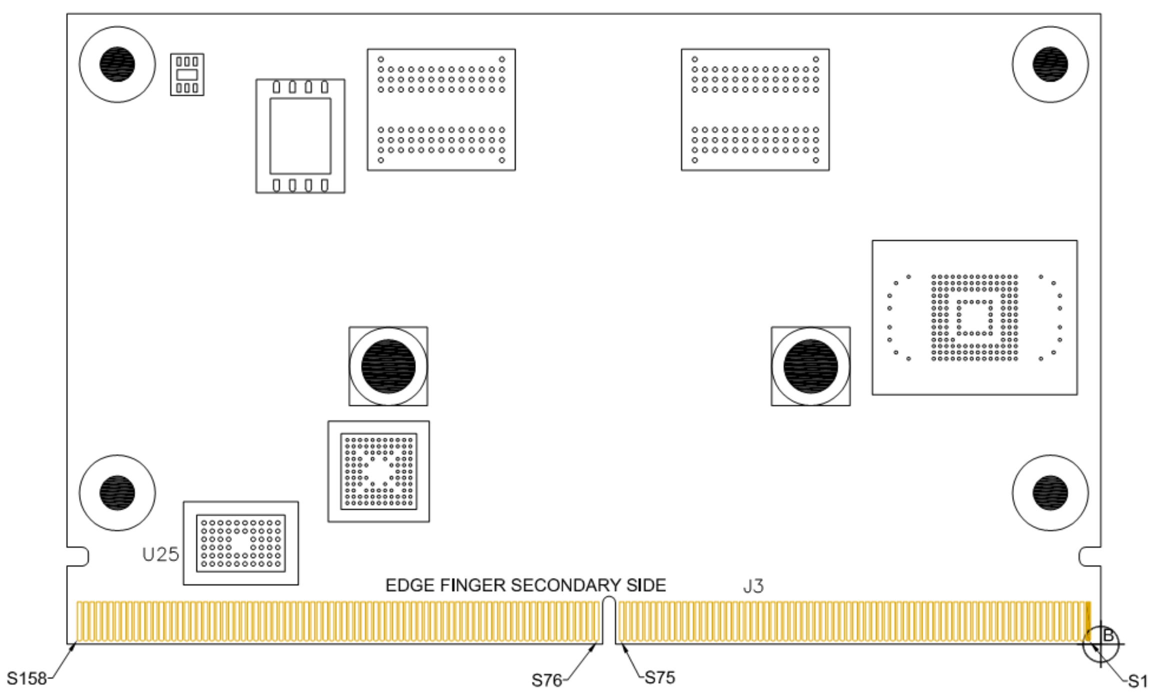

Figure 12: SMARC sAT30 edge finger secondary pins

Pin mapping between the SMARC sAT30 module edge connector and T30 SoC is shown in the table below. Connections between the edge connector and other devices on the module are not shown.

SMARC sAT30 Edge finger		NVIDIA T30 CPU		Notes
Pin #	Pin Name	Pin #	Pin Name	
P1	PCAM_PXL_CK1			Not used
P2	GND			
P3	CSI1_CK+ / PCAM_D0	AG2	CSI_CLKBP	
P4	CSI1_CK- / PCAM_D1	AG3	CSI_CLKBN	
P5	PCAM_DE			Not used
P6	PCAM_MCK			Not used
P7	CSI1_D0+ / PCAM_D2	AE1	CSI_D1BP	
P8	CSI1_D0- / PCAM_D3	AD1	CSI_D1BN	
P9	GND			
P10	CSI1_D1+ / PCAM_D4	AH1	CSI_D2BP	
P11	CSI1_D1- / PCAM_D5	AH2	CSI_D2BN	
P12	GND			
P13	CSI1_D2+ / PCAM_D6			Not used
P14	CSI1_D2- / PCAM_D7			Not used
P15	GND			
P16	CSI1_D3+ / PCAM_D8			Not used
P17	CSI1_D3- / PCAM_D9			Not used
P18	GND			
P19	GbE_MDI3-			Intel I210
P20	GbE_MDI3+			Intel I210
P21	GbE_LINK100#			Intel I210 and OD driver
P22	GbE_LINK1000#			Intel I210 and OD driver
P23	GbE_MDI2-			Intel I210

SMARC sAT30 Edge finger		NVIDIA T30 CPU		Notes
P24	GbE_MDI2+			Intel I210
P25	GbE_LINK_ACT#			Intel I210 and OD driver
P26	GbE_MDI1-			Intel I210
P27	GbE_MDI1+			Intel I210
P28	GbE_CTREF			Not used
P29	GbE_MDI0-			Intel I210
P30	GbE_MDI0+			Intel I210
P31	SPI0_CS1#	N4	ULPI_STP	
P32	GND			
P33	SDIO_WP	K5	CLK2_OUT	
P34	SDIO_CMD	N6	SDMMC1_CMD	
P35	SDIO_CD#	M5	GPIO_PV2	
P36	SDIO_CK	M6	SDMMC1_CLK	
P37	SDIO_PWR_EN	M1	GPIO_PV3	
P38	GND			
P39	SDIO_D0	K1	SDMMC1_DAT0	
P40	SDIO_D1	K2	SDMMC1_DAT1	
P41	SDIO_D2	K3	SDMMC1_DAT2	
P42	SDIO_D3	K4	SDMMC1_DAT3	
P43	SPI0_CS0#	J24	SPI1_CS0#	
P44	SPI0_CK	B28	SPI1_SCK	
P45	SPI0_DIN	F28	SPI1_MISO	
P46	SPI0_DO	F29	SPI1_MOSI	
P47	GND			
P48	SATA_TX+	AE16	SATA_L0_TXP	Through 100nF capacitor C90
P49	SATA_TX-	AD16	SATA_L0_TXN	Through 100nF capacitor C91

SMARC sAT30 Edge finger		NVIDIA T30 CPU		Notes
P50	GND			
P51	SATA_RX+	AD19	SATA_L0_RXP	Through 100nF capacitor C92
P52	SATA_RX-	AE19	SATA_L0_RXN	Through 100nF capacitor C93
P53	GND			
P54	SPI1_CS0#	G28	SPI2_CS0#	
P55	SPI1_CS1#	F25	SPI2_CS1#	
P56	SPI1_CK	D29	SPI2_SCK	
P57	SPI1_DIN	D30	SPI2_MISO	
P58	SPI1_DO	B27	SPI2_MOSI	
P59	GND			
P60	USB0+	W2	USB1_DP	
P61	USB0-	W3	USB1_DN	
P62	USB0_EN_OC#			MAXV CPLD
P63	USB0_VBUS_DET	W5	USB1_VBUS	5V VBUS power
P64	USB0_OTG_ID	T7	USB1_ID	
P65	USB1+	T5	USB2_DP	
P66	USB1-	T6	USB2_DN	
P67	USB1_EN_OC#			MAXV CPLD
P68	GND			
P69	USB2+	V2	USB3_DP	
P70	USB2-	V3	USB3_DN	
P71	USB2_EN_OC#			MAXV CPLD
P72	PCIE_C_PRSNT#			Not used
P73	PCIE_B_PRSNT#	AD25	PEX_L0_PRSNT	
P74	PCIE_A_PRSNT#	AD24	PEX_L1_PRSNT	

SMARC sAT30 Edge finger		NVIDIA T30 CPU		Notes
P75	PCIE_A_RST#	AG27	PEX_L1_RST	Provision to connect pin P75 to GMI_AD15 (F1) through a 0 ohm resistor, R302 (By default R302 is Not Installed)
P76	PCIE_C_CKREQ#			Not used
P77	PCIE_B_CKREQ#	AG24	PEX_L0_CLKREQ	
P78	PCIE_A_CKREQ#	AD26	PEX_L1_CLKREQ	
P79	GND			
P80	PCIE_C_REFCK+			Not used
P81	PCIE_C_REFCK-			Not used
P82	GND			
P83	PCIE_A_REFCK+	AB23	PEX_CLK2P	
P84	PCIE_A_REFCK-	AB24	PEX_CLK2N	
P85	GND			
P86	PCIE_A_RX+	AH24	PEX_L4_RXP	
P87	PCIE_A_RX-	AJ24	PEX_L4_RXN	
P88	GND			
P89	PCIE_A_TX+	AF21	PEX_L4_TXP	
P90	PCIE_A_TX-	AG21	PEX_L4_TXN	
P91	GND			
P92	HDMI_D2+	AJ7	HDMI_TXD2P	
P93	HDMI_D2-	AK7	HDMI_TXD2N	
P94	GND			
P95	HDMI_D1+	AJ6	HDMI_TXD1P	
P96	HDMI_D1-	AH6	HDMI_TXD1N	
P97	GND			
P98	HDMI_D0+	AH4	HDMI_TXD0P	

SMARC sAT30 Edge finger		NVIDIA T30 CPU		Notes
P99	HDMI_D0-	AJ4	HDMI_TXD0N	
P100	GND			
P101	HDMI_CK+	AK4	HDMI_TXCP	
P102	HDMI_CK-	AK3	HDMI_TXCN	
P103	GND			
P104	HDMI_HPD	AG13	HDMI_INT	
P105	HDMI_CTRL_CK	AG14	DDC_SCL	
P106	HDMI_CTRL_DAT	AJ10	DDC_SDA	
P107	HDMI_CEC	AC18	HDMI_CEC	Not used
P108	GPIO0 / CAM0_PWR#	J30	KB_COL00	
P109	GPIO1 / CAM1_PWR#	N26	KB_COL01	
P110	GPIO2 / CAM0_RST#	V25	KB_COL02	
P111	GPIO3 / CAM1_RST#	K28	SDMMC3_DAT7	
P112	GPIO4 / HDA_RST#	F26	CLK1_REQ	
P113	GPIO5 / PWM_OUT	AB27	GPIO_PU3	
P114	GPIO6 / TACHIN	AA27	GPIO_PU6	
P115	GPIO7 / PCAM_FLD	AG7	GPIO_PBB4	
P116	GPIO8 / CAN0_ERR#	T26	KB_ROW00	
P117	GPIO9 / CAN1_ERR#	M23	KB_ROW01	
P118	GPIO10	T1	ULPI_DATA6	
P119	GPIO11	T24	KB_ROW06	
P120	GND			
P121	I2C_PM_CK	M24	PWR_I2C_SCL	
P122	I2C_PM_DAT	N27	PWR_I2C_SDA	
P123	BOOT_SEL0#			MAX V CPLD
P124	BOOT_SEL1#			MAX V CPLD

SMARC sAT30 Edge finger		NVIDIA T30 CPU		Notes
P125	BOOT_SEL2#			MAX V CPLD
P126	RESET_OUT#			PMU TPS65911C and MAX V CPLD
P127	RESET_IN#			PMU TPS65911C through Level Translator
P128	POWER_BTN#			PMU TPS65911C
P129	SER0_TX	W25	UART2_TXD	
P130	SER0_RX	AB28	UART2_RXD	
P131	SER0_RTS#	AB26	UART2_RTS#	
P132	SER0_CTS#	AA25	UART2_CTS#	
P133	GND			
P134	SER1_TX	R3	ULPI_DATA0	
P135	SER1_RX	V1	ULPI_DATA1	
P136	SER2_TX	AC27	UART3_TXD	
P137	SER2_RX	W27	UART3_RXD	
P138	SER2_RTS#	AB29	UART3_RTS#	
P139	SER2_CTS#	W29	UART3_CTS#	
P140	SER3_TX	M2	ULPI_CLK	
P141	SER3_RX	M4	ULPI_DIR	
P142	GND			
P143	CAN0_TX			Not used
P144	CAN0_RX			Not used
P145	CAN1_TX			Not used
P146	CAN1_RX			Not used
P147	VDD_IN			
P148	VDD_IN			
P149	VDD_IN			
P150	VDD_IN			

SMARC sAT30 Edge finger		NVIDIA T30 CPU		Notes
P151	VDD_IN			
P152	VDD_IN			
P153	VDD_IN			
P154	VDD_IN			
P155	VDD_IN			
P156	VDD_IN			
S1	PCAM_VSYNC			Not used
S2	PCAM_HSYNC			Not used
S3	GND			
S4	PCAM_PXL_CK0			
S5	I2C_CAM_CK	AG5	CAM_I2C_SCL	
S6	CAM_MCK	AD5	CAM_MCLK	
S7	I2C_CAM_DAT	AH7	CAM_I2C_SDA	
S8	CSI0_CK+ / PCAM_D10	AD4	CSI_CLKAP	
S9	CSI0_CK- / PCAM_D11	AC4	CSI_CLKAN	
S10	GND			
S11	CSI0_D0+/PCAM_D12	AD2	CSI_D1AP	
S12	CSI0_D0-/PCAM_D13	AD3	CSI_D1AN	
S13	GND			
S14	CSI0_D1+/PCAM_D14	AE3	CSI_D2AP	
S15	CSI0_D1-/PCAM_D15	AE2	CSI_D2AN	
S16	GND			
S17	AFB0_OUT			Not used
S18	AFB1_OUT			Not used
S19	AFB2_OUT			Not used
S20	AFB3_IN			Not used

SMARC sAT30 Edgefinger		NVIDIA T30 CPU		Notes
S21	AFB4_IN			Not used
S22	AFB5_IN			Not used
S23	AFB6_PTIO			Not used
S24	AFB7_PTIO			Not used
S25	GND			
S26	SDMMC_D0	L27	SDMMC3_DAT0	
S27	SDMMC_D1	J26	SDMMC3_DAT1	
S28	SDMMC_D2	J28	SDMMC3_DAT2	
S29	SDMMC_D3	K26	SDMMC3_DAT3	
S30	SDMMC_D4			Not used
S31	SDMMC_D5			Not used
S32	SDMMC_D6			Not used
S33	SDMMC_D7			Not used
S34	GND			
S35	SDMMC_CK	G30	SDMMC3_CLK	
S36	SDMMC_CMD	J29	SDMMC3_CMD	
S37	SDMMC_RST#	K24	SDMMC3_DAT6	
S38	AUDIO_MCK	C27	CLK1_OUT	
S39	I2S0_LRCK	C29	DAP2_FS	
S40	I2S0_SDOUT	G27	DAP2_DOUT	
S41	I2S0_SDIN	F27	DAP2_DIN	
S42	I2S0_CK	C28	DAP2_SCLK	Through a 33 ohm Series resistor (R295)
S43	I2S1_LRCK	R4	DAP3_FS	
S44	I2S1_SDOUT	M3	DAP3_DOUT	
S45	I2S1_SDIN	N3	DAP3_DIN	

SMARC sAT30 Edge finger		NVIDIA T30 CPU		Notes
S46	I2S1_CK	R6	DAP3_SCLK	
S47	GND			
S48	I2C_GP_CK	G5	GEN2_I2C_SCL	
S49	I2C_GP_DAT	G7	GEN2_I2C_SDA	
S50	I2S2_LRCK	AA24	DAP4_FS	
S51	I2S2_SDOUT	W28	DAP4_DOUT	
S52	I2S2_SDIN	AA29	DAP4_DIN	
S53	I2S2_CK	AA26	DAP4_SCLK	
S54	SATA_ACT#	A3	GMI_CS3#	
S55	AFB8_PTIO			Not used
S56	AFB9_PTIO			Not used
S57	PCAM_ON_CSI0#			
S58	PCAM_ON_CSI1#			
S59	SPDIF_OUT	A28	SPDIF_OUT	
S60	SPDIF_IN	H27	SPDIF_IN	
S61	GND			
S62	AFB_DIFF0+			Not used
S63	AFB_DIFF0-			Not used
S64	GND			
S65	AFB_DIFF1+			Not used
S66	AFB_DIFF1-			Not used
S67	GND			
S68	AFB_DIFF2+			Not used
S69	AFB_DIFF2-			Not used
S70	GND			
S71	AFB_DIFF3+			Not used

SMARC sAT30 Edge finger		NVIDIA T30 CPU		Notes
S72	AFB_DIFF3-			Not used
S73	GND			
S74	AFB_DIFF4+			Not used
S75	AFB_DIFF4-			Not used
S76	PCIE_B_RST#	AG26	PEX_L0_RST#	
S77	PCIE_C_RST#			Not used
S78	PCIE_C_RX+			Not used
S79	PCIE_C_RX-			Not used
S80	GND			
S81	PCIE_C_TX+			Not used
S82	PCIE_C_TX-			Not used
S83	GND			
S84	PCIE_B_REFCK+	AK27	PEX_CLK1P	
S85	PCIE_B_REFCK-	AK28	PEX_CLK1N	
S86	GND			
S87	PCIE_B_RX+	AH19	PEX_L0_RXP	
S88	PCIE_B_RX-	AJ19	PEX_L0_RXN	
S89	GND			
S90	PCIE_B_TX+	AF18	PEX_L0_TXP	
S91	PCIE_B_TX-	AG18	PEX_L0_TXN	
S92	GND			
S93	LCD_D0	AE9	LCD_D18	
S94	LCD_D1	AE10	LCD_D19	
S95	LCD_D2	AE8	LCD_D0	
S96	LCD_D3	AF12	LCD_D1	
S97	LCD_D4	AD10	LCD_D2	

SMARC sAT30 Edgefinger		NVIDIA T30 CPU		Notes
S98	LCD_D5	AK15	LCD_D3	
S99	LCD_D6	AK16	LCD_D4	
S100	LCD_D7	AK10	LCD_D5	
S101	GND			
S102	LCD_D8	AH13	LCD_D20	
S103	LCD_D9	AH9	LCD_D21	
S104	LCD_D10	AK12	LCD_D6	
S105	LCD_D11	AG16	LCD_D7	
S106	LCD_D12	AG8	LCD_D8	
S107	LCD_D13	AD15	LCD_D9	
S108	LCD_D14	AK9	LCD_D10	
S109	LCD_D15	AJ12	LCD_D11	
S110	GND			
S111	LCD_D16	AE13	LCD_D22	
S112	LCD_D17	AK13	LCD_D23	
S113	LCD_D18	AF9	LCD_D12	
S114	LCD_D19	AC12	LCD_D13	
S115	LCD_D20	AD12	LCD_D14	
S116	LCD_D21	AE18	LCD_D15	
S117	LCD_D22	AF13	LCD_D16	
S118	LCD_D23	AH15	LCD_D17	
S119	GND			
S120	LCD_DE	AG9	LCD_DE	
S121	LCD_VS	AF10	LCD_VSYNC	
S122	LCD_HS	AF16	LCD_HSYNC	
S123	LCD_PCK	AG11	LCD_PCLK	

SMARC sAT30 Edge finger		NVIDIA T30 CPU		Notes
S124	GND			
S125	LVDS0+			LVDS Transmitter
S126	LVDS0-			LVDS Transmitter
S127	LCD_BKLT_EN	AH12	LCD_PWR2	
S128	LVDS1+			LVDS Transmitter
S129	LVDS1-			LVDS Transmitter
S130	GND			
S131	LVDS2+			LVDS Transmitter
S132	LVDS2-			LVDS Transmitter
S133	LCD_VDD_EN	AG29	VI_D06	
S134	LVDS_CK+			LVDS Transmitter
S135	LVDS_CK-			LVDS Transmitter
S136	GND			
S137	LVDS3+			LVDS Transmitter
S138	LVDS3-			LVDS Transmitter
S139	I2C_LCD_CK	AB25	GEN1_I2C_SCL	
S140	I2C_LCD_DAT	V29	GEN1_I2C_SDA	
S141	LCD_BKLT_PWM	AC25	GPIO_PU4	
S142	LCD_DUAL_PCK			MAX V CPLD
S143	GND			
S144	RSVD / EDP_HPD			Not used
S145	WDT_TIME_OUT#			MAX V CPLD
S146	PCIE_WAKE#	AF22	PEX_WAKE#	
S147	VDD_RTC			RTC Power
S148	LID#			PMU TPS65911C
S149	SLEEP#			PMU TPS65911C

SMARC sAT30 Edge finger		NVIDIA T30 CPU		Notes
S150	VIN_PWR_BAD#			PMU TPS65911C
S151	CHARGING#	T3	ULPI_DATA3	
S152	CHARGER_PRSNT#			PMU TPS65911C
S153	CARRIER_STBY#	AG30	VI_VSYNC	
S154	CARRIER_PWR_ON			PMU TPS65911C and MAX V CPLD
S155	FORCE_RECOV#	F2	GMI_OE#	Pull up/ Pull down option
S156	BATLOW#	D28	DAP1_FS	
S157	TEST#			MAX V CPLD
S158	VDD_IO_SEL#			Tied to GND to indicate 1.8V I/O

4.2 JTAG

Figure 12 shows the SMARC sAT30 JTAG connectors location and pin out.

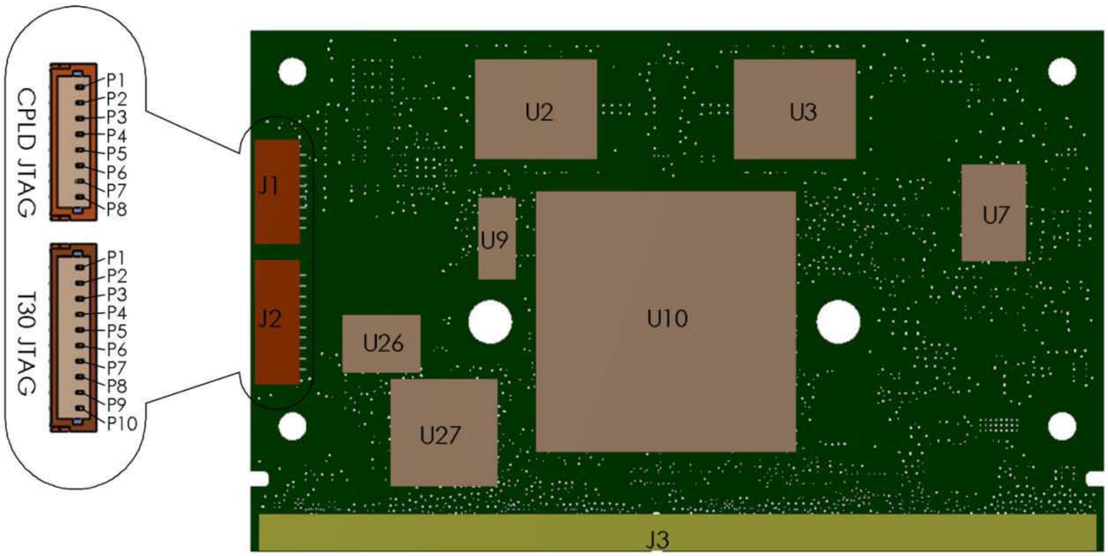

Figure 13: SMARC sAT30 JTAG Connectors

4.2.1 Connector J2-T30 CPU JTAG

T30 SoC JTAG connector pin1 & location detail is shown in the figure below:

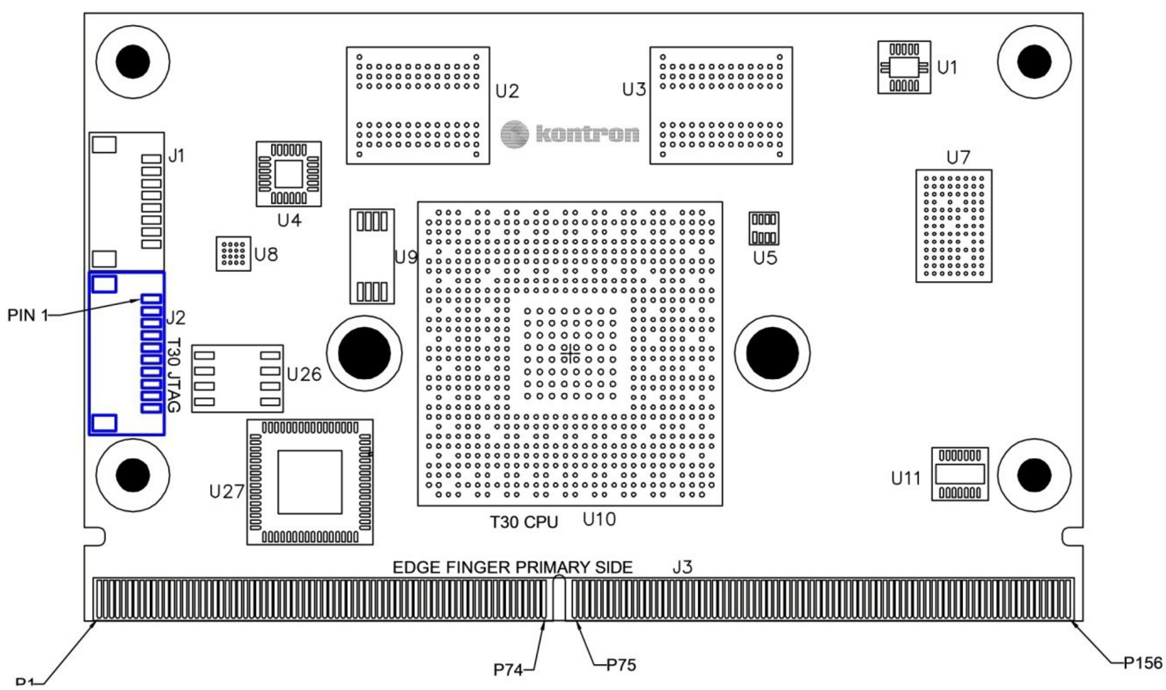

Figure 14: T30 CPU JTAG

Connector: JST SM10B-SRSS-TB, 1mm pitch R/A SMD Header.

Pin #	Signal	Notes
1	V_JTAG_T30	1.8 Volts /3.3 Volts
2	JTAG_TSRT#	
3	JTAG_TMS	
4	JTAG_TDO	
5	JTAG_TDI	
6	JTAG_TCK	
7	JTAG_RTCK	
8	GND	
9	MFG_MODE#	
10	GND	

Caution! The JTAG port is for internal use only. Do not connect any devices.

4.2.2 Connector J1 – CPLD JTAG

CPLD JTAG connector pin1 & location detail is shown in the figure below.

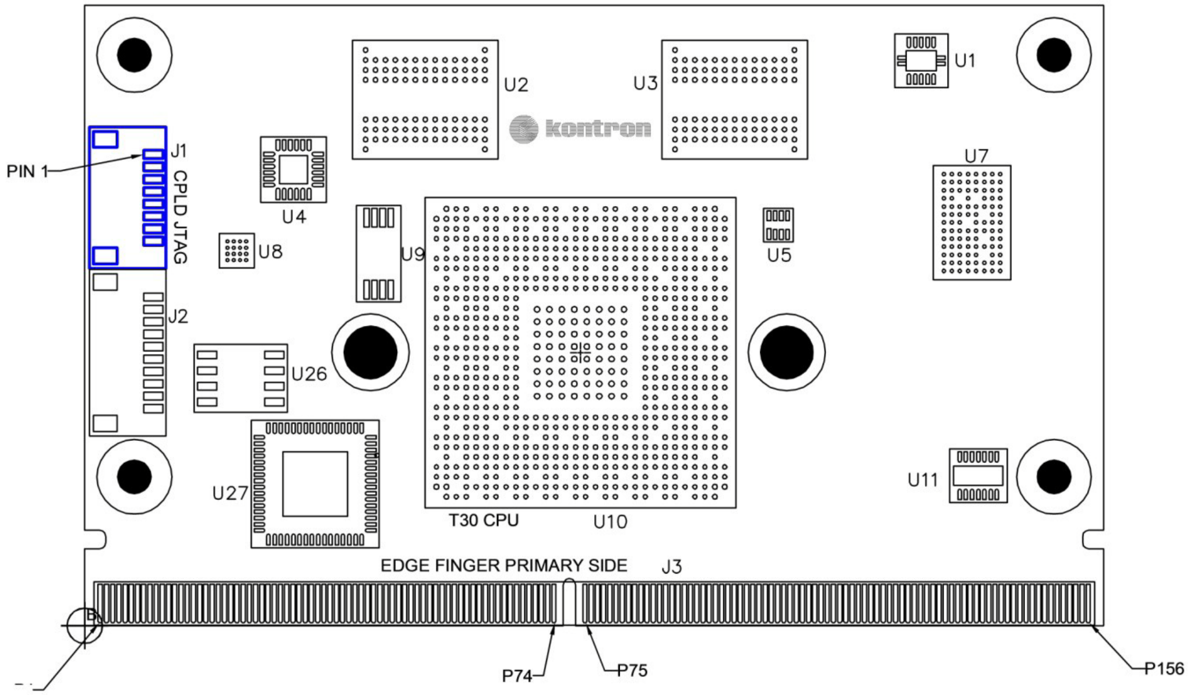

Figure 15: CPLD JTAG

Connector: JST SM08B-SRSS-TB, 1mm pitch R/A SMD Header.

Pin #	Signal	Notes
1	V_3V3	3.3 Volts
2	JTAG_CPLD_TDI	
3	JTAG_CPLD_TCK	
4	JTAG_CPLD_TMS	
5	JTAG_CPLD_TDO	
6	GND	
7	No Connect	
8	GND	

Caution! The JTAG port is for internal use only. Do not connect any devices.

5 SMARC sAT30 Special Features

5.1 Watchdog Timer

The SMARC sAT30 module implements two Watchdog Timers (WDTs). Each one of these options is described below.

5.1.1 CPLD Watchdog Timer

[TBD. This feature is yet to be implemented. This is the functionality described by the SMARC Specification]

5.1.2 Tegra T30 SoC Watchdog Timer

NVIDIA’s Tegra T30 features an internal WDT. Kontron’s Linux kernel enables the internal T30 WDT and makes this functionality available to users through the standard Linux Watchdog API.

A description of the API is available following the link below:

http://www.kernel.org/doc/Documentation/watchdog/watchdog-api.txt

5.2 PMU GPIO

The PMU on the SMARC sAT30 contains a few GPIOs. These GPIOs are used for power management functionality but can also be used for general purpose I/O. These GPIOs are different from SMARC sAT30 module hardware specification GPIOs.

The table below shows the PMU GPIO usage information details:

TI PMU TPS659110C		SMARC sAT30 Edge finger		Net name	Notes
Pin #	Pin Name	Pin #	Pin Name		
F1	SLEEP	S149	SLEEP#	CORE_PWR_REQ/ SLEEP_IN#	Default Function : Core power enable signal Alternate Function: Sleep indication from carrier board
L3	INT1			PMU_INT#	PMU Interrupt signal
N1	PWRHOLD	S150	VIN_PWR_BAD#	POWER_HOLD/ VIN_PWR_BAD#	Power bad indication from carrier board used as an option to hold the PMU power output with AND gate logic with system reset.
N2	PWRDN			AP_OVERHEAT#	High Temp warning signal

TI PMU TPS659110C		SMARC sAT30 Edge finger		Net name	Notes
L6	HDRST	P127	RESET_IN#	RESET_IN#/ SYS_RESET_IN#	Reset input to the PMU through level translator
E4	PWRON	P128	POWER_BTN#	PMU_ONKEY#/ ONKEY#	Power button input from carrier board through zero ohm resistor
H4	NRESPWRON			SYS_RESET#	System reset out signal for T30 CPU
C7	NRESPWRON2	P126	RESET_OUT#	PMU_RESET_OUT_1V8#/ RESET_OUT#	System reset out signal for the carrier board
L5	GPIO0			EN_5V_CHARGEPUMP	V_5V0_STBY Power regulator enable
F6	GPIO1			PMU_LED1#	Not Used
L2	GPIO2			EN_VDD_SoC	V_1V2 Power regulator enable
B7	GPIO3			PMU_LED2#	Not Used
H7	GPIO4	S152	CHARGER_PRESENT#	CHARGER_PRESENT/ CHARGER_PRESENT#	Charger present indication signal through level translator
G6	GPIO5	S148	LID#	LID#	Lid open/close indication
G3	GPIO6			EN_3V3_SYS	V_3V3 Power regulator enable
L4	GPIO7			EN_DDR_BUCK	V_1V35_DDR3 Power regulator enable
K5	GPIO8			EN_5V0_BUCKBOOST	V_5V0_SYS Power regulator enable

5.3 SMARC sAT30 I/O

The SMARC sAT30 module provides multiple I/O lines for various functions. 12 I/Os lines are used as interrupt capable GPIOs, which follow SMARC hardware specification. GPIO5 PWM output and GPIO6 Tachometer input support is also provided as per the SMARC hardware specification.

Caution! These details are provided for reference. Generally, access to the I/O is abstracted in the Kontron BSP packages.

GPIO functionality as well as I/O mapping to the SMARC sAT30 connector is shown below:

NVIDIA T30 CPU		SMARC sAT30 Edge finger		Net name	Notes
Pin #	Pin Name	Pin #	Pin Name		
J30	KB_COL00	P108	GPIO0 / CAM0_PWR#	GPIO0/ CAM0_PWR#	Default Function : Boot code should set this to output, high Alternate Function: CAM0 active low camera power enable
N26	KB_COL01	P109	GPIO1 / CAM1_PWR#	GPIO1/ CAM1_PWR#	Default Function : Boot code should set this to output, high Alternate Function: CAM1 active low camera power enable
V25	KB_COL02	P110	GPIO2 / CAM0_RST#	GPIO2/ CAM0_RST#	Default Function : Boot code should set this to output, high Alternate Function: CAM0 active low reset
K28	SDMMC3_DAT7	P111	GPIO3 / CAM1_RST#	GPIO3/ CAM1_RST#	Default Function : Boot code should set this to output, high Alternate Function: CAM1 active low reset
F26	CLK1_REQ	P112	GPIO4 / HDA_RST#	GPIO4 / HDA_RST#	Default Function : Boot code should set this to output, high Alternate Function: HD Audio reset, active low

NVIDIA T30 CPU		SMARC sAT30 Edge finger		Net name	Notes
AB27	GPIO_PU3	P113	GPIO5/ PWM_OUT	GPIO5/ PWM_OUT	Default Function : Boot code should set this to output, high Alternate Function: PWM output
AA27	GPIO_PU6	P114	GPIO6 / TACHIN	GPIO6/ TACHIN	Default Function : Boot code should set this to input Alternate Function: Tachometer input
AG7	GPIO_PBB4	P115	GPIO7/ PCAM_FLD	GPIO7/ PCAM_FLD	Default Function : Boot code should set this to input Alternate Function: Parallel camera field input signal
T26	KB_ROW00	P116	GPIO8/ CAN0_ERR#	GPIO8	Default Function : Boot code should set this to input Alternate Function: General purpose IO
M23	KB_ROW01	P117	GPIO9 / CAN1_ERR#	GPIO9	Default Function : Boot code should set this to input Alternate Function: General purpose IO
T1	ULPI_DATA6	P118	GPIO10	GPIO10	Default Function : Boot code should set this to input Alternate Function: General purpose IO
T24	KB_ROW06	P119	GPIO11	GPIO11	Default Function : Boot code should set this to input Alternate Function: General purpose IO
M26	KBROW09			EN_3V3_GbE	V_3V3_GbE power enable

NVIDIA T30 CPU		SMARC sAT30 Edge finger		Net name	Notes
N24	KB_ROW04			LVDS_24BITSEL	LVDS Transmitter 24 bit data enable signal
N30	KB_ROW05			LVDS_18BITSEL	LVDS Transmitter 18 bit data enable signal
M28	KB_ROW03			BOARD_ID_WP	Board ID EEPROM write protect control signal
F8	GMI_AD00			NAND_D0	Boot device strap signal
G6	GMI_AD01			NAND_D1	Boot device strap signal
D3	GMI_AD02			NAND_D2	Boot device strap signal
E4	GMI_AD03			NAND_D3	Boot device strap signal
G2	GMI_AD04			NAND_D4	BCT configuration selection strap
D2	GMI_AD05			NAND_D5	BCT configuration selection strap
B3	GMI_AD06			NAND_D6	BCT configuration selection strap
G1	GMI_AD07			NAND_D7	BCT configuration selection strap
E6	GMI_ADV#			NAND_ALE	JTAG selection strap
A4	GMI_CLK			NAND_CLE	JTAG selection strap
F2	GMI_OE#			NAND_RE#/ FORCE_RECOVERY#	Force recovery selection strap
G4	GMI_WR#			NAND_WE#	Normal operation of T30 CPU selection strap
D6	GMI_CS4#			EN_USB0_VBUS_CPLD	USB0 Power enable between T30 CPU and CPLD
J5	GMI_CS6#			EN_USB1_VBUS_CPLD	USB1 Power enable between T30 CPU and CPLD
J7	GMI_CS7#			EN_USB2_VBUS_CPLD	USB2 Power enable between T30 CPU and CPLD

NVIDIA T30 CPU		SMARC sAT30 Edge finger		Net name	Notes
F4	GMI_AD09			USB0_OC_CPLD#	USB0 Over current indication between T30 CPU and CPLD
K7	GMI_CS1#			USB1_OC_CPLD#	USB1 Over current indication between T30 CPU and CPLD
F6	GMI_CS2#			USB2_OC_CPLD#	USB2 Over current indication between T30 CPU and CPLD
J2	GMI_AD14			GbE_PCIE_DIS#	GbE disable signal
F1	GMI_AD15	P75	PCIE_A_RST#	CARD_PEX_RST#	PCIe A optional active low reset
D5	GMI_WP#			MFG_MODE_R	T30 CPU manufacturing mode control signal
A3	GMI_CS3#	S54	SATA_ACT#	SATA_ACT_LED#	SATA activity indicator
AG30	VI_VSYNC	S153	CARRIER_STBY#	CARRIER_STBY#	System standby state indication
AE27	VI_D04			LVDS_SHTDN#	LVDS Transmitter IC disable signal
AG29	VI_D06	S133	LCD_VDD_EN	EN_VDD_PNL	LCD Data power enable
AE29	VI_D08			EN_3V3_FUSE	V_3V3_Fuse power enable
AD28	VI_D09			EN_3V3_HVDDPEX	V_3V3_HVDDPEX power enable
AG6	GPIO_PCC2			TEMP_ALERT#	Excessive temperature indication signal from temperature sensor
AH12	LCD_PWR2	S127	LCD_BKLT_EN	LCD_BL_EN	LCD Backlight Enable
J27	SDMMC3_DAT4			EN_3V3_EMMC	V_3V3_EMMC power enable
K24	SDMMC3_DAT6	S37	SDMMC_RST#	WF_RST#	Reset signal to the carrier eMMC device
M5	GPIO_PV2	P35	SDIO_CD#	SDIO_CD#	SD Card detect signal

NVIDIA T30 CPU		SMARC sAT30 Edge finger		Net name	Notes
M1	GPIO_PV3	P37	SDIO_PWR_EN	SDIO_PWR_EN	SD Card Power enable
K5	CLK2_OUT	P33	SDIO_WP	SDIO_WP#	SD Card write protect indication
D28	DAP1_FS	S156	BATLOW#	BATLOW#	Low Battery indication from the carrier
AC25	GPIO_PU4	S141	LCD_BKLT_PWM	LCD_BL_PWM	LCD Backlight PWM output
T3	ULPI_DATA3	S151	CHARGING#	CHARGING#	Battery charging activity indication signal

5.4 Temperature Sensor

The SMARC sAT30 module features a temperature sensor available on the I2C_PM bus. An On Semiconductor NCT72 has been used to implement this feature. I2C address information to access this device is provided in **section 3.2.22 I2C Interface**.

The temperature sensor allows two temperatures to be read: 1) the Tegra SoC internal thermal diode and 2) the sAT30 Module ambient PCB temperature.

The temperatures can be read via Linux command line functions, or via the BSP.

To read the CPU temp, run the commands:

i2cget –y 0x4c 0x01

i2cget –y 0x4c 0x10

The first command gives you the temp (in binary) in 1°C increments.

The second command gives you added granularity (in binary) in 0.25°C increments. (Only the two MSB's are used, so you will only get; 0x00, 0x40, 0x80, 0xc0 for 0.0, 0.25, 0.50 and 0.75, respectively.

To read the local (NCT72 measured/ambient) temp run:

I2cget –y 0x4c 0x00

This will return the local temp (in binary) in 1°C increments.

There is no added granularity register for the local temp.

The CPU thermal diode readout is a valuable tool to use during system development. It should be used to characterize and qualify the system thermal solution.

5.5 SMARC sAT30 Power Management

The SMARC sAT30 module supports the following system and power management modes:

- LP0 (Deep Sleep Mode).
- LP1 (Sleep Mode).
- Active Mode.

Low Power mode support and supported resume events are software dependant. Please consult the software release notes available with the SMARC sAT30 board support package at http://emdcustomersection.kontron.com/.

5.6 Board ID EEPROM

The SMARC sAT30 module includes an I2C serial EEPROM available on the I2C_PM bus. An Atmel 24C32 or equivalent EEPROM is used in the module. The device operates at 1.8V. The Module serial EEPROM is placed at I2C slave addresses A2 A1 A0 set to 0 (I2C slave address 50 hex, 7 bit address format or A0 / A1 hex, 8 bit format) (for I2C EEPROMs, address bits A6 A5 A4 A3 are set to binary 0101 convention).

The module serial EEPROM is intended to retain module parameter information, including serial number. The module serial EEPROM data structure conforms to the PICMG® EEEP Embedded EEPROM Specification.

6 Thermal Design Considerations

6.1 Thermal Management

An optional heat spreader plate assembly is available from Kontron for the SMARC sAT30 module. The heat spreader plate on top of this assembly is NOT a heat sink. It works as a SMARC®- standard thermal interface to be used with a heat sink or other cooling device.

External cooling must be provided to maintain the heat spreader plate at proper operating temperatures. Under worst-case conditions, the cooling mechanism must maintain an ambient air and heat spreader plate temperature of 60° C or less.

The aluminum slugs and thermal pads on the underside of the heat spreader assembly implement thermal interfaces between the heat spreader plate and the major heat-generating components on the sAT30 Module. About 80% of the power dissipated within the module is conducted to the heatspreader plate and can be removed by the cooling solution.

You can use passive thermal-management solutions with the heatspreader plates. The optimum cooling solution varies, depending on the SMARC® application and environmental conditions.

6.2 Heat Spreader Dimensions

The SMARC sAT30 module includes two mounting holes for mounting the passive heat sink, located to the left and right of the T30 SoC. Heat spreader dimensions are shown in the diagram below. (TIM" stands for Thermal Interface Material)

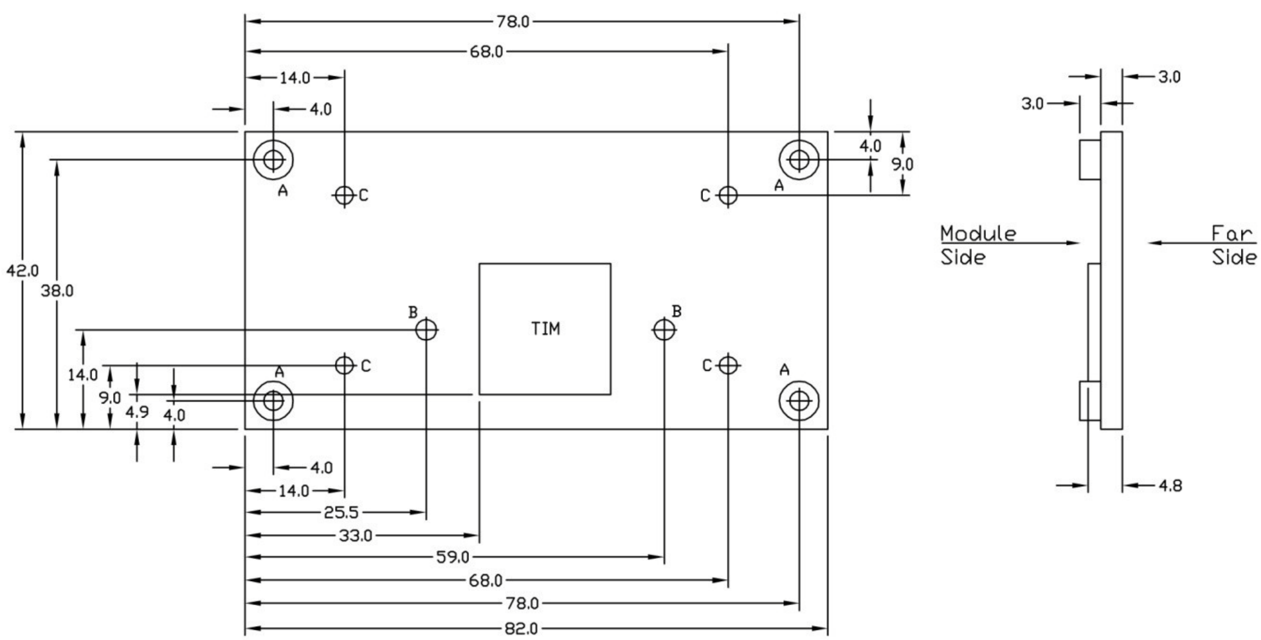

Figure 16: Heat Spreader

The table below describes the function and assembly hardware required by each of the heatspreader holes.

Hole	Heatspreader	SMARC sAT30	Evaluation Carrier
A	3mm standoffs Clearance for M2.5	Clearance holes	M2.5 Threaded Standoffs
B	Clearance for M2.5	3mm captive standoff M2.5 thread	N/A
C	M3 thread	N/A	N/A

6.3 Thermal Parameters

The T30 SoC thermal parameters are shown in the table below:

Description	Detail
Junction Temperature(Tj) max	90^0C
Thermal Resistance, CPU Junction to ambient (θ_{JA})	11.6 ^{0}C/W
Thermal Resistance, CPU Junction to case (θ_{JC})	1.18 ^{0}C/W
Thermal Resistance, CPU case to heat spreader far surface (θcs)	Less than 1 ^{0}C/W

A heat spreader is available now from Kontron for the sAT30 Module. A passive heat sink solution is pending.

6.4 Operation without a Heat Spreader / Heat Sink

The SMARC sAT30 Module is sometimes used in a room temperature environment without any heat sink at all. While it is easy and convenient, it is not generally recommended, as it can put the Tegra CPU die at or above the 90^0C limit, depending on what you are running and how system performance parameters (CPU speed, number of cores active, etc.).

At the Linux desktop, without any heat sinking at all, assuming a typical Module power consumption of 1.6W and an ambient room temperature of 23^0C, the CPU die would be at about 42^0C (1.6W * 11.6 ^{0}C/W + 23^0C). The temperature may actually be a bit less, as not all of the assumed 1.6W is going to the Tegra.

Running an MPEG4 decode, with all Module features (USB, PCIe, GBE, SATA) enabled has a typical power consumption of 5.5W. This yields a calculated CPU die temperature of 87^0C - pretty close to the Tegra limit.

The stress test, at 7W, puts the Tegra well over the die temperature limit, if there is no heat sinking.

7 SMARC sAT30 Software

7.1 Introduction

Software in the SMARC sAT30 is derived from the "Linux for Tegra" software release provided by NVIDIA. Without changing any core functionality, the software has been customized to enable native peripherals on the SMARC sAT30 module and also to support additional features (http://developer.nvidia.com/mobile/linux-tegra). The SMARC sAT30 bootloader is based in U-Boot (http://www.denx.de/wiki/U-Boot/).

7.2 Linux for Tegra

The initial customer release for the SMARC sAT30 software package is based in "Linux for Tegra" release 15, based on Linux kernel version 3.1.10. "Linux for Tegra" is an NVIDIA Linux package that has been customized to support its Tegra series processors. More details can be obtained from http://developer.nvidia.com/mobile/linux-tegra.

7.3 SMARC sAT30 Linux for Tegra Modifications

NVIDIA has made available an evaluation platform named "Cardhu". Kontron has performed a few modifications to the "Linux for Tegra" package available for "Cardhu":

» Updated U-Boot bootloader and enabled support for various LVDS panels.

» Updated Kernel configuration file to support I2C, I2S and all embedded interfaces available in the SMARC sAT30.

» Added support for a set of programmable GPIO's.

» Added support for the Intel I210 (Springville) SMARC sAT30 GbE.

» Added support for common miniPCIe WiFi devices.

» Various I2C address changes.

» Enabled SATA and PCIe.

Kontron's SMARC sAT30 software, documentation and release notes are available for download at the EMD Customer Section: http://emdcustomersection.kontron.com.

7.4 Kontron BSP (Board Support Package)

The Kontron sAT30 Module is supported by Kontron BSPs (Board Support Package). The first sAT30 BSP targets Linux support, available under Kontron part number 771-242-00. BSPs for other operating systems are planned. Check with your Kontron contact for the latest BSPs.

8 SMARC sAT30 Boot Brief

8.1 SMARC sAT30 Boot Up Sequence

The following steps define the SMARC sAT30 boot process at a high level:

1. The power supplies on the module will be up and stable at the required voltage level after powering-on the system.
2. System level hardware executes the power-up sequence. This sequence ends when system level hardware releases SYS_RESET_N.
3. The boot ROM on the Tegra 3 SoC begins executing and programs the on-chip I/O controllers to access the secondary boot device.
4. Secondary boot device will be selected based on the external boot device selection jumpers which are provided on the SMARC carrier board. Details are provided in the section 8.2 BOOT Selection.
5. The boot ROM on the Tegra 3 device fetches the Boot Configuration Table (BCT) and boot loader from the secondary boot device.
6. If the BCT and boot loader are fetched successfully, boot ROM on the Tegra 3 device yields to the boot loader. (Otherwise, boot ROM on the Tegra 3 device enters USB recovery mode.)

   Note: The SMARC sAT30 uses U-Boot boot loader.
7. The boot loader configures processor, memories and essential peripherals into known and usable state.
8. The boot loader then loads the kernel image and jump to kernel.
9. The kernel sets up the processor and all peripherals as per configuration.
10. Kernel starts various kernel daemons and processes.
11. Finally kernel loads the file system and OS desktop.

Kontron has described the SMARC sAT30 boot sequence in the “Booting SMARC” white paper available in the EMD Section (http://emdcustomersection.kontron.com). This is an interesting and insightful read. Kontron encourages users to read this document and learn how to enable the power of this architecture.

8.2 BOOT Selection

SMARC sAT30 module can be booted from various devices or modules. The boot selection is done in the carrier board. By default, module eMMC Flash is the source.

Boot options supported by SMARC sAT30 are shown in the table below:

BOOT_SEL2#	BOOT_SEL1#	BOOT_SEL0#	Boot Source
FLOAT	FLOAT	GND	Module eMMC Flash
FLOAT	FLOAT	FLOAT	Module SPI
GND	GND	GND	Carrier SATA

Caution! A BOOT_SELx# combination not contained in the table above is not valid. The SMARC sAT30 module will default to boot from the module eMMC Flash if an invalid combination is selected.

The SMARC sAT30 boot selection is provided from the module CPLD as a 4bit selection to the NVIDIA Tegra T30 SoC. The CPLD provides a 3bit selection from the carrier as shown in the table above. NAND_D [3:0] is allows pull up and pull down in the module for optional boot select configuration.

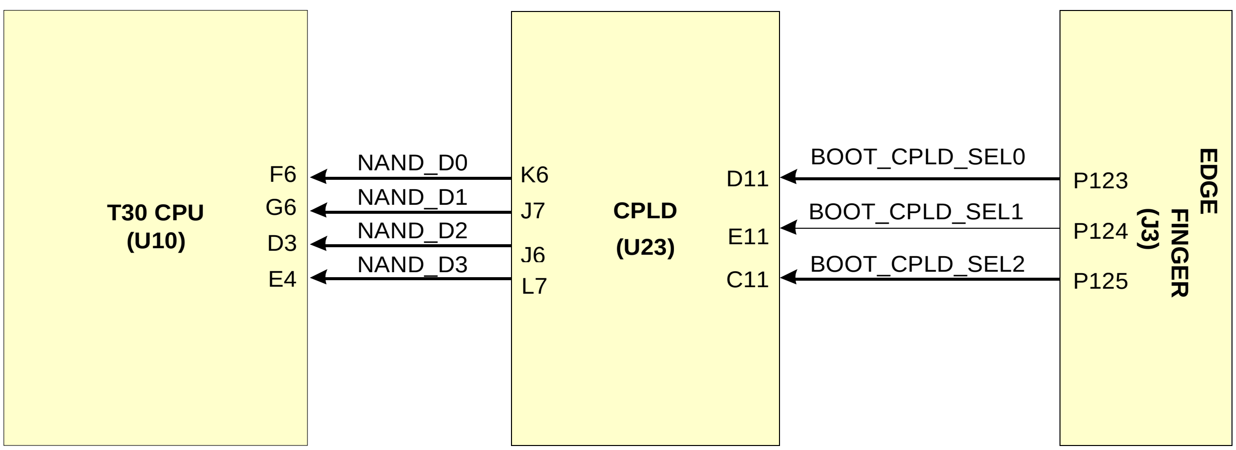

Figure 17: Boot Selection Strap Implementation

NVIDIA T30 CPU		CPLD		Net Name
Pin #	Pin Name	Pin #	Pin Name	
F8	GMI_AD00	K6	IO_K6	NAND_D0
G6	GMI_AD01	J7	IO_J7	NAND_D1
D3	GMI_AD02	J6	IO_J6	NAND_D2
E4	GMI_AD03	L7	IO_L7	NAND_D3

CPLD		SMARC sAT30 Edge finger		Net Name
Pin #	Pin Name	Pin #	Pin Name	
D11	IO_D11	P123	BOOT_SEL0#	BOOT_CPLD_SEL0
E11	IO_E11	P124	BOOT_SEL1#	BOOT_CPLD_SEL1
C11	IO_C11	P125	BOOT_SEL2#	BOOT_CPLD_SEL2

9 SMARC sAT30 Programming Methods

9.1 eMMC Flash & External SD Card Programming Using Force Recovery Method

The SMARC sAT30 module supports Force Recovery through the USB0 port. This port is configured in client mode while Force Recovery is enabled.

The following procedure is to be followed to configure the system into Force Recovery mode:

1. Hold the Reset & Force Recovery button for a few seconds. Both buttons are located in the SMARC carrier.

2. Release the Reset button initially and later release the Force Recovery button.

3. Boot firmware will be downloaded to the SMARC sAT30 module iNAND Flash boot device using a flash script provided by NVIDIA.

Boot firmware can be downloaded to the Module iNAND Flash boot device from a Linux host system. A valid SMARC sAT30 file set should be present on the host system. The file set will contain the BCT file, Boot loader, Kernel, root file system and some demo applications. Refer to the Kontron EMD Website and download a valid BSP. A sAT30 BSP will contain all files needed to flash the iNAND device. Follow the instructions contained in the sTA30 BSP.

More details can be found in the "Linux for Tegra" documentation: http://developer.nvidia.com/mobile/linux-tegra.

9.2 SPI Flash Programming

[TBD. This feature is not yet supported]

10 Appendix A: Major Components BOM

Description	Ref	MFG	MPN	Qty
IC CPU NVIDIA Tegra T30 FCBGA728	U10	NVIDIA	T30MQS-A3	1
IC PMU TPS6591104E BGA98	U7	TEXAS INSTRUMENTS	TPS6591104EA2ZRC/R	1
IC LVDS TRANSMITTER SN75LVDS83B BGA56	U25	TEXAS INSTRUMENTS	SN75LVDS83BZQLR	1
IC SPI FLASH 64 Megabit SST25VF064C WSON8	U16	MICROCHIP	SST25VF064C-80-4C-Q2AE	1
IC eMMC FLASH 16GB SDIN5D2 TFBGA169	U18	SANDISK	SDIN5D2-16G-L	1
IC GbE (Springville) WGI210AT QFN64	U27	Intel	WGI210AT	1
IC TEMP-SENSOR NCT72CMT WDFN8	U5	ON SEMICONDUCTOR	NCT72CMTR2G	1
IC EEPROM 32Kbits AT24C32D TSSOP8	U9	ATMEL	AT24C32D-XHM-T	1
IC CPLD 5M240Z MBGA100	U23	ALTERA	5M240ZM100C5N	1

11 Appendix B: Document Revision History

Revision	Date	Edited by	Changes
1.0	2012-09-27	SMilnor	Initial Public Release

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